CONTROL DATA®
DISK STORAGE UNIT

84X-ENHANCED
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LOGIC CARDS

CONTROL DATA CORPORATION

CUSTOMER ENGINEERING MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Preliminary edition.
(4-2-73)	
A	Manual released. This edition obsoletes all previous editions.
(4-9-73)	
B	Revise section four to incorporate the following logic card schematics; 1AJV, 1ALV, 1APV,
(5-1-73)	2AQV, 1ASV, AAUV, 1AVV, ECGV, 2CVV, 2FEV, 2FLV, DFPV, AFRV, 3FTV, 3GJV, 2GKV,
	2GLV, 2GNV, 2GPV, 2GSV, 3GTV, 3GUV, 2GVV, 2GWV, 2GXV, 2GYV, 2GZV, AQZV, 1RCV,
	3RLV, 3RWV, 3TWV, OWCV, GWEV, OWGV, 1WHV, 1WJV, 1WMV, 2WWV, DWZV. Also
	incorporated in this revision is Engineering Change Order PE34240.
C	Revise Section 4 to incorporate the following logic card schematics: 2BBV, ABPV, JCGV, 3FRV,
(8-10-73)	AFUV, AHEV, 2JYV, 2WGV. Also incorporated technical and editorial changes ; and
	Engineering Change Orders PE34327, PE34339.
D	Revised manual to incorporate the following Logic Card Schematics: 2BPV, AEJV, 3EJV,
(11-13-73)	3GTV, 1HAV, 1HQV, 3JCV, 3JLV, 3JMV, 3JNV, 3JPV, 3JQV, 3JRV, 3JSV, ARWV, ASAV,
	1WGV, OWYV. Also incorporated technical and editorial changes; and Engineering Change
	Order PE34396C.
E	Revised manual to incorporate the following logic card schematics BFSV, CFSV. Also incorporated
(12-5-73)	technical and editorial changes. This edition obsoletes all previous editions.
F	Manual revised to incorporate Engineering Change Orders PE34229, PE34647, PE34789, PE34873.
(5-7-74)	Technical and editorial changes affecting pages v, vi, vii, 2-1/2-2, 2-3, 2-24.1/2-24.2, 2-30.1,
	2-30.2, 3-34, 3-107, 4-42.1, 4-42.2, 4-60.1/4-60.2, 4-60.3, 4-60.4, 4-61, 4-92.1 thru 4-92.4,
	4-194, 4-195, 4-204, 4-205.
G	Revise manual to incorporate the following logic card schematics DZPN, EFSV affecting pages
(9-19-74)	vi, vii, 4-3, add pages 4-2.1 thru 4-2.4, 4-100.9 thru 4-100.12.
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PREFACE

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the disk storage unit (drive).

Logic card information is provided by four sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - Introduction to logic symbology and card construction.

Section 2 - Description of integrated circuits used in the drive. Includes pin assignments along with truth tables and/or typical waveforms.

Section 3 - Description of descrete components and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ) explains these functions and illustrates the actual discrete elements.

Section 4 - Schematics of logic cards. These schematics are arranged in alphabetical sequence of the last three characters of the card type. The first character of the card type is for internal control of card revisions.

CONTENTS

FIGURES

SECTION 1

INTRODUCTION

MAINTENANCE AIDS

GENERAL

Section 1 contains information on logic symbology, operational amplifiers, integrated circuit package configuration, discrete component descriptions and logic card diagrams.

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

Standard logic levels used are: "1" = +3 volts and "0" = 0 volts. All signals are named for their function when a "1". For non-standard logic levels or analog signal voltages, refer to applicable circuit description.

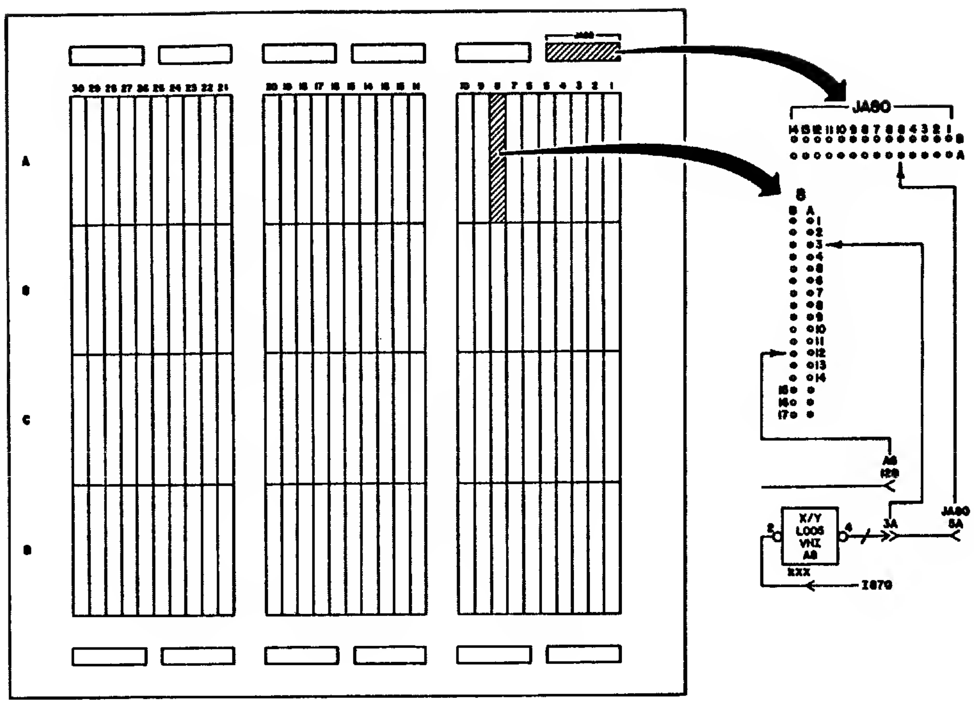
BACK PANEL

The Back Panel consists of the logic board wire wrap assembly and guiding piece parts for the logic cards.

Logic cards are plugged into the logic board wire wrap assembly. Guide rails connected to perpendicular panels guide the cards into place and restrict horizontal or vertical movement.

Wire wrap pins extend through the back panel. The logic cards mate with these pins on one side of the back panel. On the other side, the "wire wrap" side, wiring interconnects the logic functions between cards. This wiring is secured to the pins by the wire wrap technique. These pins also provide convenient test points for monitoring logic levels of all signals entering and leaving each card.

The wire wrap surface of the logic board wire wrap assembly contains wire wrap pin identification (Figure 1-1). Logic cards are designated by horizontal row (A, B, C, or D) and vertical column (1 through 30). Wire wrap pins are then called out by pin number and column A or B. For example, A8-12B is the back panel pin at logic row A, position 8, pin 12 of column B.



Wire Wrap Pin Identification

A8	Position 8 in Chassis Row A
12B	Pin number 12 in Column B
3A	Pin number 3 in Column A. When Chassis Row and Position are not listed it is identical to the one above it.
JA80	Auxiliary connector used to input or output signals to/from Back Panel.
5A	Pin number 5 in Row A

Logic Representation

X/Y	Function symbol
L005	Logic term or identifier
VHI	Circuit type designator. Alpha characters indicate discrete components, (see Part 3). Numeric characters indicate integrated circuits (see Part 2).

A8	Location of Logic Card. Connector 8 of Row A. Location of full size cards identified with top connector.
xxx	Special circuit characteristics. (Oscillator frequency, delay period, etc.)
2	Input applied to transistor Q2.
4	Output transistor (if applicable) Q4.
—/—	non Logic Level
>>,<	Pin connections.
—<—	Indicates direction of signal flow.
—I870	When no pin connections are indicated, it is a continuous fail going from preceding term to indicated term. Page number will be given if different, (xx-I870).

7J192

Figure 1-1. Wire Wrap Board Assembly

JA80 through JA85 and JA90 through JA95 are auxiliary connectors used to interface logic cards with maintenance panel, I/O connectors, etc. Pin identification is by pin number (1 through 14) and row (A or B). (JA80-5A is auxiliary connector JA80, pin 5, row A).

LOGIC CARDS

PHYSICAL DESCRIPTION

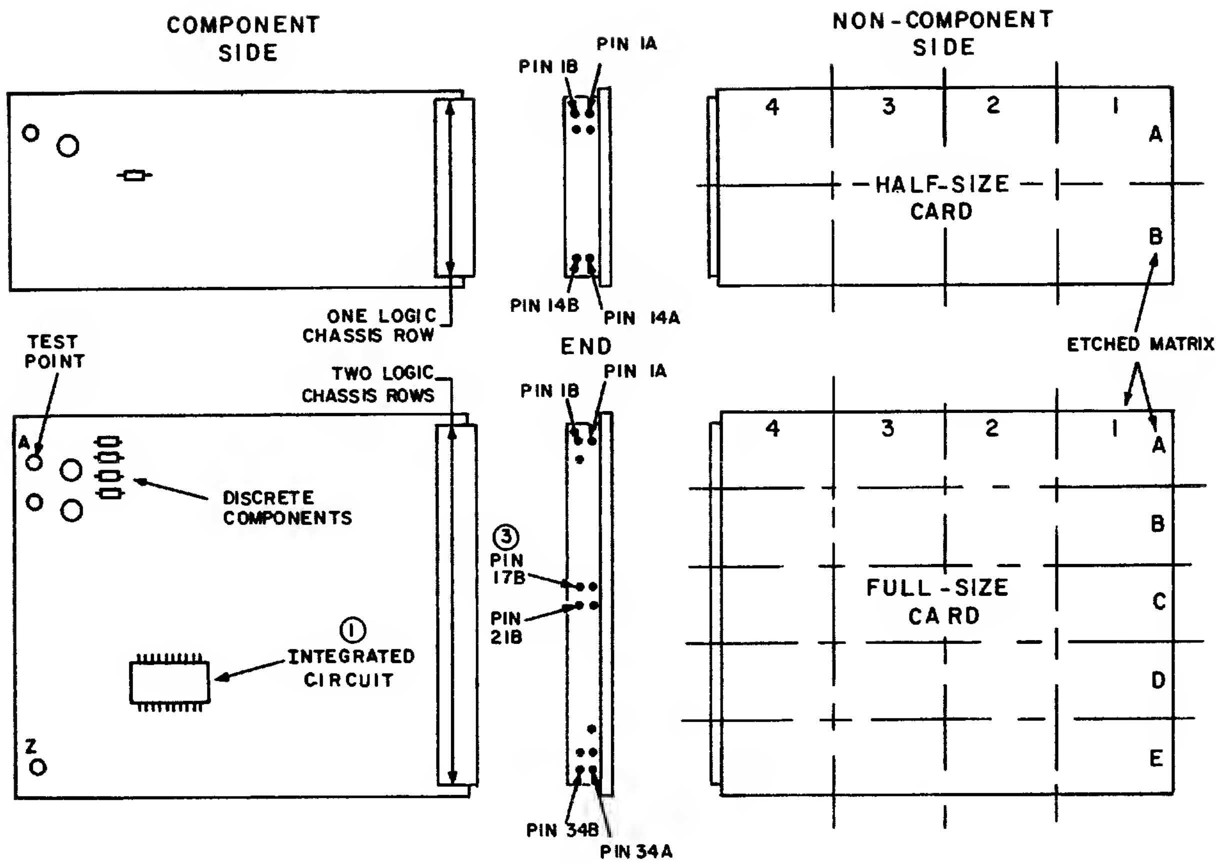
All components of the logic cards (Figure 1-2) are mounted on one side of a printed circuit board (PCB). Two sizes of PCB are used. The 6.075 x 2.3 inch PCB is called the half-size card (plugs into one logic row). The 6.075 x 4.85 inch PCB is the full-size card. The latter card spans two rows of the logic chassis.

Numerical designators (1 through 99) are etched on the non-component side of the board identify each transistor. A 4-character alpha-numeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alphanumeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

PIN ASSIGNMENTS

Half-size cards are equipped with a 28-pin (sockets) connector, while the full-size card contains a 62-pin connector. Connectors are mounted along the shorter dimension on the component side of the board.

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34, however pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.



NOTES:

① INTEGRATED CIRCUIT LOCATED AT BOARD MATRIX D2

2. ON LOGIC DRAWINGS, CARD PINS AND MATRIX LOCATIONS, ARE PRECEDED BY 3 DIGITS THAT IDENTIFY LOCATION OF CARD IN LOGIC CHASSIS (A23, POSITION 23 IN CHASSIS ROW A)

③ PINS 18, 19, 20, (A AND B) NOT PRESENT

6T6

Figure 1-2. Logic Card Detail

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

TEST POINTS

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alphanumerically starting with A on the top, outer edge. Test points A and Z are available for ground reference on full-size cards. Only test point Z is available for ground reference on half-size cards.

LOGIC SYMBOLOGY

INPUT/OUTPUT STATE INDICATORS

Input/output state indicators are the polarity indicator (or) and the logic negation indicator (or).

The input polarity indicator indicates the most negative potential is required to satisfy the logic function represented by the qualifying symbol. The output polarity indicator indicates the most negative potential is present at the output when the logic function is satisfied. The absence of the polarity indicator indicates the most positive potential is present.

The logic negation indicator is a small circle located at the origin or termination of a signal line, and tangent to a logic symbol. The presence or absence of this indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a "0" logic level on that line is needed to satisfy the function. The absence of the circle represents a logical "1" as needed to satisfy the function.

The relative level indicator depicts the occurrence of inversion. Figure 1-3 shows some representative examples of the relative level indicator being used in this manner.

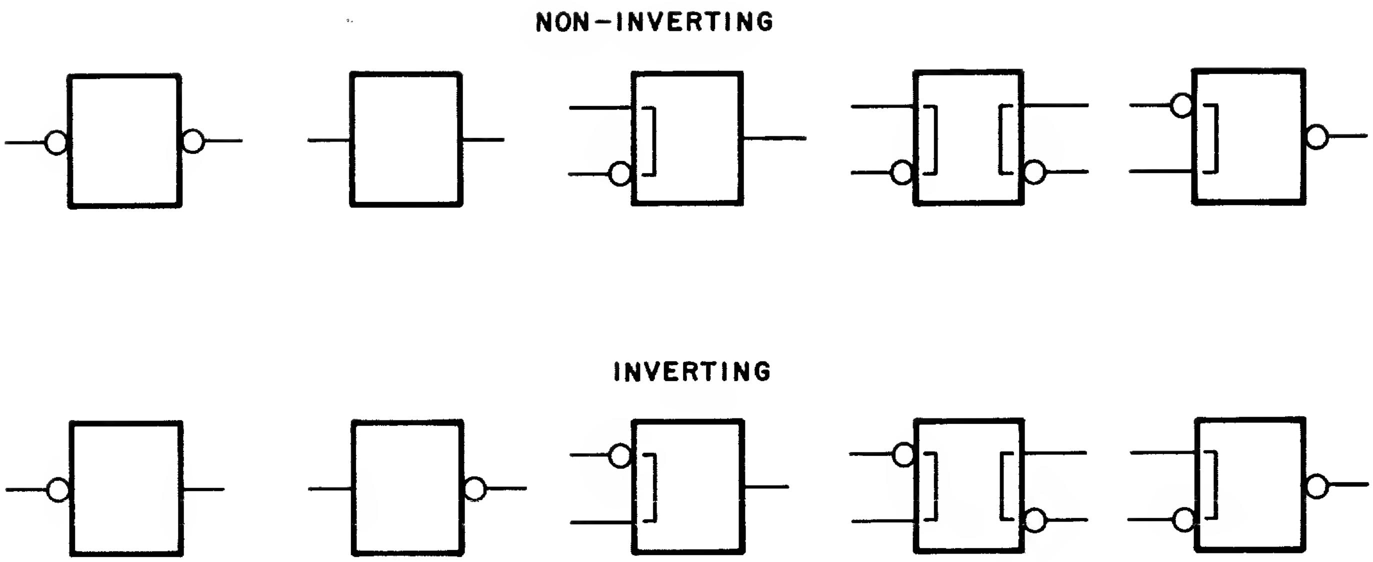


Figure 1-3. Inversion Conventions

DYNAMIC INDICATOR

The presence of a dynamic indicator (▷) just inside a symbol indicates the inputs are gated (satisfied) with the dynamic positive-going transition of the input line to the state shown. A logic negation indicator (circle) accompanying the dynamic indicator signifies that a negative-going transition is required to gate in the inputs. Absence of the dynamic indicator indicates the inputs are gated (satisfied) with the static state of the input line.

SIGNAL LINE INDICATORS

Non-Standard Levels

Some signal line indicators indicate non-standard levels on input/output lines. These signal line indicators are as follows:

 non-standard logic levels

 analog or non-logic levels

 variable control

Absence of these indicators shown above indicates a standard logic level.

Inhibit

The inhibit line indicates gating of the logic function will be inhibited whenever the line is at the level indicated by the logic negation indicator. Inhibit line symbols are as follows:

 with logic negation indicator

 without logic negation indicator

Miscellaneous

Other signal line indicators are as follows:

 test point

 twisted pair

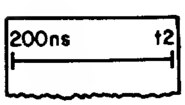
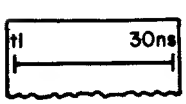
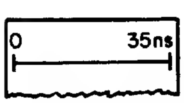
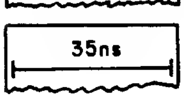
FUNCTION SYMBOLS

Circuit function symbols for discrete components and integrated circuits are as follows:

1 OR gate or inverter

& AND gate

=1	exclusive OR
▷	amplifier (with or without gain)
	amplifier with adjustable gain
Σ▷	summing amplifier
∫▷	integrating amplifier
∂▷	differentiating amplifier
X/▷	digital to analog conversion
	digital to analog conversion with adjustable gain
▷/Y	analog to digital conversion
▷X/Y	amplifying level translator (gain noted outside box)
|▷|	positive analog rectifier (symbol preceded by a minus sign if negative rectification is used)
ΣX/▷	analog summation of digital inputs. Reference voltage outside box indicates output signal level resulting when specified input(s) are negated
	Schmitt trigger
	saturable, non-linear, gain controlled amplifier
F▷	function generator
∩▷	active bandpass filter
∩	bandpass or resonant circuit

X → Y	coder
X/Y	Level conversion - transmission line to logic level, switch state (ground or open) to logic level, logic level to power output (to drive lamp, relay, solenoid, etc.)
∫X/Y	integrating level translator
	variable gain source amplifier
	switch receiver with integrating of digital signal and hysteresis
	retriggerable multivibrator (single shot)
	voltage controlled, free running multivibrator
>50 HZ	frequency sensor
000	odd parity generator
00	even parity generator
	symmetry restoration circuit
	ones delay - when input changes to a "1" a 200 nsec delay occurs before the "1" is passed on
	zeros delay - when input changes to a "0" a 30 nsec delay occurs before the "0" is passed on
	0 → 1 is not delayed. 1 → 0 delayed by 35 nsec
	both transistors are delayed by 35 nsec.

INPUT/OUTPUT DESIGNATORS

Inputs are individually identified as necessary by an input designator inside the symbol block and adjacent to the left side following all prefixes indicating dependency. These input designators follow:

R	reset or clear
S	set
G	gating type input that affects other inputs or outputs
J	J input of J-K flip-flop
K	K input of J-K flip-flop
Z	used to link gating (clock) input of control block to J and K inputs of J-K flip flops
T	toggle or complement input
D	data input of D-type flip-flops
C	a gating (clock input for D-type flip-flops
→	shift right (or down)
←	shift left (or up)
+1	increase contents by one (count up)
−1	decrease contents by one (count down)
] OR [	indicates grouped inputs that maintain a fixed relationship in states and always change together

1, 2, 4, 8	indicates relative weighting of inputs or outputs in codes. They may be consecutive, binary, decimal representation of binary values, etc.
A, B, C, ETC.	when two or more of these are used together in inputs to a symbol, it indicates individual signals or individual groups of signals to be identified for further operations such as arithmetic functions

Certain input designators (C and G) may also be used as prefixes to other input designators, but not to each other, C and G indicate dependency of every designator, such as D, they prefix, and are referred to as dependency notation. For example, CD indicates that the input is gated to a D-type flip-flop only when the C input is active. Gate dependent inputs (G) may be distinguished from each other by 1, 2, etc. following the G. Where more than a single G term is involved, commas are used to separate the numbers. Clock dependent inputs for loading data are denoted by a "C". Different C inputs are distinguished by a number following the C.

COMMON CONTROL BLOCK

Signals entering the common control block (Figure 1-4) are common to more than one section of the circuit. The neckof the common control block abuts the top or bottom of the sections it controls. Input designators may include C, G, R, →, ←, +1, -1, plus select lines with or without decoding.

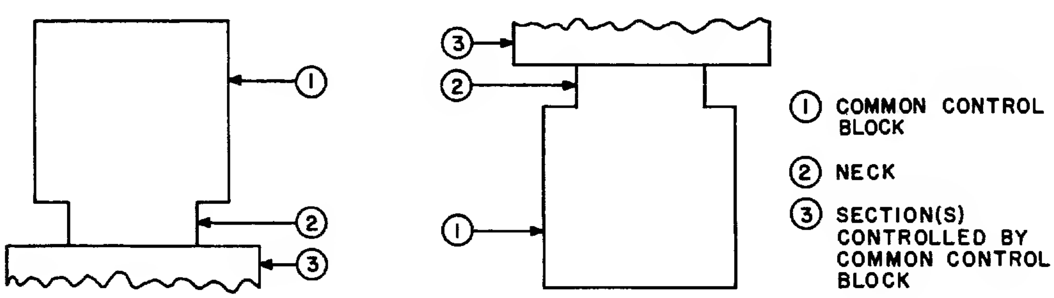


Figure 1-4. Common Control Block

WIRED FUNCTIONS

The logical representation for wired functions is shown in Figure 1-5. These functions are used where circuits have the capability of being combined as an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function simply requires that one of the inputs be a logic "0" before the output can be a logic "0". The wired AND output will be a logic "1" only when both inputs are logic "1's".

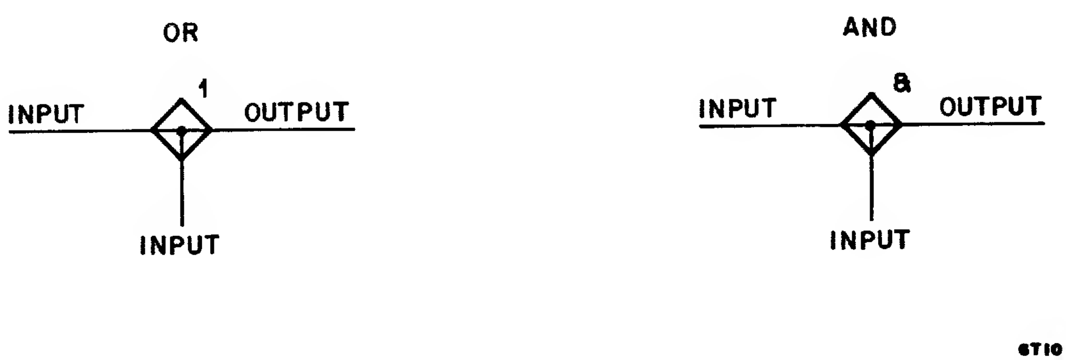


Figure 1-5. Wired Functions

INTEGRATED CIRCUITS

Figure 1-6 shows the schematic version (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

Referring to Figure 1-6 it is apparent that the two versions are essentially the same. Both views identify pin numbers, the function symbol, and the CDC element number for the circuit. Refer to Section 2 for manufacturer's information on the various element numbers. One line of information appears on the logic version that does not appear on the schematic block. This is the logic term designator which identifies this term on a logic drawing. No other logic term has the same term designator as another term.

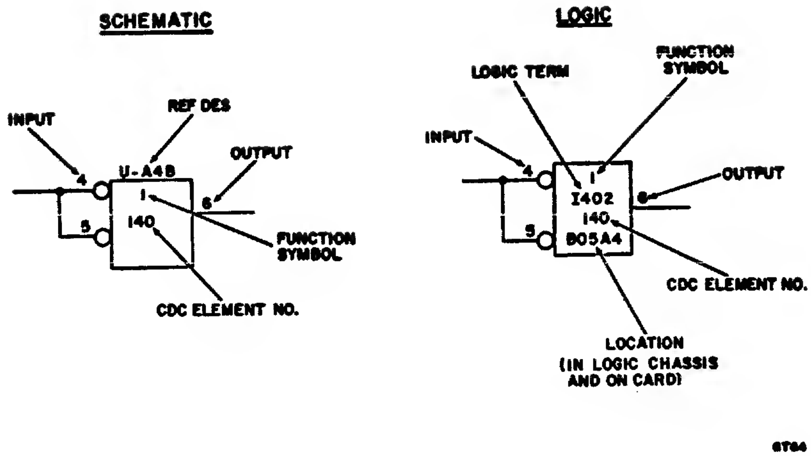


Figure 1-6. Integrated Circuit

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbols reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5 of row B.

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can amplify signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used extensively in the drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain.
2. Infinite input resistance.
3. Zero output resistance.
4. Zero offset: output is zero when input is zero.
5. High bandwidth frequency response.

BASIC CIRCUIT ELEMENTS

Figure 1-7 is a highly simplified schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

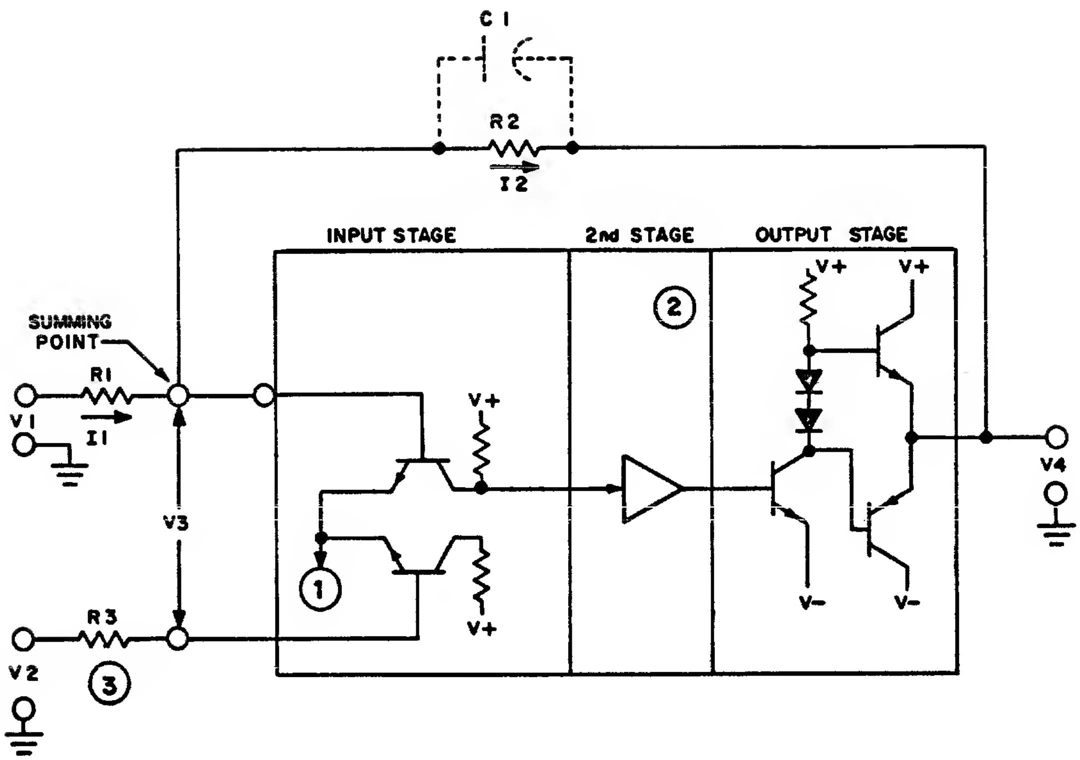
INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FETs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 millivolts are applied to the non-inverting input while 9 millivolts are applied to the inverting input, the extra 1 millivolt difference is amplified. The amplification, which may be a voltage gain of up to 100, 000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the "common-mode" input signal. In the preceding example, the 9 mv are the common-mode input, while 1 mv is the differential input. In the ideal op amp, the output is zero with identical inputs. Only the difference (1 mv) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.



NOTES;

1. TO COMMON CONSTANT-CURRENT SOURCE.

2. NOT APPLICABLE TO ALL TYPES. REFER TO MANUFACTURER'S DATA SHEET.

3. FOR BALANCED INPUT IMPEDANCE,

$$R3 = \frac{R1\ R2}{R1+R2}$$

7J133

Figure 1-7. Simplified Op Amp Schematic

BASIC CIRCUIT FUNCTIONS (FIGURE 1-7)

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio of R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; it can be assumed to be zero.
2. The differential voltage (V3) is insignificant and can be assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current II1) entering the summing point must leave it (I2). These currents are:

I1 = V1/R1

I2 = -V4/R2

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohms Law:

V4/V1 = -R2/R1 or V4 = -V1(R21R1)

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, as frequency increases, the effective impedance of R2-C1 decreases to reduce overall gain.

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset, that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made to be equal, that is, they see equal input impedances, they are common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule #2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a "virtual" ground, that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

Typical op amp circuit functions are illustrated in Figure 1-8.

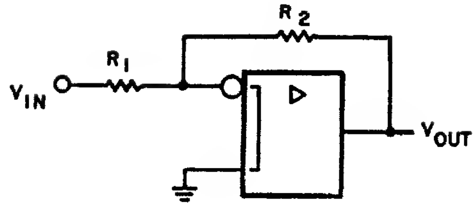
SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (Figure 1-9). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

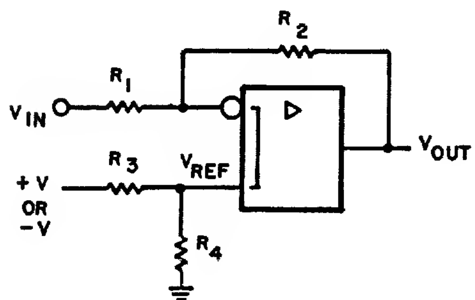
CIRCUIT TYPE — SYMBOL — OUTPUT ①

INVERTING AMP



$$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$$

INVERTING AMP WITH REFERENCE VOLTAGE



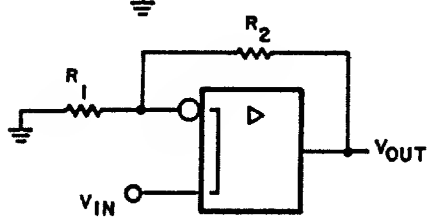
$$V_{OUT} = V_{REF} + \frac{R_2 (V_{REF} - V_{IN})}{R_1}$$

OBSERVE ALGEBRAIC SIGNS IF COMPUTING

$V_{OUT} = 0$ IF $V_{IN} = V_{REF}$

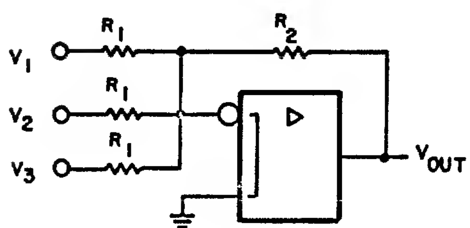
$$V_{REF} = \pm V\left(\frac{R_3}{R_3 + R_4}\right)$$

NON INVERTING AMPLIFIER



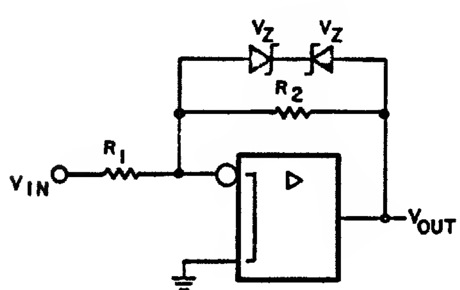
$$V_{OUT} = \frac{V_{IN} (R_1 + R_2)}{R_1}$$

SUMMING AMPLIFIER



$$V_{OUT} = -\left[\frac{R_2}{R_1} (V_1 + V_2 + V_3)\right]$$

INVERTING AMPLIFIER WITH OUTPUT LIMITING



$$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$$

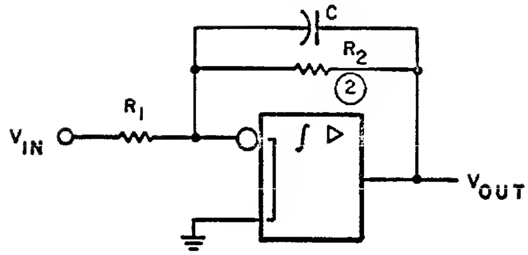
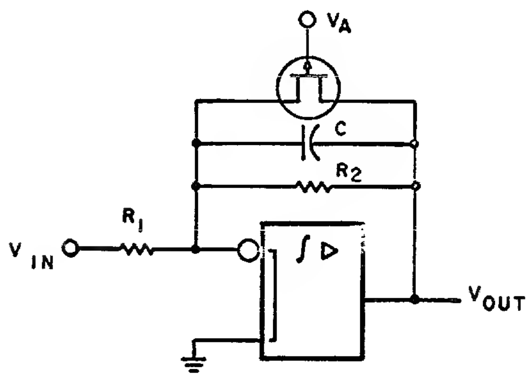
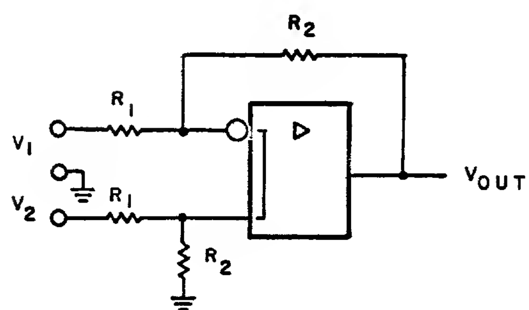
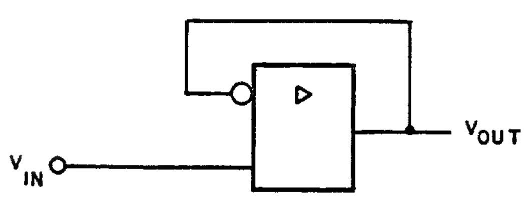
IF $\pm V_{OUT} \leq V_Z$

NOTE:

① MINUS SIGN (−) INDICATES THAT OUTPUT IS INVERTED.

7J91-1

Figure 1-8. Op Amp Circuit Functions (Sheet 1 of 3)

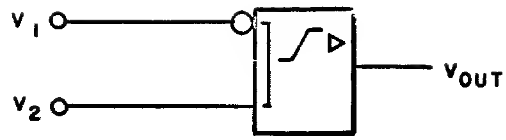
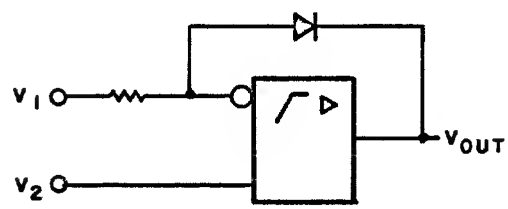
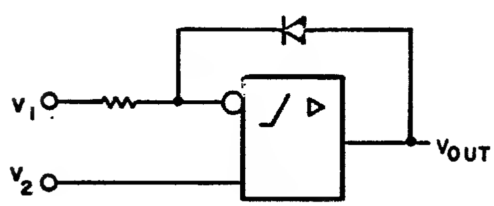
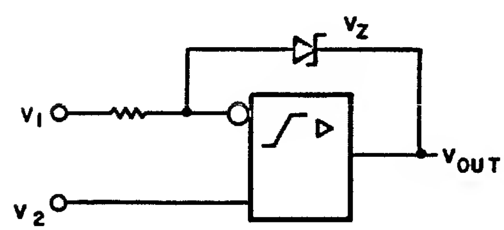
CIRCUIT TYPE	SYMBOL	OUTPUT[1]
INTEGRATING AMPLIFIER		$V_{OUT} = -\frac{1}{R_1 C}\int V_{IN}\,dt$ IF V_{IN} IS CONSTANT, $V_O = -\frac{V_{IN} \times TIME}{R_1 C}$
INTEGRATING AMPLIFIER CONTROLLED BY P-CHANNEL JFET		(A) IF V_A IS 0V $V_{OUT} = 0\,V$ (B) IF V_A IS +14V $V_{OUT} = -\frac{1}{R_1 C}\int V_{IN}\,dt$
DIFFERENTIAL AMPLIFIER		$V_{OUT} = \frac{R_2\,(V_2 - V_1)}{R_1}$
VOLTAGE FOLLOWER		$V_{OUT} = V_{IN}$

NOTES:

1. MINUS SIGN (−) INDICATES THAT OUTPUT IS INVERTED.
2. R_2 USED TO PROVIDE DC FEEDBACK TO KEEP OUTPUT SYMMETRICAL ABOUT GROUND.

7J91-2

Figure 1-8. Op Amp Circuit Functions (Sheet 2 of 3)

CIRCUIT TYPE	SYMBOL	FUNCTION
OPEN LOOP (COMPARATOR)		$V_{OUT} = +V_{SAT}$ [1] IF $V_1 < V_2$ $V_{OUT} = 0V$ IF $V_1 = V_2$ $V_{OUT} = -V_{SAT}$ [1] IF $V_1 > V_2$
SATURABLE COMPARATOR		$V_{OUT} = +V_{SAT}$ [1] IF $V_1 < V_2$ $V_{OUT} = 0V$ IF $V_1 = V_2$ $V_{OUT} = V_2$ IF $V_1 > V_2$
SATURABLE COMPARATOR		$V_{OUT} = V_2$ IF $V_1 < V_2$ $V_{OUT} = 0V$ IF $V_1 = V_2$ $V_{OUT} = -V_{SAT}$ [1] IF $V_1 > V_2$
NONLINEAR COMPARATOR		$V_{OUT} = V_Z$ IF $V_1 < V_2$ $V_{OUT} = 0V$ IF $V_1 = V_2$ $V_{OUT} = V_2$ IF $V_1 > V_2$

NOTE:

(1) V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10{,}000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

7491-3

Figure 1-8. Op Amp Circuit Functions (Sheet 3 of 3)

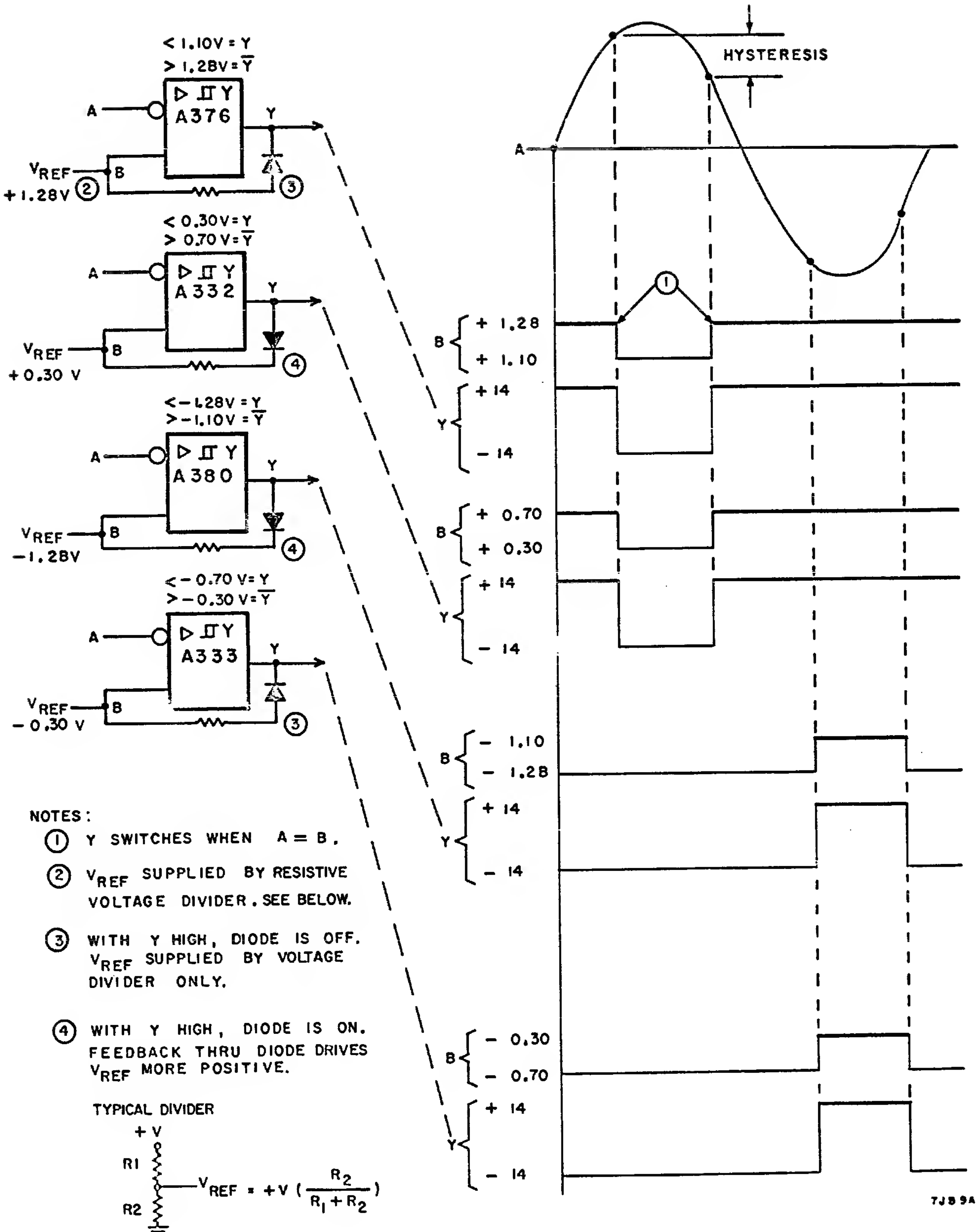


Figure 1-9. Op Amp used as a Schmitt Trigger

Consider A376 of Figure 1-9. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28V. Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

As the input A goes more positive, the output does not change until A equals B (+1.28V). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14V available at Y, the voltage at B is reduced to +1.10V. The input must now swing to less than +1.10V for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

DISCRETE COMPONENT CIRCUITS

Figure 1-10 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Four lines of information are contained within the logic symbol. The top line is the function symbol and designates the board logic function of that particular symbol. In this case,   represents an amplifier, the logic function performed by the circuit. The third line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator, detailed information on that particular circuit may be obtained by referring to Section 3.

The second line within the symbol is used to differentiate that particular symbol from similar symbols that appear on the logic diagram. It is called the logic term and consists of a one-letter prefix and an assigned identification number (in this case, A705).

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (i.e., Q22 on the card schematic diagram).

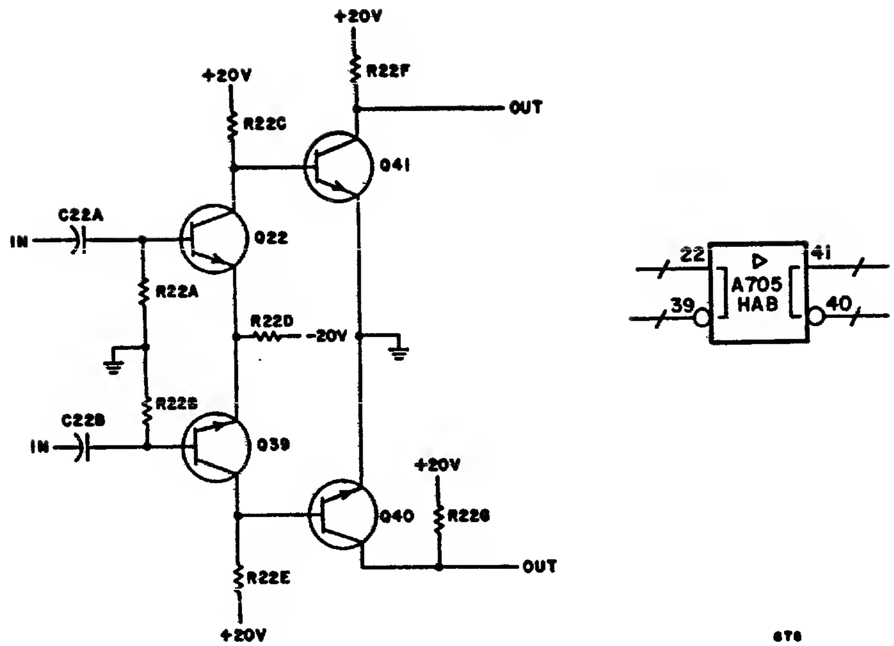


Figure 1-10. Discrete Component Circuit

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

The lines on the interior of the logic block that bracket both inputs and both outputs show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

For schematic diagrams of discrete component circuits used in this device see Section 3. An analysis of circuit operation supports each circuit diagram. The order of presentation is in accordance with the 3-letter alphabetical circuit type designator.

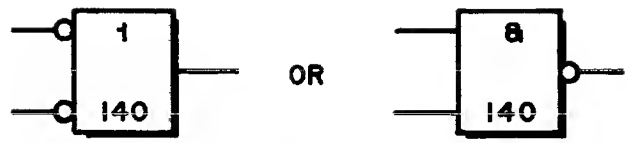
SECTION 2

INTEGRATED CIRCUIT PACKAGE CONFIGURATIONS

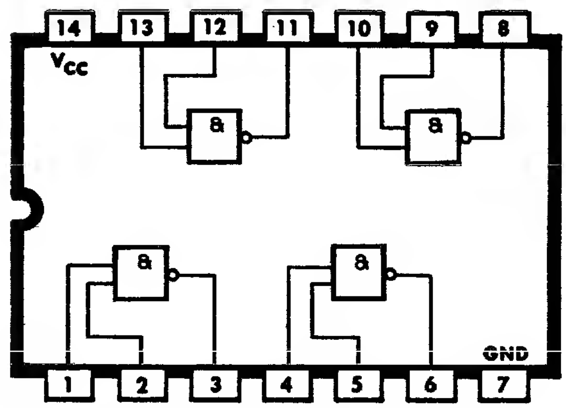
INTEGRATED CIRCUIT INDEX				
CDC Circuit Type	CDC Part No.	MFGR **	MFGR's Part No.	Revision Date
139*	51657100	F	U5F771139X	9-29-72
140	51651900	F	9002	4-10-72
140S	50254600	T	74S00	4-10-72
141	50250700	F	9003	4-10-72
143	51639900	F	9009	4-10-72
143S	50254800	T	74S40	4-10-72
144	41523200	F	9001	4-10-72
145	51701900	F	9005	4-10-72
146	51701800	F	9016	4-10-72
147	50251900	F	9007	4-10-72
149H	50251800	M	3021	4-10-72
158	51761500	F	9316	4-10-72
159	51754700	F	9300	4-10-72
161	51718600	F	9601	4-10-72
162	50252900	T	75107	12-1-72
164H	50250900	M	3062	4-10-72
164S	50255000	T	74S113	4-10-72
166	50252200	F	9312	4-10-72
172H	50251600	M	3002	4-10-72
173H	50251700	M	3004	9-29-72
175H	50251500	M	3060	12-1-72
176	50252800	T	75110	4-10-72
182	50252000	T	74197	9-29-72
182	50252000	S	8291	9-29-72
188	51783900	F	9015	5-7-74
189	51784000	F	9322	4-10-72
191	95305700	F	9301	4-10-72
193	50254300	T	74123	12-1-72
195	15104300	F	9602	12-1-72
200	50254200	T	7406	9-29-72
208S	50254900	T	74S20	4-10-72
218	15107500	M	3003	5-7-74
300*	84667800	F	UB5770939X	9-29-72
301*	50251300	F	U5B7741393	9-29-72
304*	50254400	F	U5F7715393	9-29-72
307*	51753300	F	U5B771039X	9-29-72
308*	15106100	S	NE531	9-29-72
309*	95817600	RCA	CA3001	9-29-72
315*	15110800	RCA	CA3040	9-29-72
316*	15110900	N	LH0002CH	9-29-72
321S	15115400	TE	TSC4711	12-1-72
350*	50254100	M	MC1463R	9-29-72
351*	50254000	M	MC1469R	9-29-72
380*	50256900	RCA	RCA51258	9-29-72
502	15105400	T	74180	4-10-72
519	15104400	T	74174	12-1-72
521	36188100	T	7483	9-29-72
579	15106400	S	NE562	4-10-72
AMP-1*	11844900	CDC		9-29-72
AMP-2*	40132000	CDC		9-29-72

*Integrated circuit operational amplifiers (op-amps) are not considered field replaceable due to balancing problems and are not included within this section. Refer to Manufacturer's Data Handbook for op-amp circuit information.

**MFGR's
- F = Fairchild Semiconductors
- T = Texas Instruments
- M = Motorola Semiconductor Products, Inc.
- S = Signetics Corporation
- N = National Semiconductor
- TE = Transitron Electronics



LOGIC SYMBOL



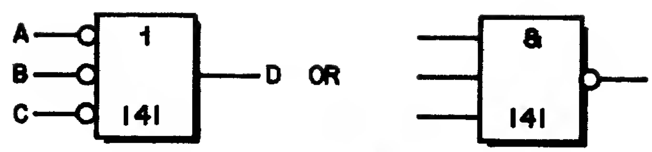
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

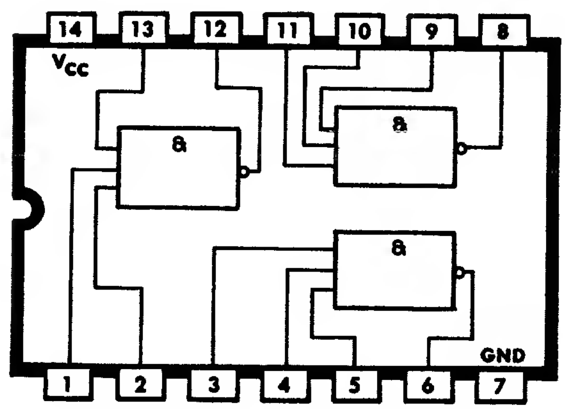
TRUTH TABLE
(FOR ONE GATE)

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 140 manufactured by Fairchild Semiconductors (P/N 9002) used for low speed applications.
4. Type 140S manufactured by Texas Instruments (P/N 74S00) used for high speed applications.



LOGIC SYMBOL



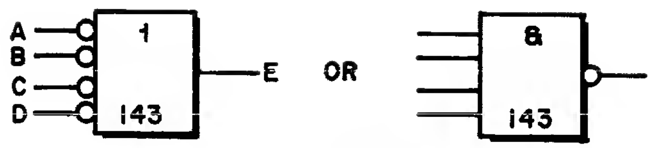
PACKAGE PIN CONFIGURATION

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE
(FOR ONE GATE)

NOTES:

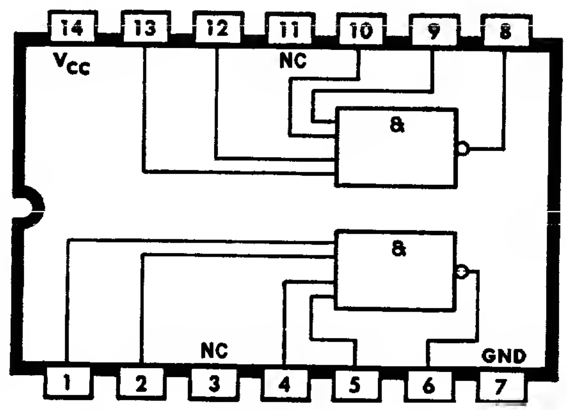
1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 141 manufactured by Fairchild Semiconductors (P/N 9003).



LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

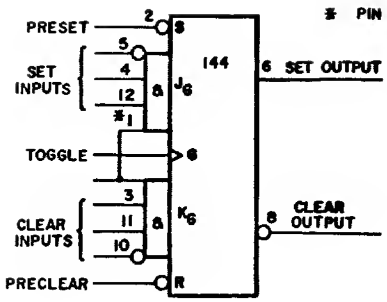
TRUTH TABLE
(FOR ONE GATE)



PACKAGE PIN CONFIGURATION

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 143 manufactured by Fairchild semiconductors (P/N 9009) used for low speed switching applications.
4. Type 143S manufactured by Texas Instruments (P/N 74S40) used for high speed switching applications.



* PIN 1 IS CONNECTED INTERNALLY TO BOTH INPUTS

J – J OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE (G)

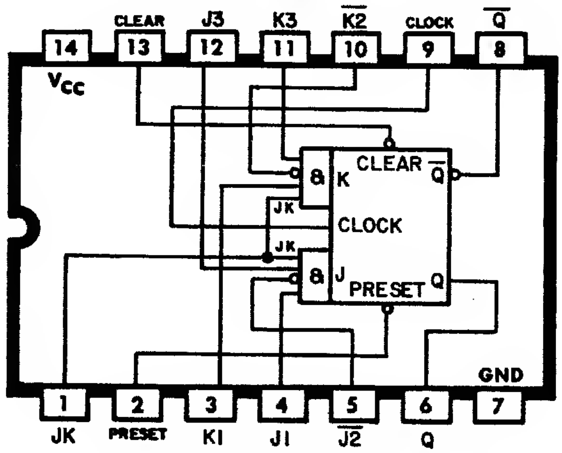
K – K OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE (G)

G – GATE INPUT, HAS NO DIRECT EFFECT ON CIRCUIT, BUT MUST PRESENT BEFORE SIGNALS PRESENT ON INPUT(S) CAN BE TRANSFERRED TO OUTPUT(S)

S – SET INPUT, WHEN "0", FF IS SET REGARDLESS OF INPUTS AND GATE STATES

R – RESET(CLEAR) INPUT. WHEN "0", FF IS CLEARED REGARDLESS OF INPUTS AND GATE STATES

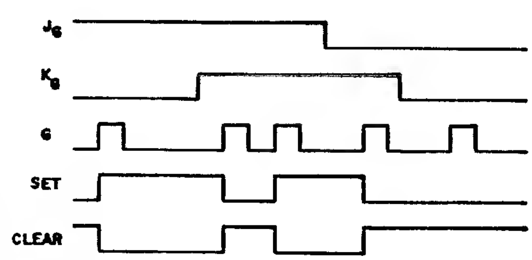
LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

INPUTS		OUTPUTS BEFORE TOGGLE		OUTPUTS AFTER TOGGLE	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

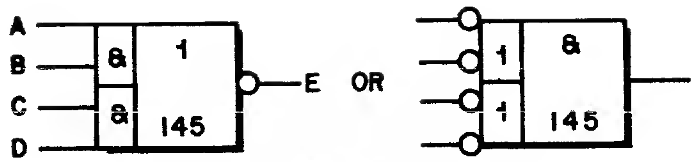
TRUTH TABLE



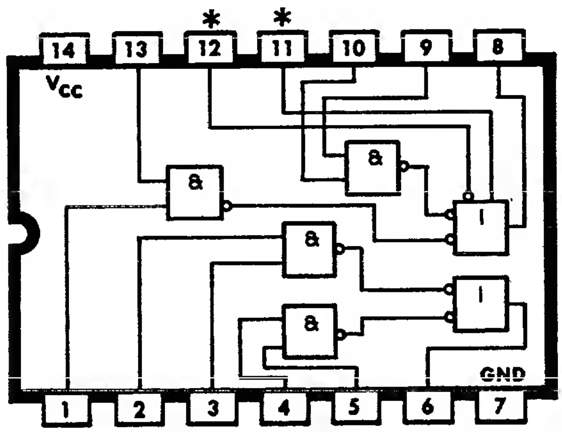
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 144 manufactured by Fairchild Semiconductors (P/N 9001).



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

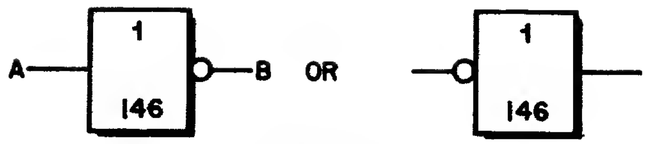
* PINS USED FOR CONNECTING EXTENDERS

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

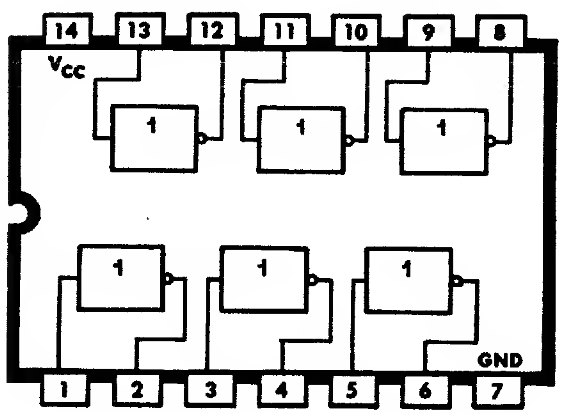
TRUTH TABLE

NOTES:

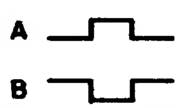
1. Symbol shown as it would appear on logic diagrams.
2. Type 145 manufactured by Fairchild Semiconductors (P/N 9005).



LOGIC SYMBOL



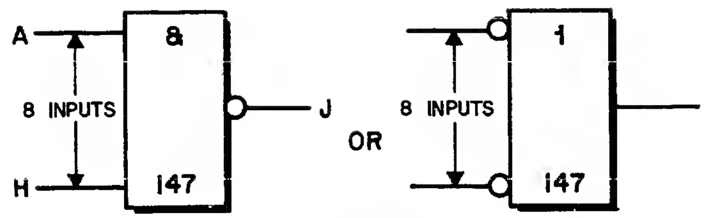
PACKAGE PIN CONFIGURATION



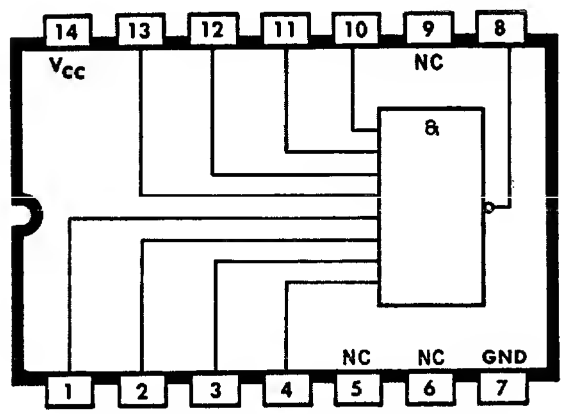
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 146 manufactured by Fairchild Semiconductors (P/N 9016).



LOGIC SYMBOL



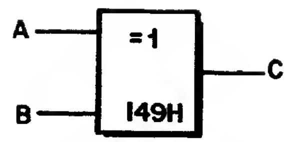
PACKAGE PIN CONFIGURATION

A	B	→ H	J
1	0	→ 0	0
0	1	→ 1	0
0	0	→ 0	1
1	1	→ 1	0

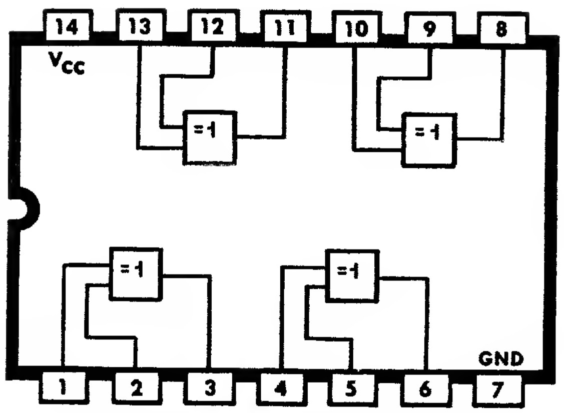
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 147 manufactured by Fairchild Semiconductors (P/N 9007).



LOGIC SYMBOL



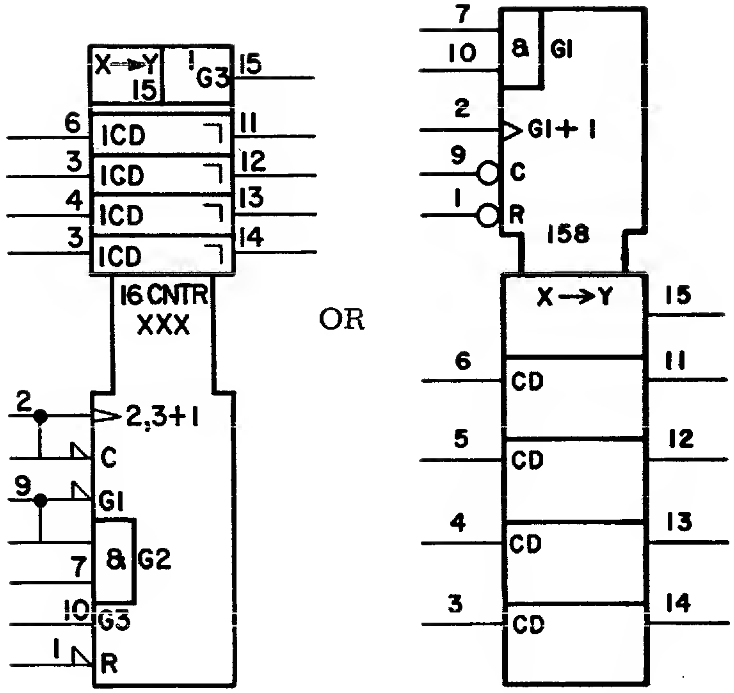
PACKAGE PIN CONFIGURATION

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

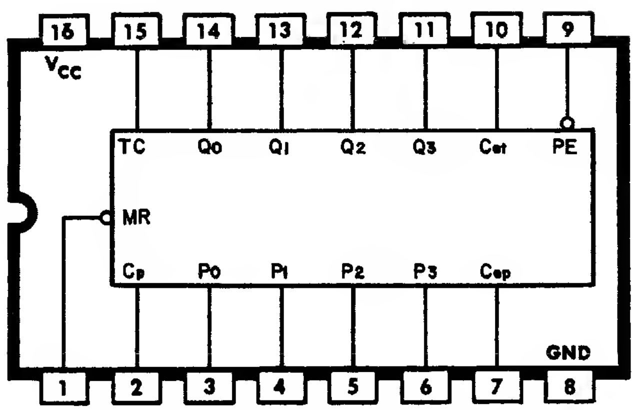
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 149H manufactured by Motorola Semiconductor Products, Inc., (P/N 3021).

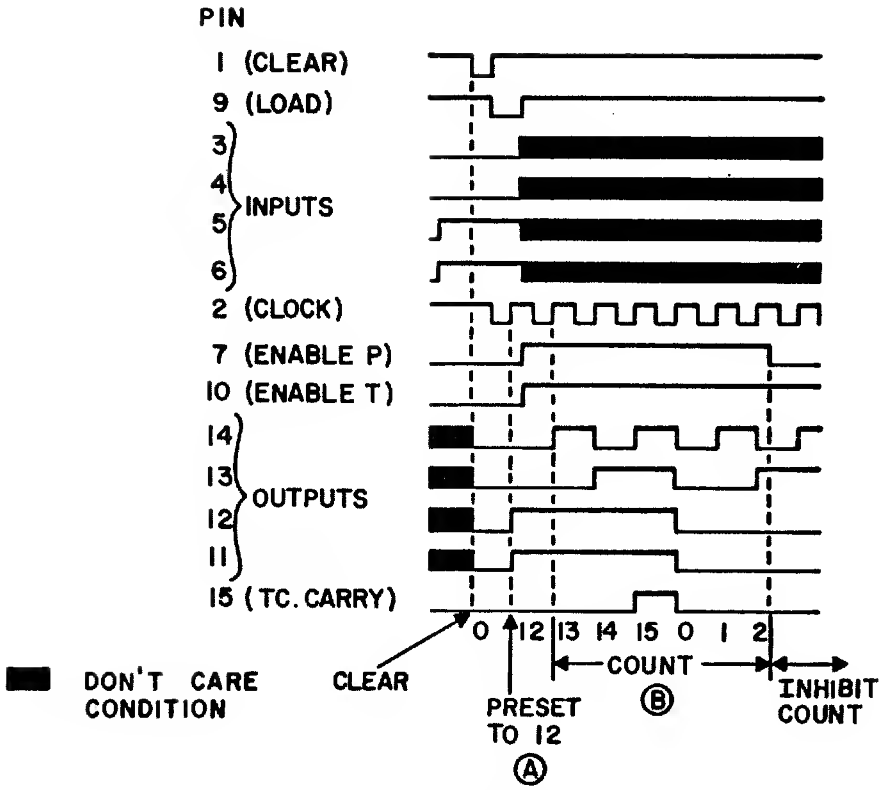


LOGIC SYMBOL



PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

PACKAGE PIN CONFIGURATION



Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7&10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

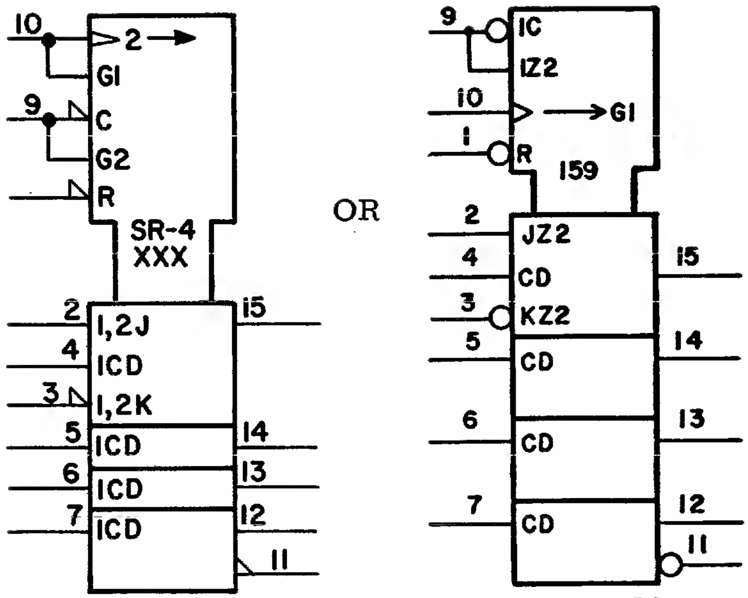
Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

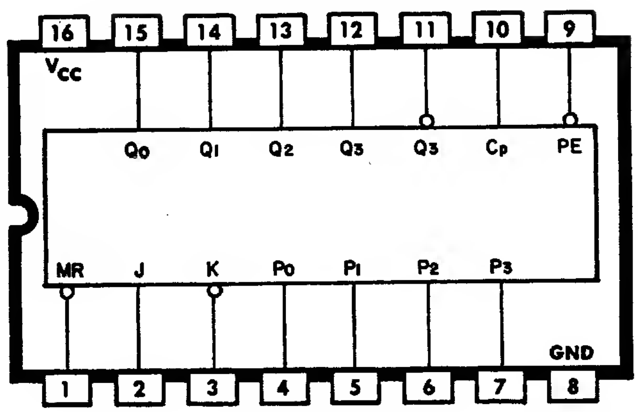
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic drawings.
2. Type 158 manufactured by Fairchild Semiconductors (P/N 9316).

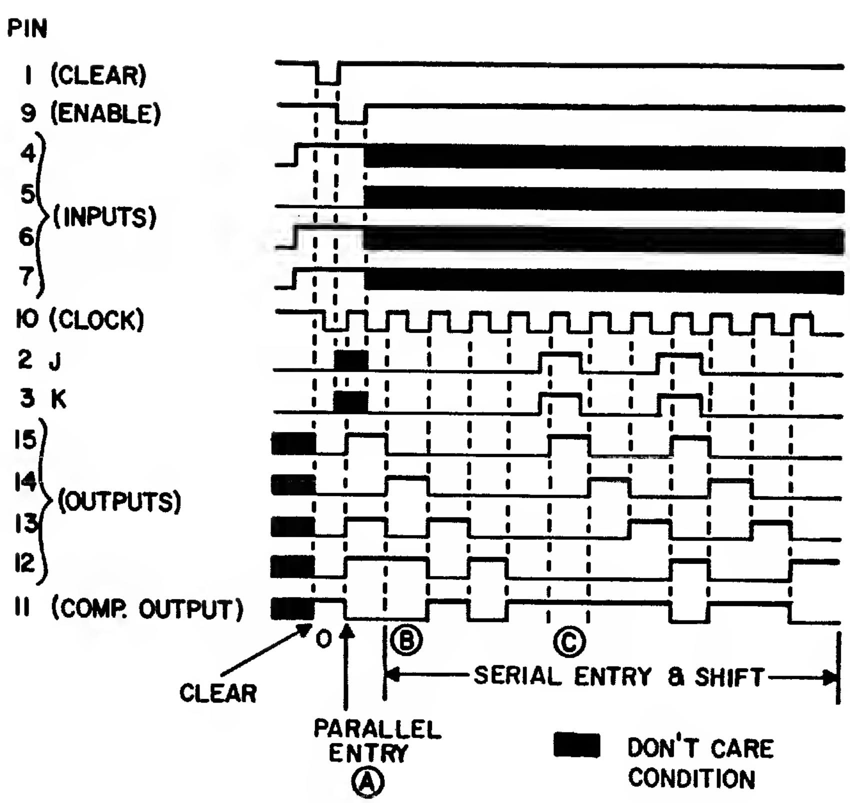


LOGIC SYMBOL



PIN(S)	FUNCTION	
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)	
2	FIRST STAGE J (ACTIVE HIGH) INPUT	SERIAL INPUTS
3	FIRST STAGE K (ACTIVE LOW) INPUT	
4, 5, 6, 7	PARALLEL INPUTS	
9	PARALLEL ENABLE (ACTIVE LOW) INPUT (SHIFT/LOAD)	
10	CLOCK (ACTIVE HIGH GOING EDGE) INPUT	
11	COMPLEMENTARY LAST STAGE OUTPUT	
12, 13, 14, 15	PARALLEL OUTPUTS	

PACKAGE PIN CONFIGURATION



NOTES:

Ⓐ DATA ENTERED INTO D-INPUT VIA PIN 4 BY PIN 9 LOW AND POSITIVE-GOING SIGNAL ON PIN 10.

Ⓑ DATA ENTERED INTO JK(Z) INPUT BY PIN 9 HIGH AND POSITIVE-GOING SIGNAL ON PIN 10. PIN 4 INPUT INHIBITED BECAUSE OF PIN 9 HIGH. OUT IS THEN AS FOLLOWS:

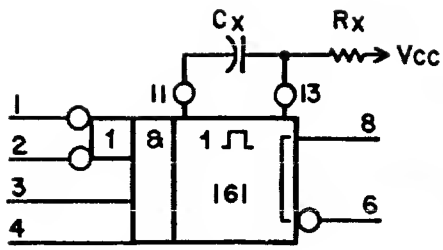
INPUT PIN		OUTPUT PIN
2	3	15
0	0	0
0	1	NO CHANGE
1	0	TOGGLES
1	1	1

Ⓒ DATA SHIFTS DOWN (PIN 15 — 14, ETC.) WITH CLOCK.

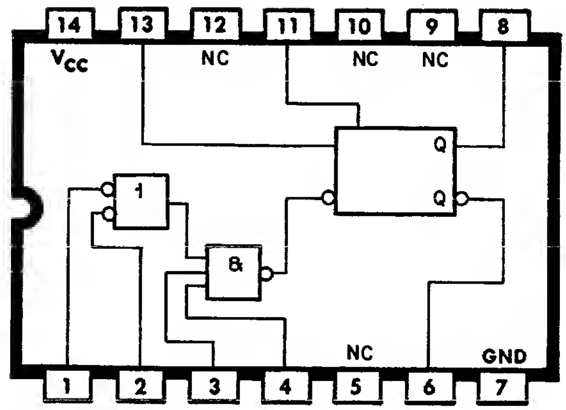
TIMING SEQUENCE

NOTES:

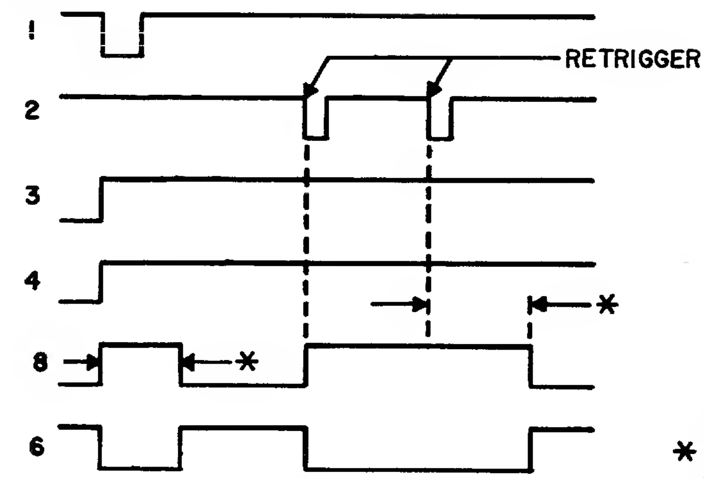
1. Symbol shown as it would appear on logic diagrams.
2. Type 159 manufactured by Fairchild Semiconductors, (P/N 9300).



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

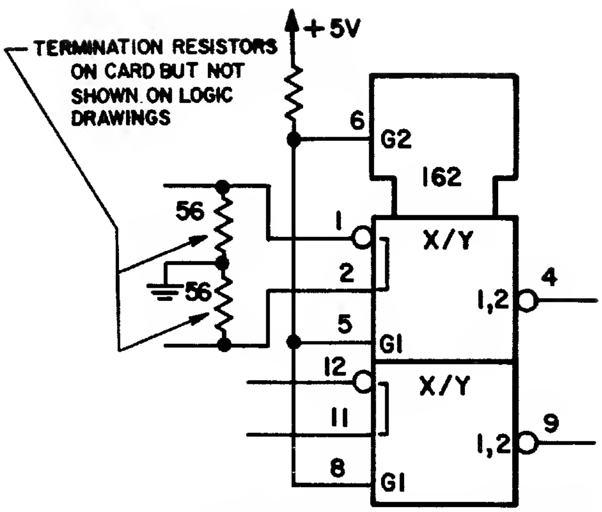


TIMING SEQUENCE

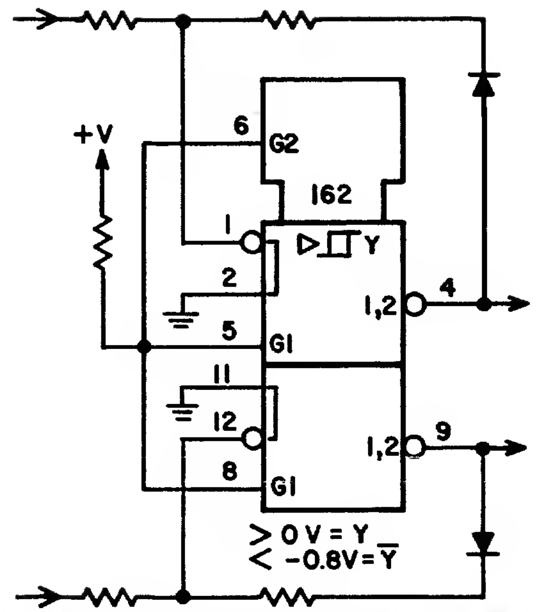
* PULSE WIDTH DETERMINED BY RC TIMING NETWORK

NOTES:

1. Symbol shown as it would appear on logic diagrams, except for timing network.
2. Type 161 manufactured by Fairchild Semiconductors (P/N 9601).

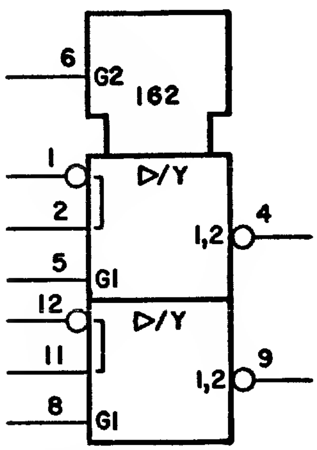


TWISTED PAIR RECEIVER APPLICATION

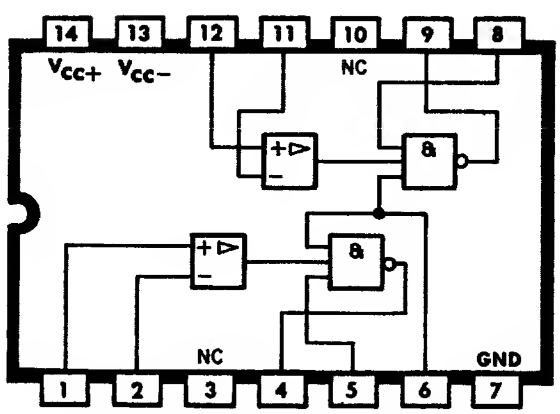


162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS.

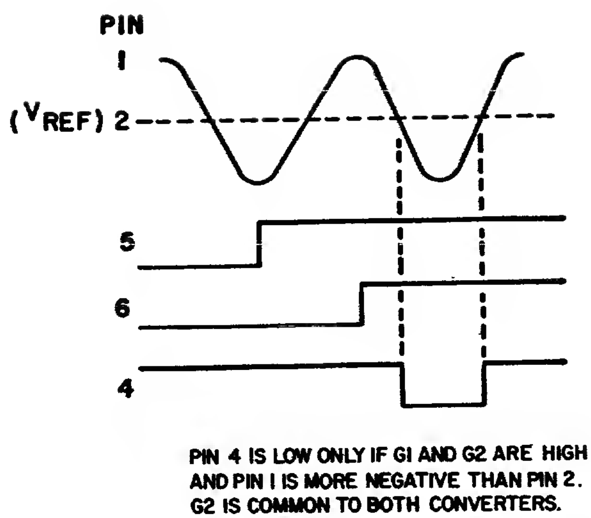
LOGIC SYMBOL



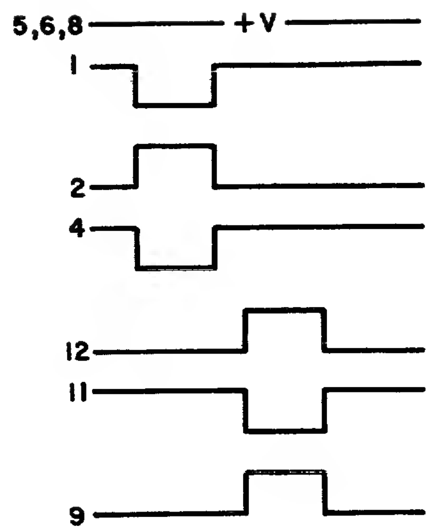
ANALOG TO DIGITAL CONVERTER APPLICATION



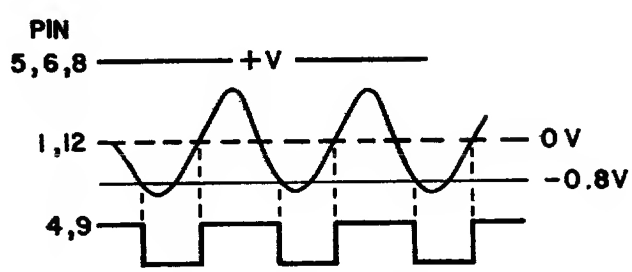
PACKAGE PIN CONFIGURATION



162 DIGITAL TO ANALOG CONVERTER APPLICATION



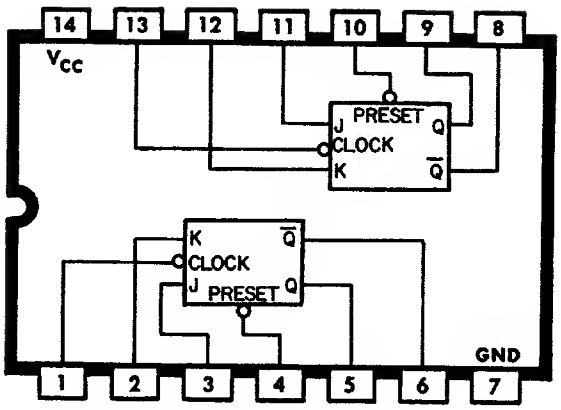
162 TWISTED PAIR RECEIVER APPLICATION



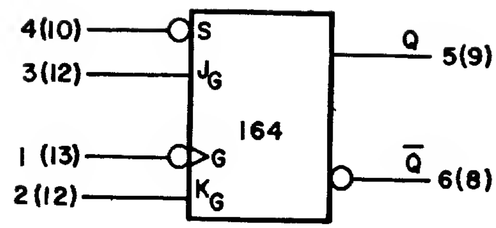
162 SCHMITT TRIGGER

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 162 manufactured by Texas Instruments (P/N 75107).



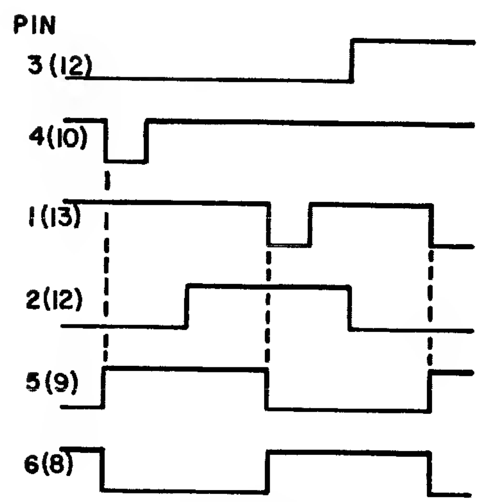
PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

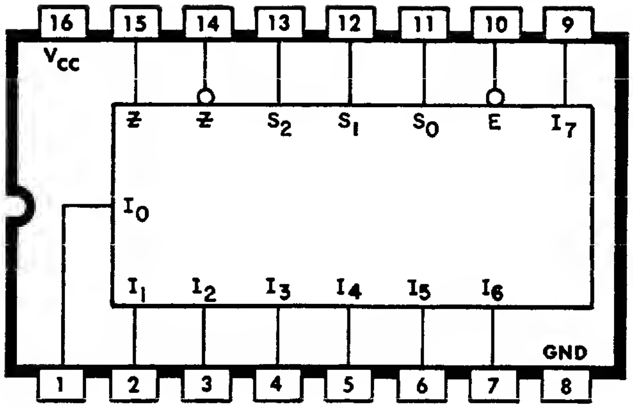
TRUTH TABLE



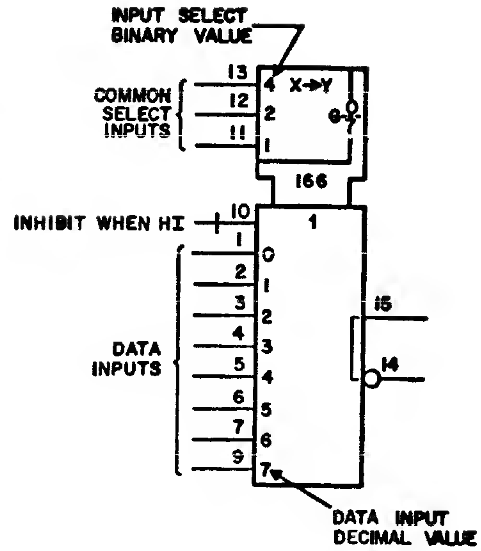
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 164H manufactured by Motorola Semiconductor Products, Inc., (P/N 3062) used for low speed applications.
4. Type 164S manufactured by Texas Instruments (P/N 74S113) used for high speed applications.



PACKAGE PIN CONFIGURATION

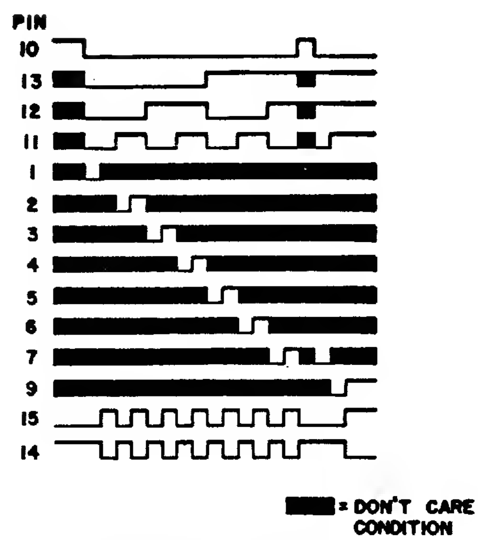


LOGIC SYMBOL

COMMON SELECT PIN			INPUT PIN GATED TO OUTPUT PIN 15 * (PIN 10 LOW)
13	12	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	9

* 1.) OUTPUT IS HIGH IF DATA INPUT IS HIGH.
2.) OUTPUT IS LOW IF DATA INPUT IS LOW.
3.) PIN 14 OUTPUT IS INVERSE OF PIN 15.
4.) IF PIN 10 IS HIGH, PIN 15 IS LOW AND 14 IS HIGH (REGARDLESS OF SELECT/DATA INPUTS).

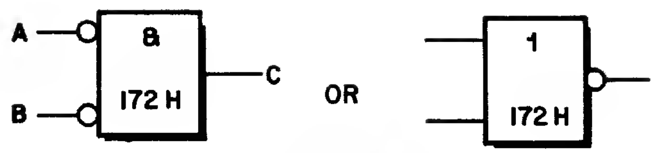
TRUTH TABLE



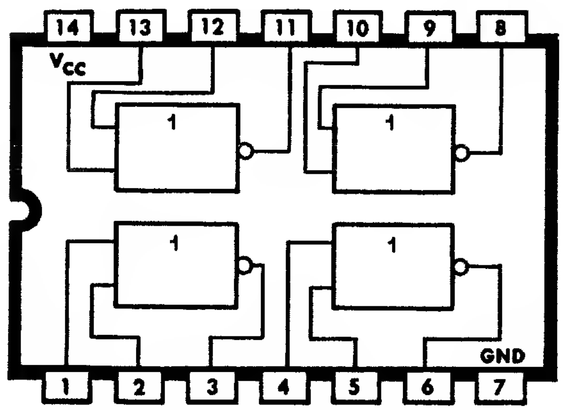
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 166 manufactured by Fairchild Semiconductors (P/N 9312).



LOGIC SYMBOL



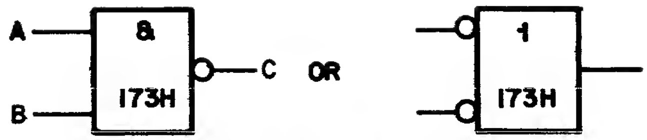
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

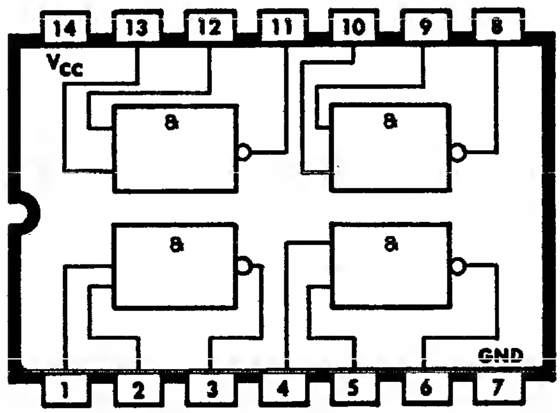
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 172H manufactured by Motorola Semiconductor Products, Inc., (P/N 3002).



LOGIC SYMBOL



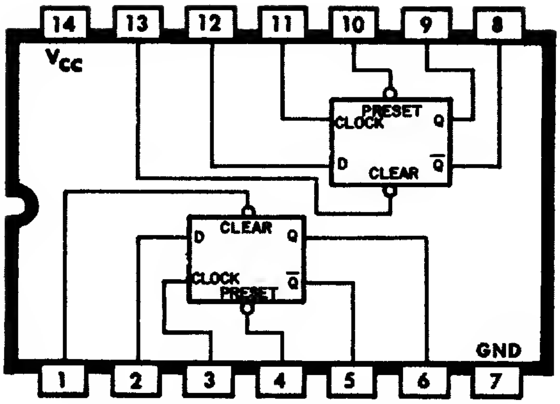
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

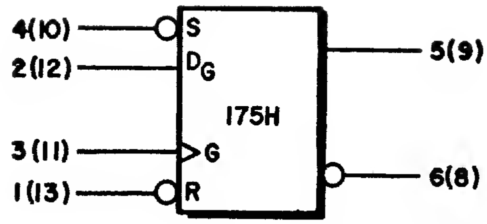
TRUTH TABLE

NOTES:

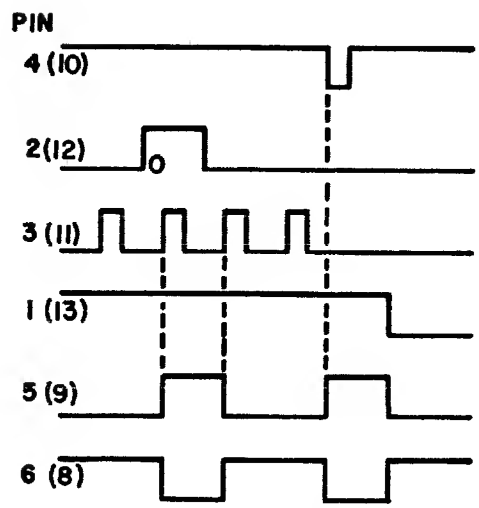
1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 173H manufactured by Motorola Semiconductor Products, Inc., (P/N 3004).
4. The output of each gate is an open collector.



PACKAGE PIN CONFIGURATION



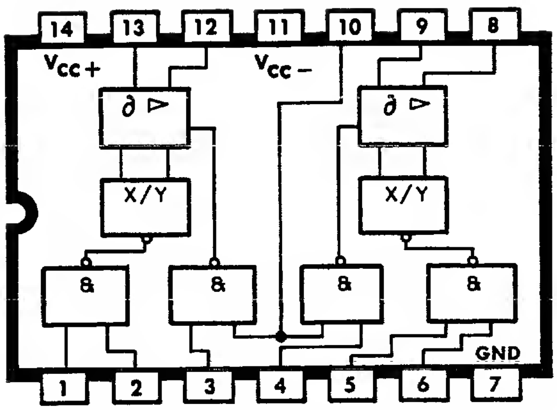
LOGIC SYMBOL



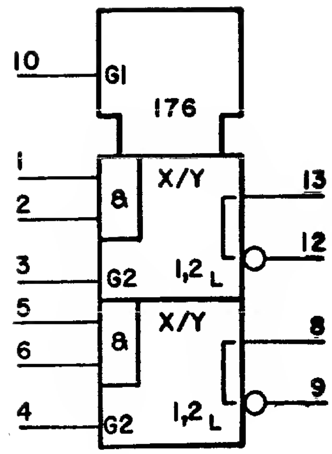
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 175H manufactured by Motorola Semiconductor Products, Inc., (P/N 3060).



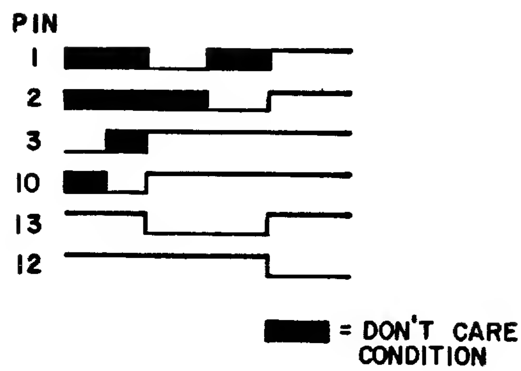
PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
1	2	3	10	12	13
1 or 0	1 or 0	1	1 or 0	1	1
1 or 0	1 or 0	1 or 0	0	1	1
0	1 or 0	1	1	0	1
1 or 0	0	1	1	0	1
1	1	1	1	1	0

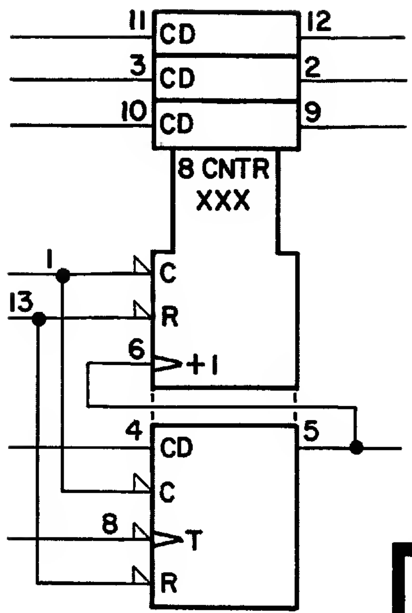
TRUTH TABLE



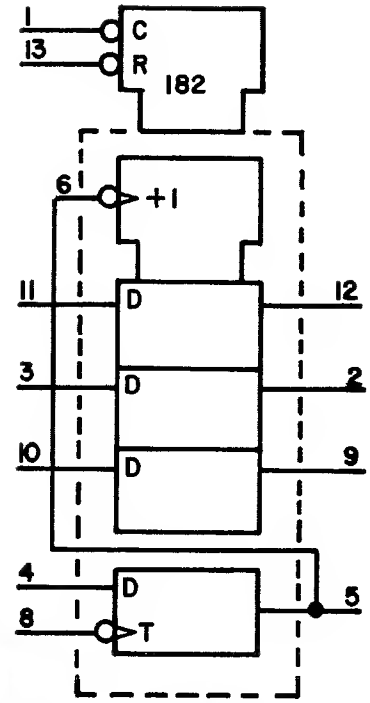
TIMING SEQUENCE

NOTES:

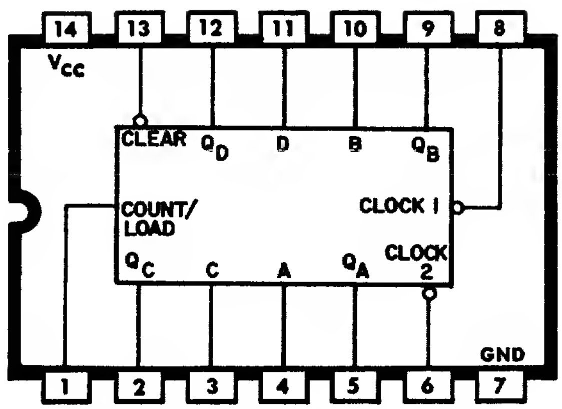
1. Symbol shown as it would appear on logic diagrams.
2. Type 176 manufactured by Texas Instruments (P/N 75110).



OR



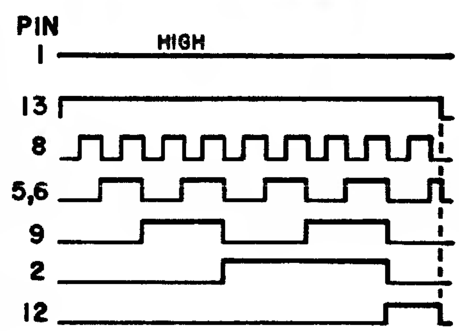
LOGIC SYMBOL



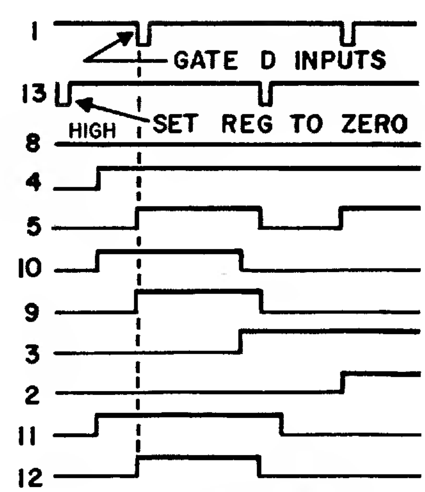
PACKAGE PIN CONFIGURATION

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TRUTH TABLE



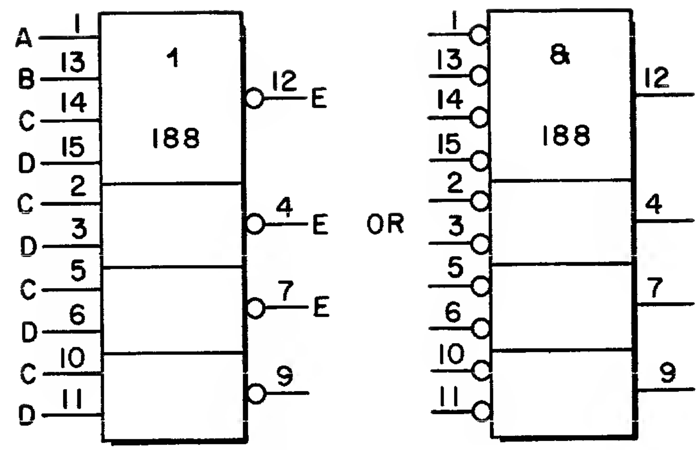
COUNTER APPLICATION



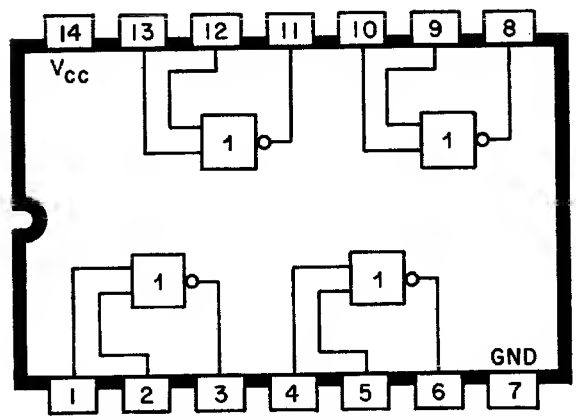
REGISTER APPLICATION

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 182 manufactured by Texas Instruments (P/N 74197) or Signetics Corporation (P/N 8291).



LOGIC SYMBOL



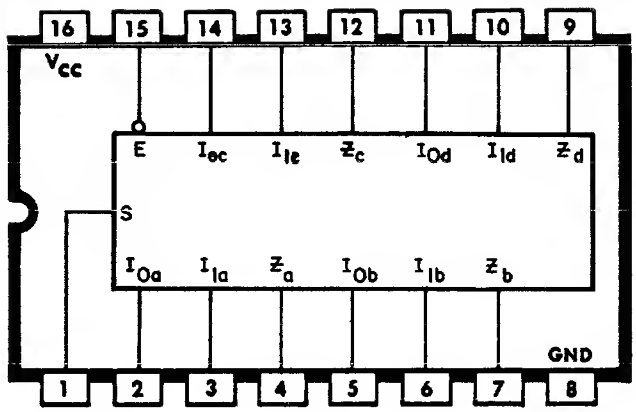
PACKAGE PIN CONFIGURATION

A	B	C	D	E
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE

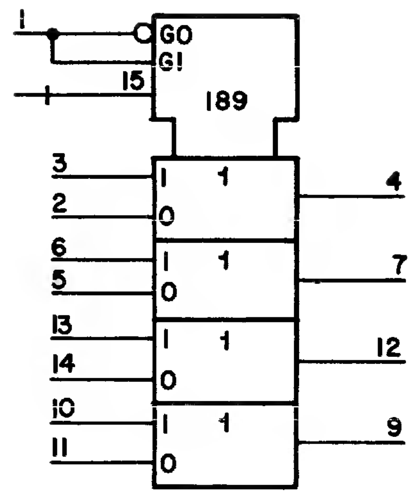
NOTES:

1. Symbol shown as it would appear on logic diagram.
2. Type 188 manufactured by Fairchild Semiconductor (P/N 9015).



PIN	FUNCTION
1	COMMON SELECT INPUT
15	ENABLE (ACTIVE LOW) INPUT
2,3,5,6,10,11,13,14	MULTIPLEXER INPUTS (a,b,c,d)
4,7,9,12	MULTIPLEXER OUTPUTS (a,b,c,d)

PACKAGE PIN CONFIGURATION



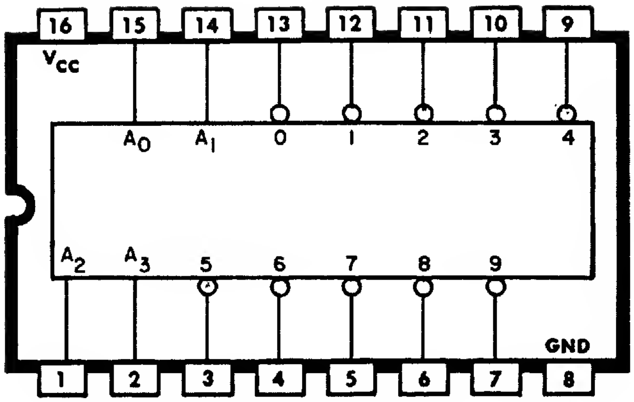
LOGIC SYMBOL

15	1	3,6,13,10	2,5,14,11	4,7,12,9
1	*	*	*	*
0	0	*	1	1
0	0	*	0	0
0	1	1	*	1
0	1	0	*	0
* = NO EFFECT ON OUTPUT				

TRUTH TABLE

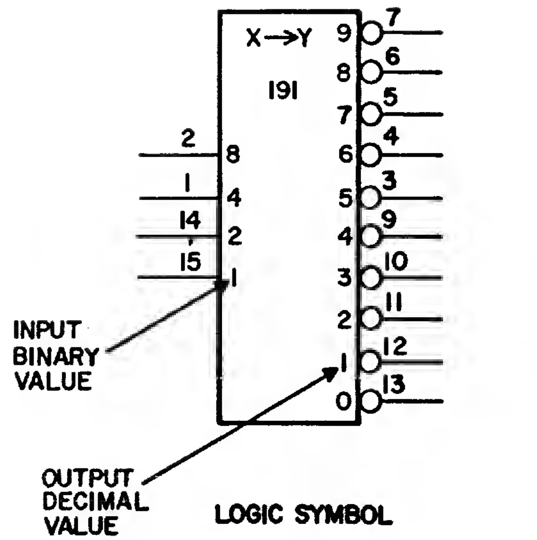
NOTES:

1. Symbol shown as it would appear on logic diagram.
2. Type 189 manufactured by Fairchild Semiconductors (P/N 9322).



PIN	FUNCTION
1,2,14,15	ADDRESS INPUTS
3–7,9–13	OUTPUTS (ACTIVE LOW)

PACKAGE PIN CONFIGURATION

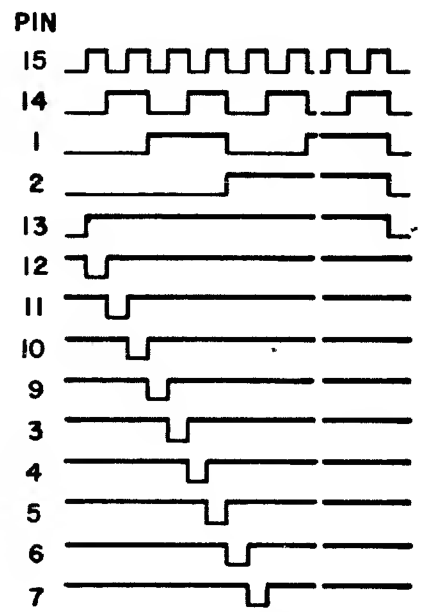


LOGIC SYMBOL

INPUT PIN 2	INPUT PIN 1	INPUT PIN 14	INPUT PIN 15	LO("0") OUTPUT PIN (OTHER OUTPUTS = "1")
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	*

* ALL OUTPUTS ARE HIGH

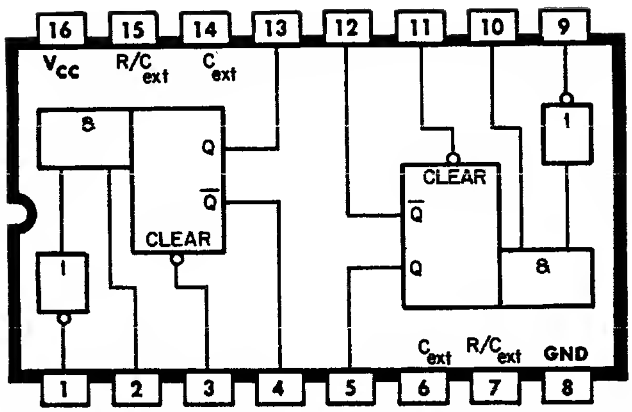
TRUTH TABLE



TIMING SEQUENCE

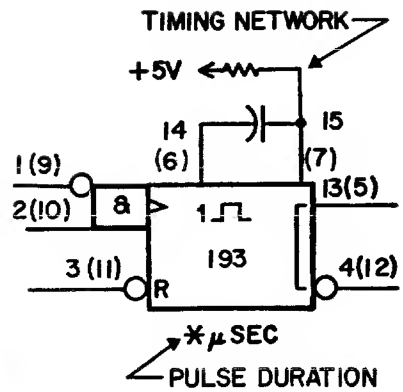
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 191 manufactured by Fairchild Semiconductors (P/N 9301).

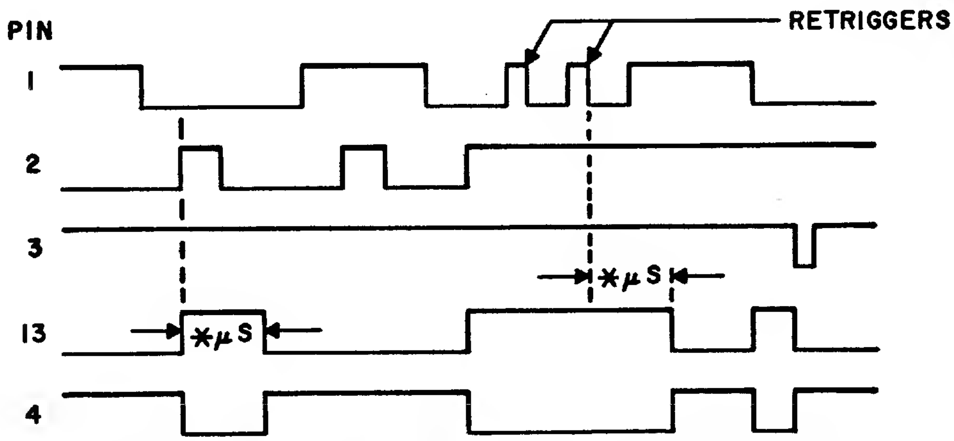


PINS 6,7,14,15 ARE USED FOR EXTERNAL TIMING NETWORK

PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

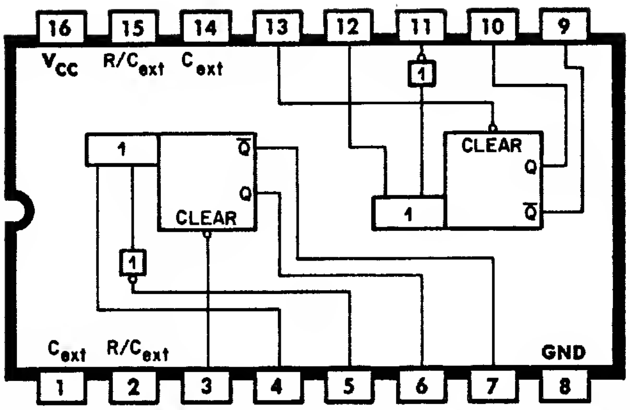


* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK

TIMING SEQUENCE

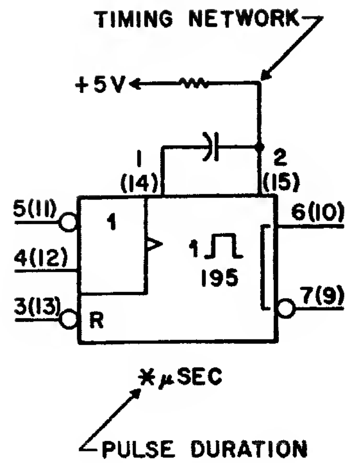
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 193 manufactured by Texas Instruments (P/N 74123).

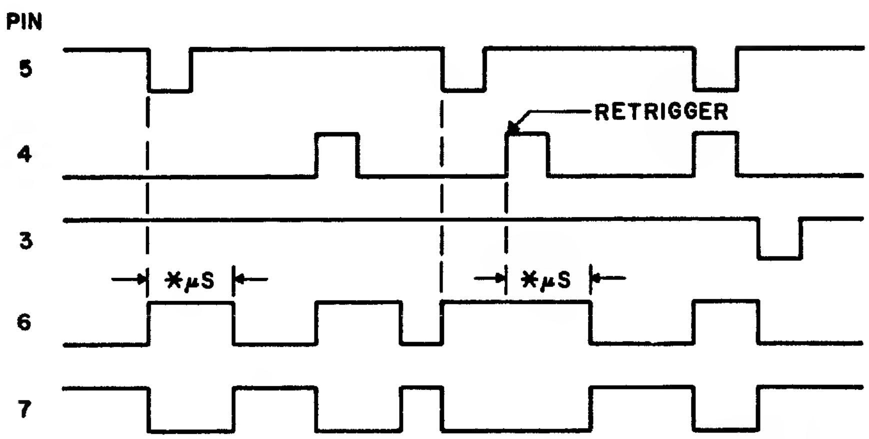


PINS 1, 2, 14, 15 ARE USED FOR EXTERNAL TIMING NETWORK

PACKAGE PIN CONFIGURATION



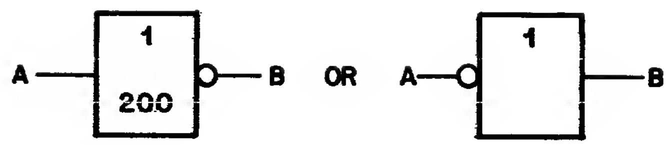
LOGIC SYMBOL



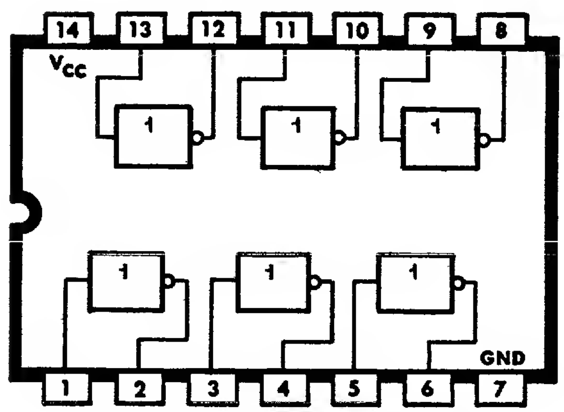
* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK

TIMING SEQUENCE

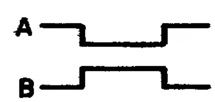
NOTES:
1. Symbol shown as it would appear on logic diagrams.
2. Type 195 manufactured by Fairchild Semiconductors (P/N 9602).



LOGIC SYMBOL



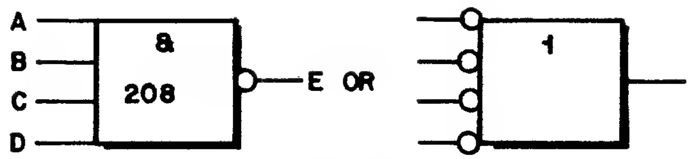
PACKAGE PIN CONFIGURATION



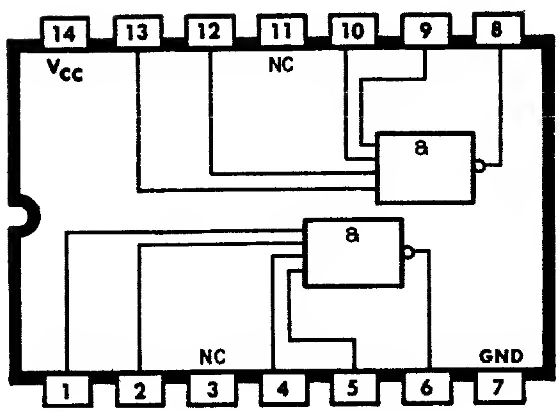
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 200 manufactured by Texas Instruments (P/N 7406).
4. The output of each gate is an open collector.



LOGIC SYMBOL



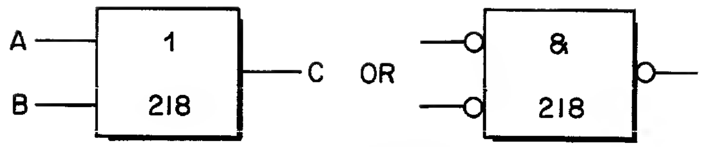
PACKAGE PIN CONFIGURATION

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

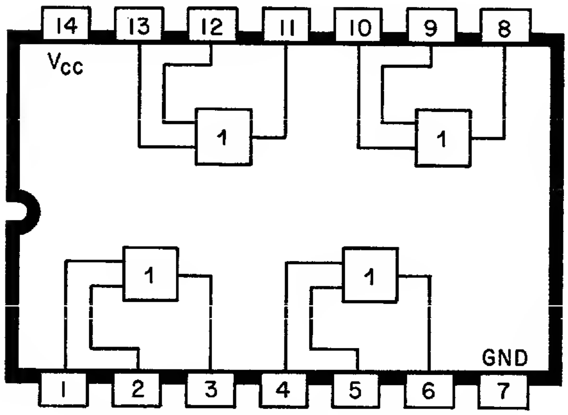
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each NAND gate.
3. Type 208S manufactured by Texas Instruments (P/N 74S20).



LOGIC SYMBOL



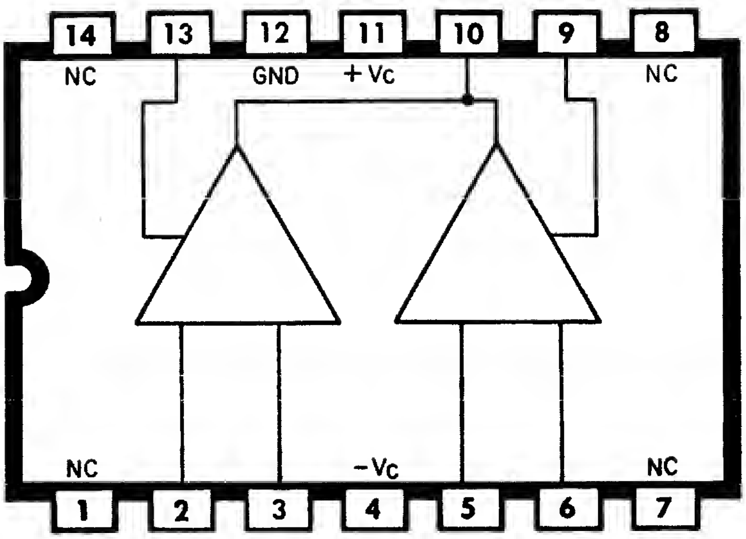
PACKAGE PIN CONFIGURATION

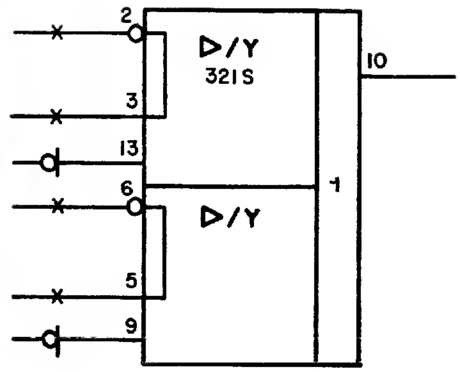
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

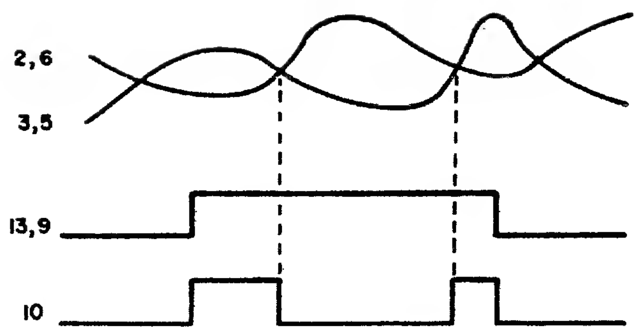
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagram.
2. Type 218 manufactured by Motorola Semiconductor (P/N 3003).

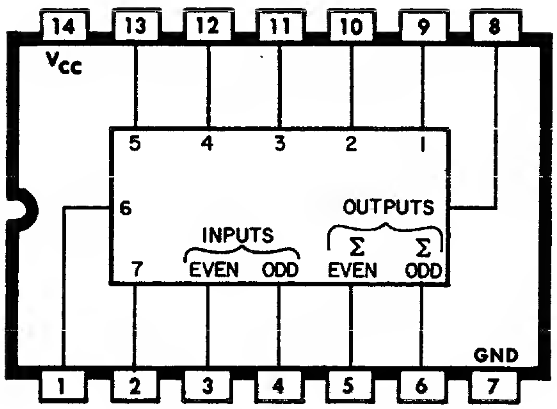




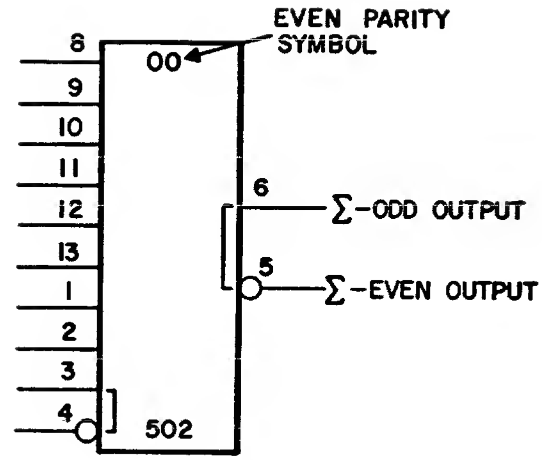


The 321S is a dual comparator. Output (pin 10) is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high.

NOTES:
1. Symbol shown as it would appear on logic diagrams.
2. Type 321S manufactured by Transitron Electron (P/N TSC5711).



PACKAGE PIN CONFIGURATION



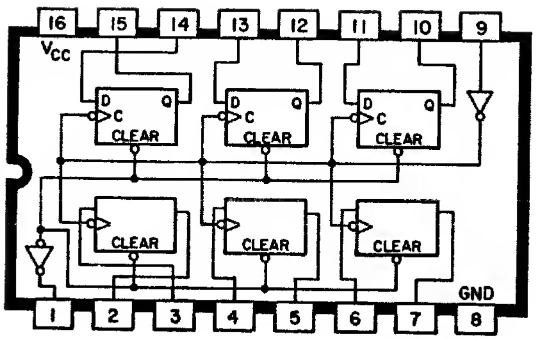
LOGIC SYMBOL

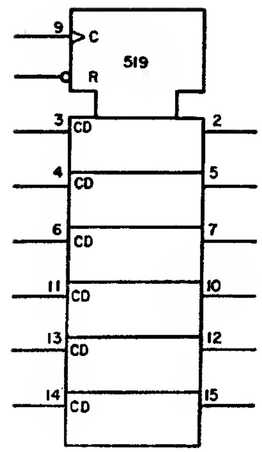
INPUTS			OUTPUTS	
Σ OF 1's AT PINS 1,2,8 THRU 13	PIN 3	PIN 4	PIN 5	PIN 6
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
EVEN OR ODD	1	1	0	0
EVEN OR ODD	0	0	1	1

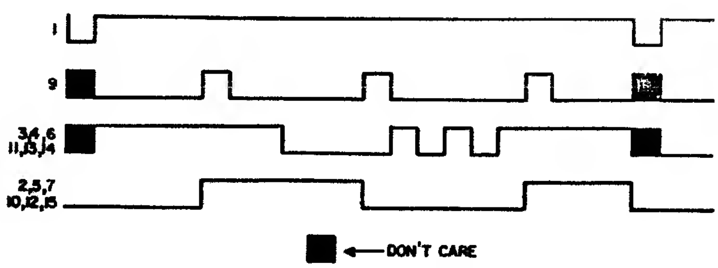
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 502 manufactured by Texas Instruments (P/N 74180).



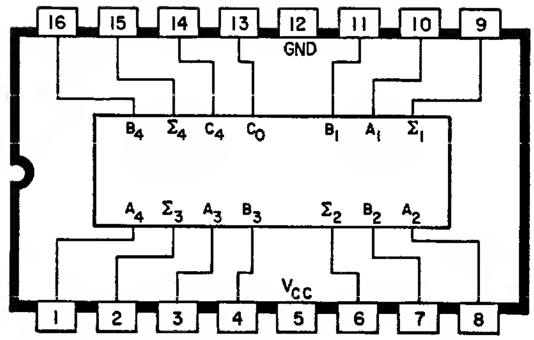


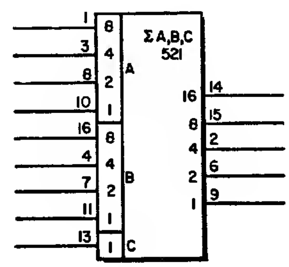


NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 519 manufactured by Texas Instruments (P/N 74174).

INPUT				OUTPUT					
				WHEN $C_0=0$ / WHEN $C_2=0$			WHEN $C_0=1$ / WHEN $C_2=1$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4
0	0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
0	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	0	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1



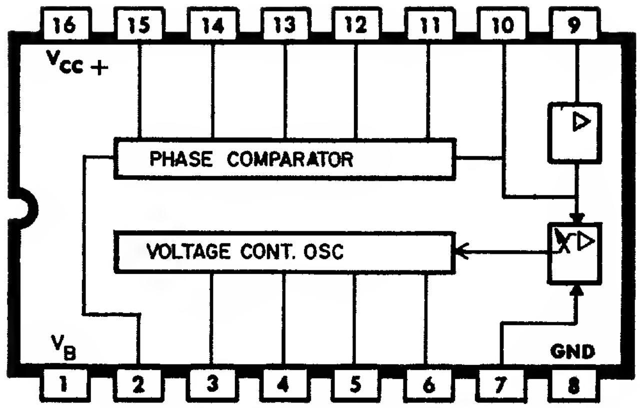


The 521 circuit type is a 4-bit binary full adder. A is added to B with C (a carry) added in at the least significant digit.

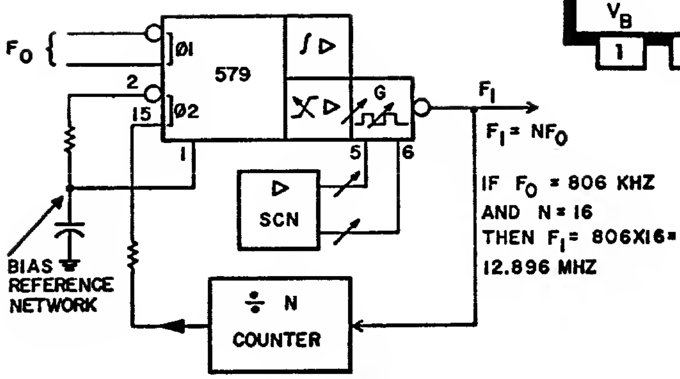
Input conditions at A_1, B_1, A_2, B_2, and C_0 are used to determine outputs E_1, E_2, and the value of an internal carry C_2 (not shown). The values at C_2, A_3, B_3, A_4, and B_4 are then used to determine outputs E_3, E_4, and C_4.

NOTES:

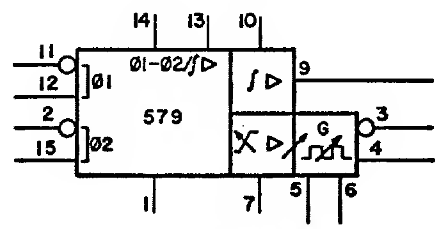
1. Symbol shown as it would appear on logic diagrams.
2. Type 521 manufactured by Tecas Instruments (P/N 7483).



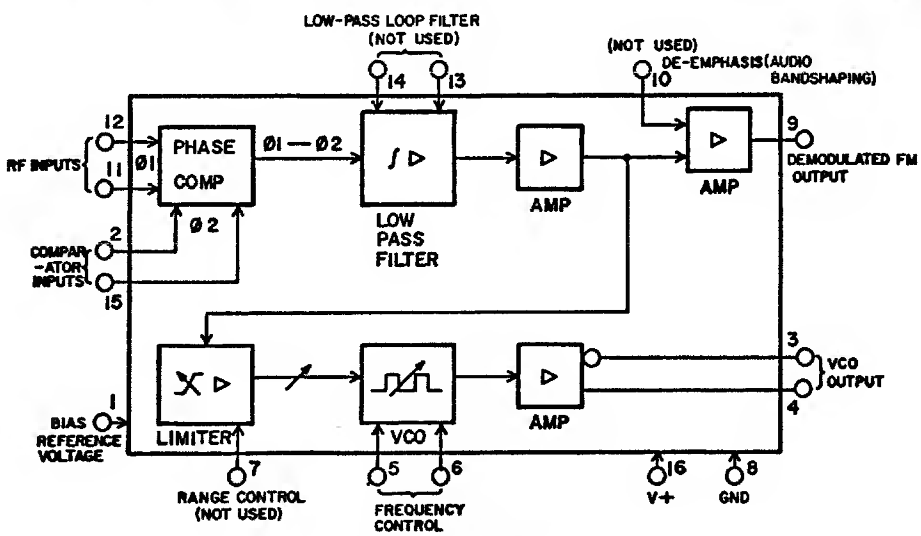
PACKAGE PIN CONFIGURATION



APPLICATION



LOGIC SYMBOL



BLOCK DIAGRAM

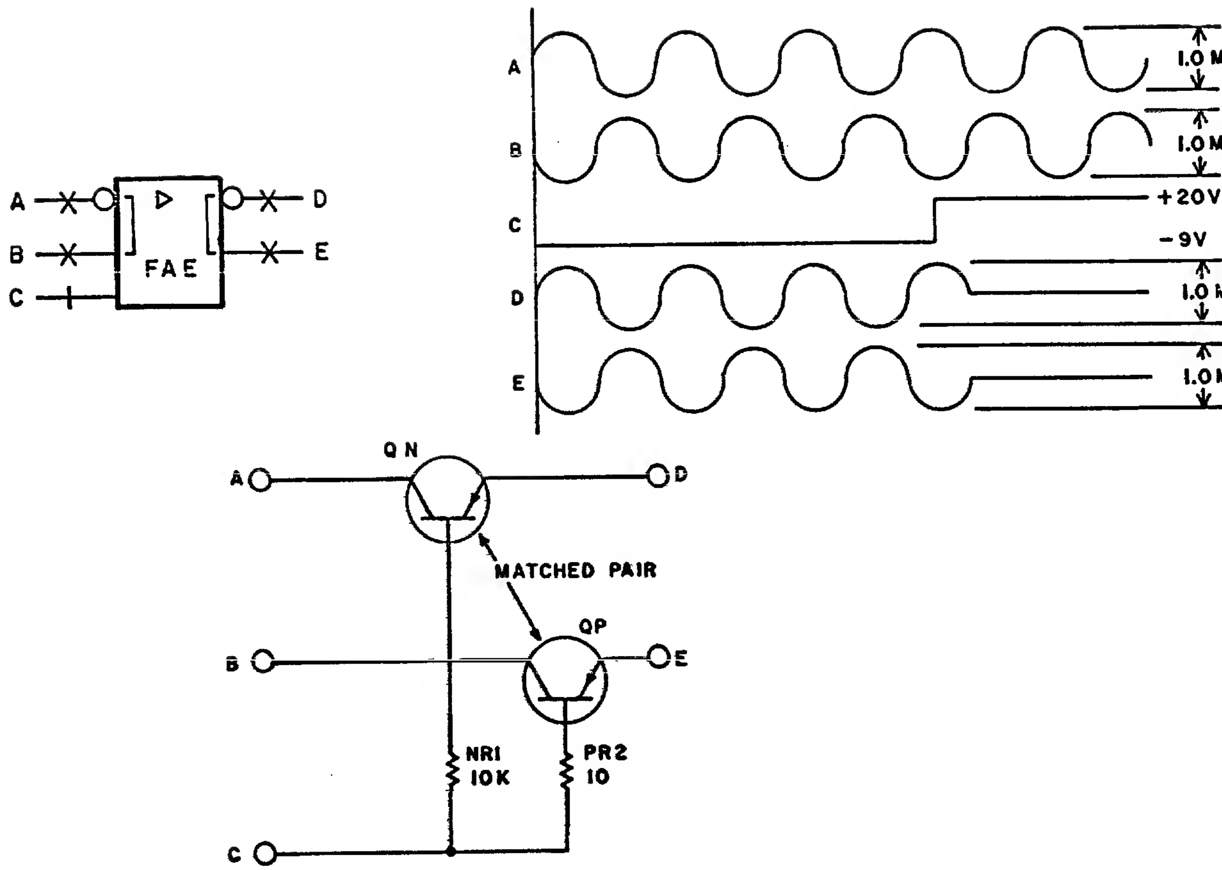
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 579 manufactured by Signetics Corporation (P/N NE562).

SECTION 3

DISCRETE COMPONENT CIRCUIT DESCRIPTIONS

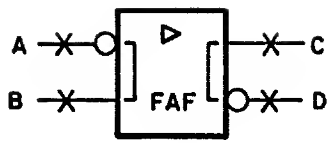
DISCRETE CIRCUIT EFFECTIVITY INDEX					
Circuit Type	Revision Date	Circuit Type	Revision Date	Circuit Type	Revision Date
FAE	3-6-72	HBI	10-13-72	SCC	6-1-72
FAF	3-6-72	HBJ	10-13-72	SCD	3-6-72
FAG	4-20-72	HCA	3-6-72	SCE	4-20-72
FAH	9-29-72	HCB	3-6-72	SCG	6-12-72
FBH	9-29-72	HCE	3-6-72	SCL	6-12-72
GJB	3-6-72	HCF	3-6-72	SCM	3-6-72
GJC	3-6-72	HCK	3-6-72	SCN	3-6-72
GJF	3-6-72	HCL	3-6-72	UBD/E/F/H	9-29-72
GJK	6-1-72	HCP	3-6-72	UBG	3-6-72
GKA/GKB	3-6-72	HCQ	3-6-72	UC-	3-20-73
GKC	3-6-72	HCU	6-12-72	UEB	3-20-73
GKD	3-6-72	HJD	3-6-72	VAF	3-6-72
GKF	3-6-72	HJE	3-6-72	VHI	3-6-72
HAK	9-29-72	ICB	3-6-72	VHJ	3-6-72
HAL/HAM	3-6-72	ICC	3-6-72	VHK	3-6-72
HAN	3-6-72	JAG	9-29-72	VHL	4-20-72
HAP	4-20-72	JAK	9-29-72	VHM	3-6-72
HAQ	4-20-72	JAM	9-24-73	VHP	3-6-72
HAR	6-12-72	LCF	3-6-72	VHQ	3-6-72
HAS/HAT	3-6-72	MAF/MAH	6-1-72	VHR	3-6-72
HAU	3-6-72	QDE	3-6-72	VKK	3-20-73
HAV	3-6-72	QEH	3-6-72	VKN	3-6-72
HAW	3-6-72	QEJ	3-6-72	VKM	3-6-72
HAX	9-29-72	QEK	3-6-72	XAF	6-12-72
HBA	9-29-72	QEL	3-6-72	XAG	3-6-72
HBB	9-29-72	QEM	9-29-72	XAH	3-6-72
HBD	6-12-72	QGD	3-6-72		
HBE	9-29-72	RCB	3-6-72		
		SAA	12-1-72		

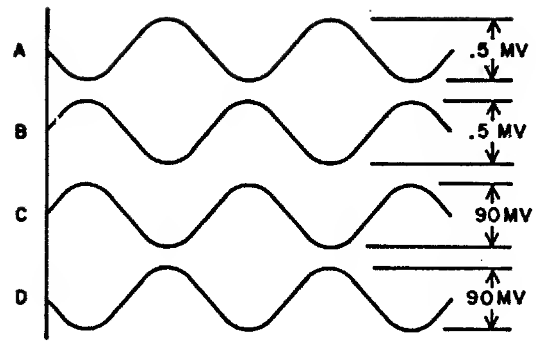


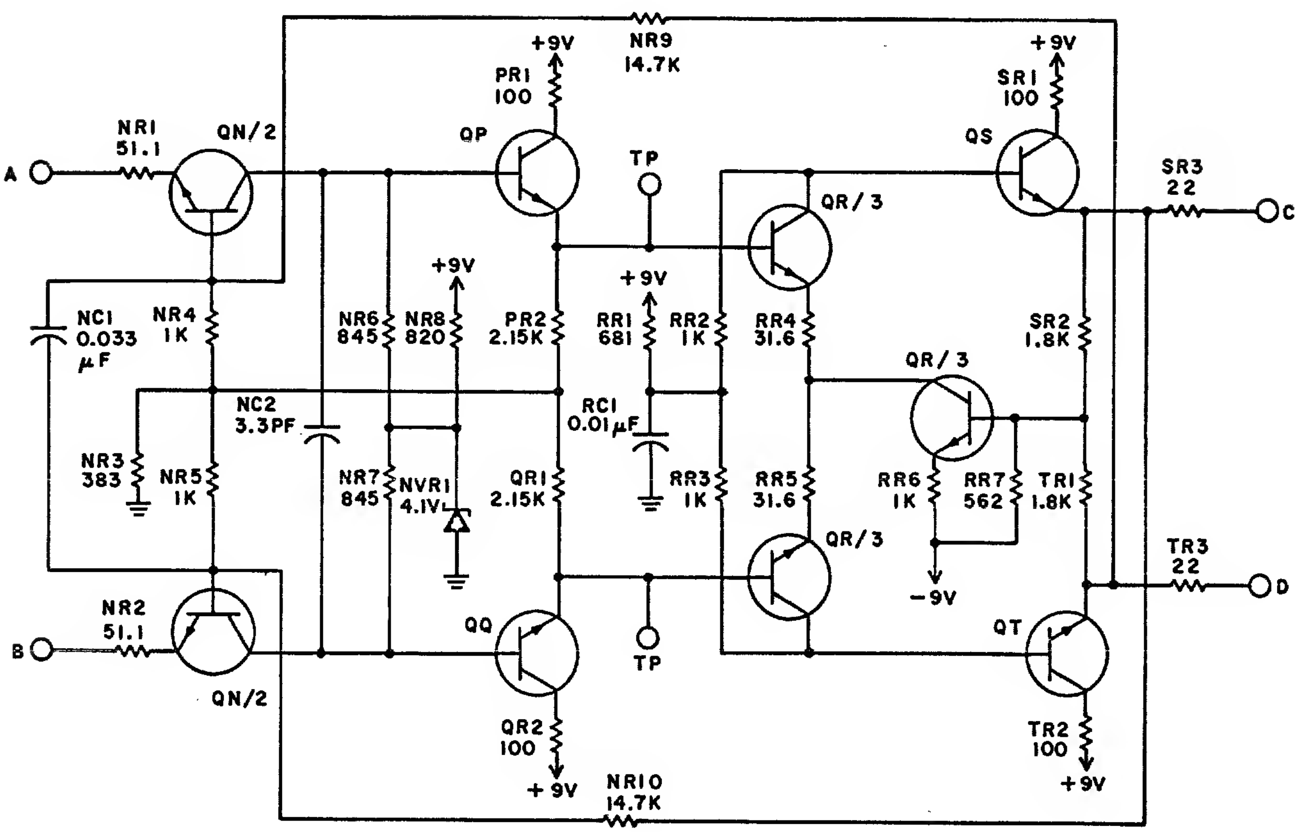
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J10

GATED AMPLIFIER - FAE

The FAE circuit consists of two matched transistors acting as low level analog gates. Inputs A and B receive the output of differential windings of a read head. Output points D and E drive the input of a low level amplifier such as an FAF. The outputs are gated by input C. When point C is at -9 volts, QN and QP turn on enabling data to flow from points A and B to ~~C~~ E and D respectively. At +20 volts on point C QN and OP turn off inhibiting the output.







NOTE:

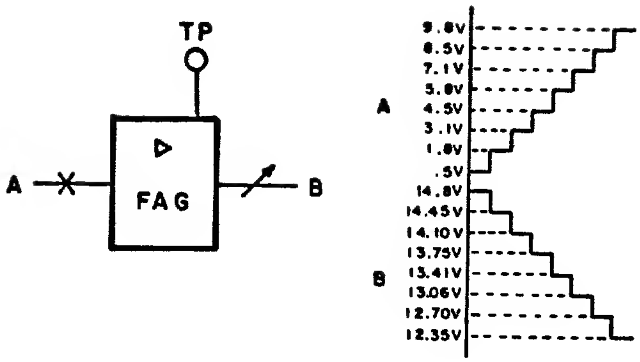
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J11

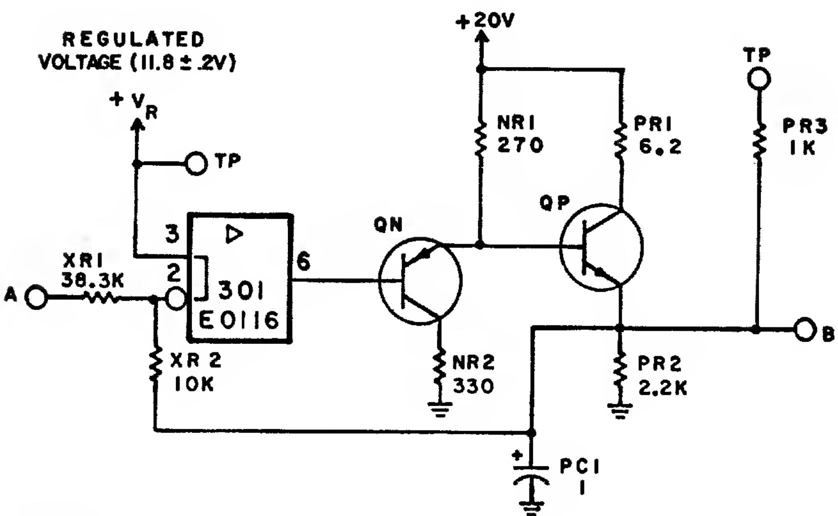
AMPLIFIER - FAF

The FAF circuit is a low level amplifier that amplifies analog read signals. Points A and B are typically connected to Gated Amplifiers which provides biasing for the common base input stage.

The amplifier consists of two stages, common base first stage (QN matched pair) and common emitter second stage (QR matched pair) with emitter follower outputs (QS and QT) for low output impedance. The gain of the first stage is dependent upon the signal source resistance and is approximately 9 with 9750 type heads as a signal source. The gain of the second stage is approximately 20, therefore, the overall amplifier gain is approximately 180.

DC feedback is provided by NR9, NR10, PR2 and QR1 to the base circuitry of the QN matched pair. This feedback helps to stabilize the DC operating points in the circuit. Capacitor NC1 provides a lower impedance path between bases of the input transistors which presents a low amplifier input impedance for AC signals over the passband of the amplifier.





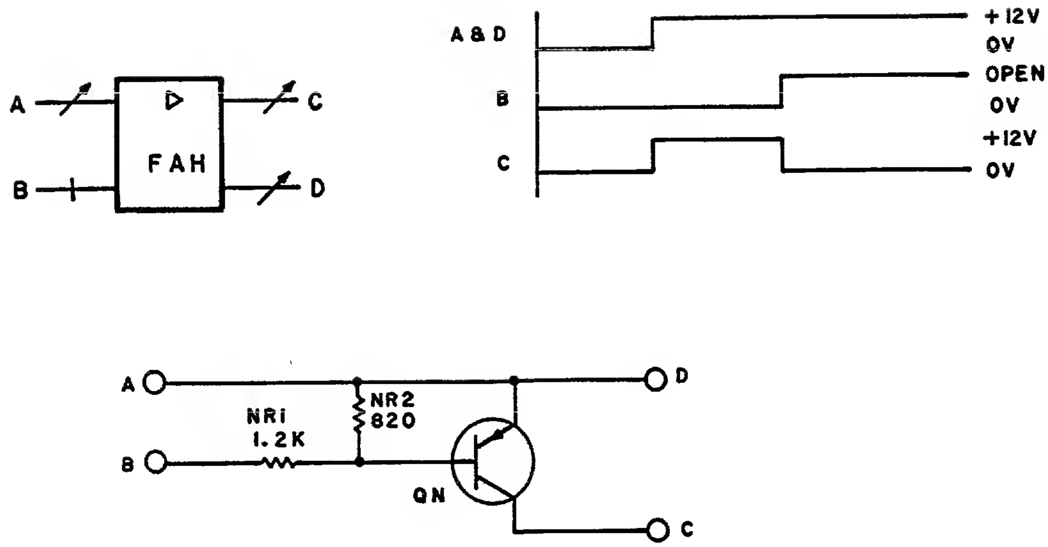
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J128

Controlled Voltage Source - FAG

The FAG circuit is a controlled voltage source providing a controlled voltage to Write Driver - JAG.

The circuit consists of an operational amplifier and a two transistor buffer extends the output current capability. The transistor buffer is included in the negative feedback circuit to reduce the output voltage change due to temperature variation.

The output at B (V_B) is related to the two inputs V_R and A(V_A) by the following expression: $V_B = V_R \left(1 + \frac{XR2}{XR1}\right) - \frac{XR2}{XR1} V_A$



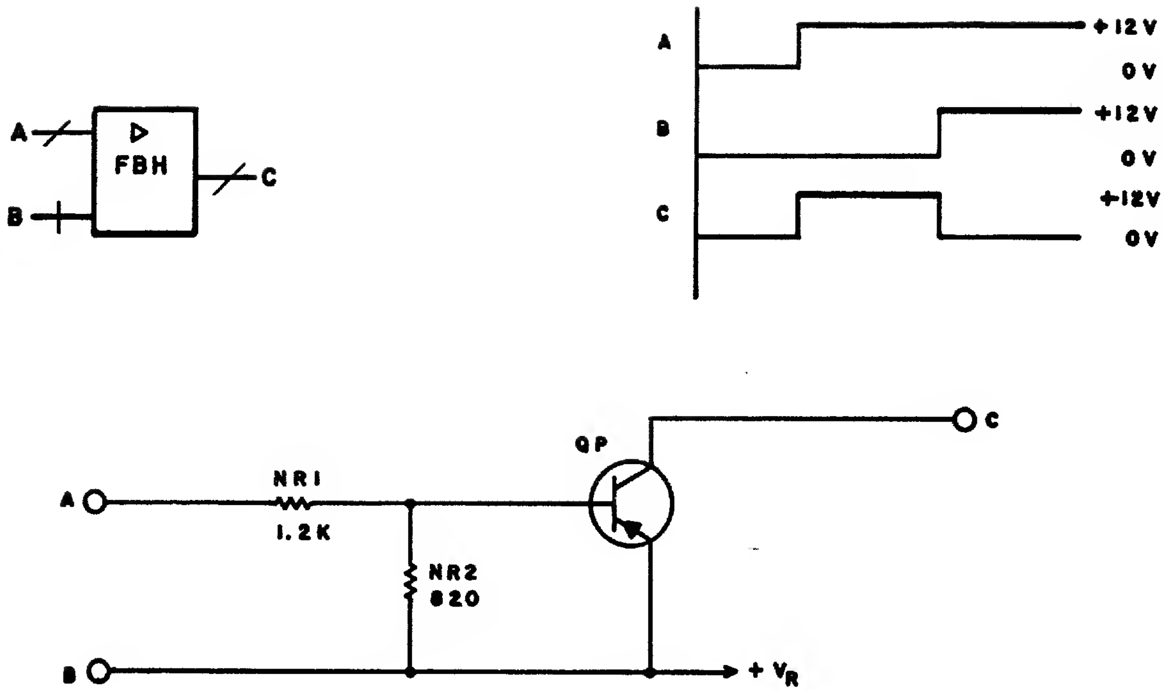
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J13

VOLTAGE SWITCH - FAH

The FAH circuit is a voltage switch which transfers a voltage at point A to point C when QN is turned on by the proper voltage condition at point B.

In a typical circuit the voltage at point A (V_a) is +12 volts. With 0 volts applied to point B (V_b= 0 volts), transistor QN turns on and point C goes to +12 volts (V_c = +12 volts). When point B is open (as when connected to an open collector IC that is turned off) QN will turn off and point C will be disconnected from point A and return to any quiescent potential in the circuit it is connected to.

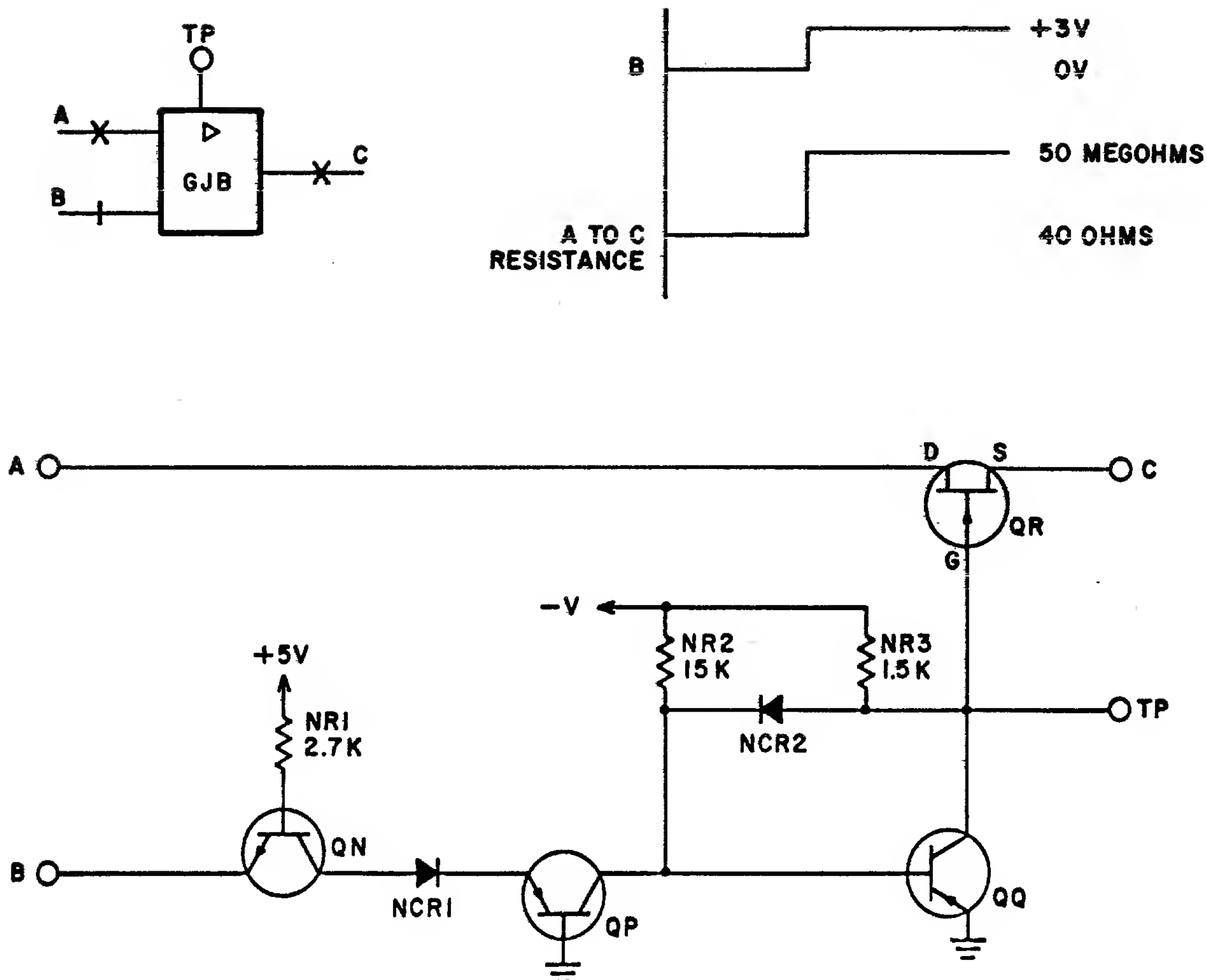


NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

VOLTAGE SWITCH - FBH

The FBH is a voltage switch which transfers a voltage at input B to output C when QP is turned on by the proper voltage condition at input A.

In a typical circuit the voltage at input B is +12 volts. With 0 volts applied to input A, transistor QP turns on and output C goes to +12 volts. When input B is open (as when connected to an open collector IC that is turned off) QP will turn off and output C will be disconnected from input B and return to any quiescent potential in the circuit it is connected to.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

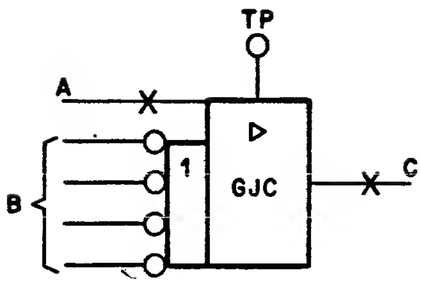
6T132

GATED ANALOG CLAMP - GJB

The GJB circuit functions to turn QR (an N channel junction field effect transistor) on when a logical 0 is applied at input B and to turn QR off when a logical 1 is applied at input B.

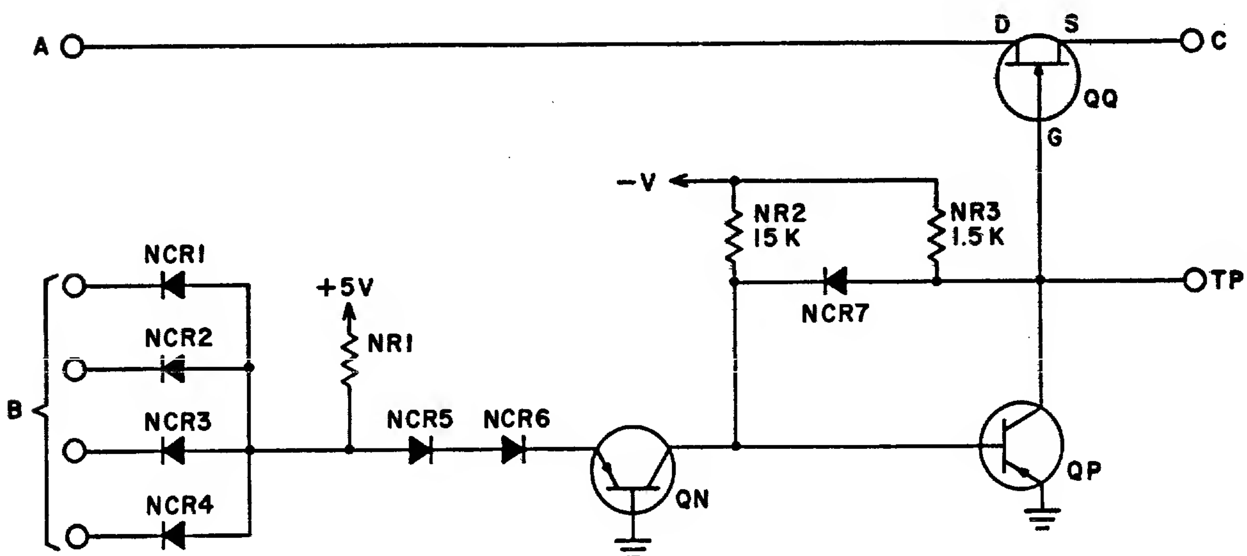
In actual application input A is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal C is connected to the output of the operational amplifier. When QR turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QR are 40 ohms and 50 megohms respectively.



IF ANY INPUT B EQUALS 0 VOLTS,
THE A TO C RESISTANCE EQUALS 40 OHMS.

IF ALL INPUT B'S EQUAL +3 VOLTS,
THE A TO C RESISTANCE EQUALS 50 MEGOHMS.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

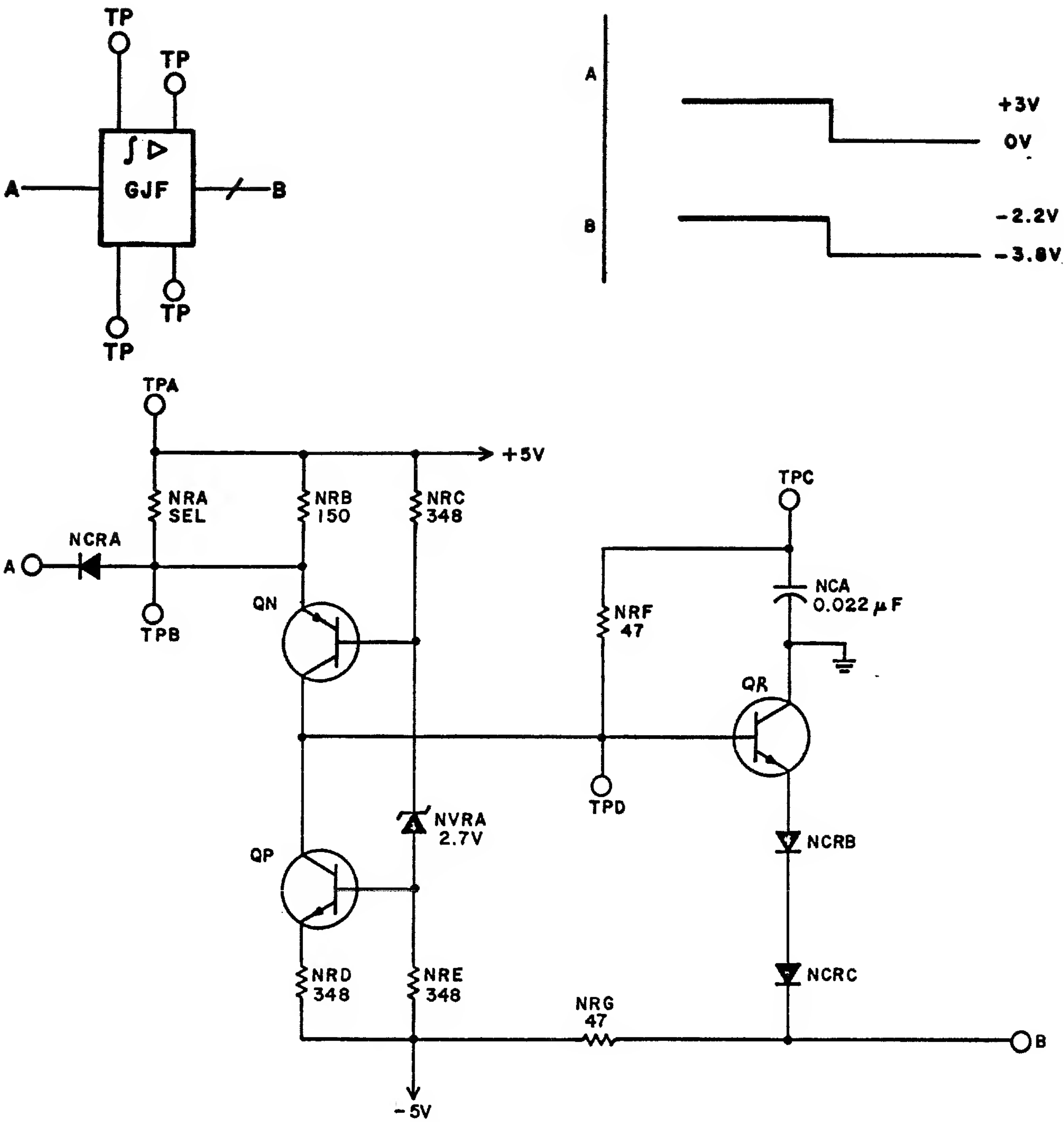
8T133

MULTIPLE GATE ANALOG CLAMP - GJC

The GJC circuit functions to turn QQ (an N channel junction field effect transistor) on when a logical 0 is applied at any of the B inputs and to turn QQ off when all of the B inputs are at a logical 1.

In actual application input A is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal C is connected to the output of the operation amplifier. When QQ turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QQ are 40 ohms and 50 megohms respectively.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7855

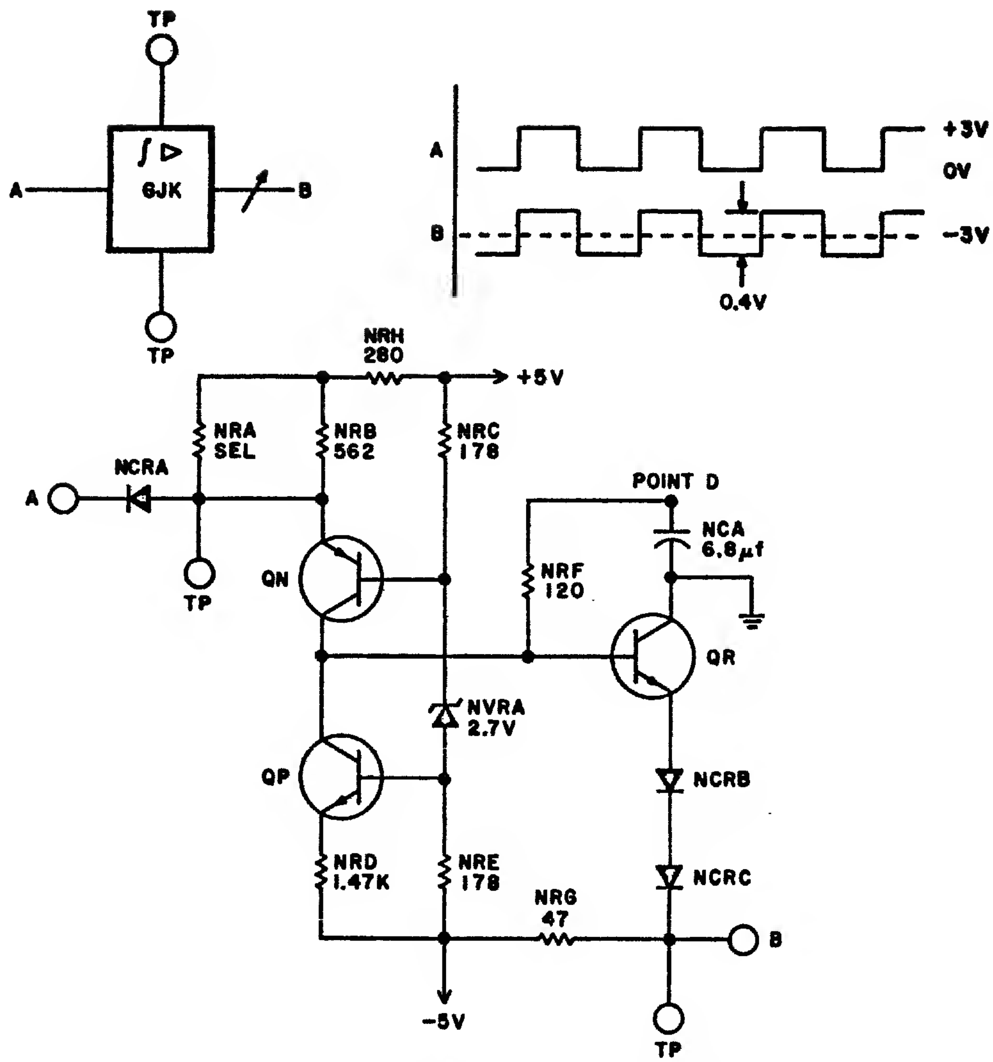
LOW PASS FILTER AND AMPLIFIER – GJF

The GJF circuit consists of a bidirectional current pump, a filter, and a level shifter. The circuit converts TTL input signals from a comparator circuit and integrates these signals to produce a dc voltage level at TPC. Because of the phase locked oscillator closed loop, the current pump drives the dc level at TPC to reach a steady state when the signal at input A is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency causes a change in voltage at TPC.

NRC, NVRA, and NRE form a reference voltage divider for the current pump. NRD and QN is the negative going current sink. This sinks a current of approximately 7.5 ma continually. NCRA, NRA, NRB, and QN form a switchable current source of approximately 15 ma. When a square wave of TTL logic levels is applied to input A, NCA alternately is charged and discharged by 7.5 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times, therefore, the voltage at TPC has very little ac component in it.

Resistor NRF generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRF and the currents from the bidirectional pump. The net result at TPD is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QR, NCRB, NCRC, and NRG form a buffer and level shifting circuit. They shift the waveform at TPD negatively to a level appropriate for controlling voltage controlled oscillator.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J170

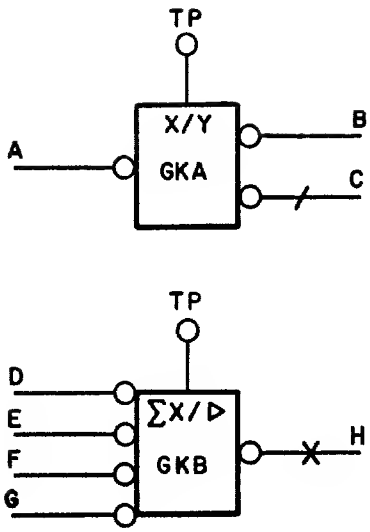
LOW PASS FILTER AND AMPLIFIER - GJK

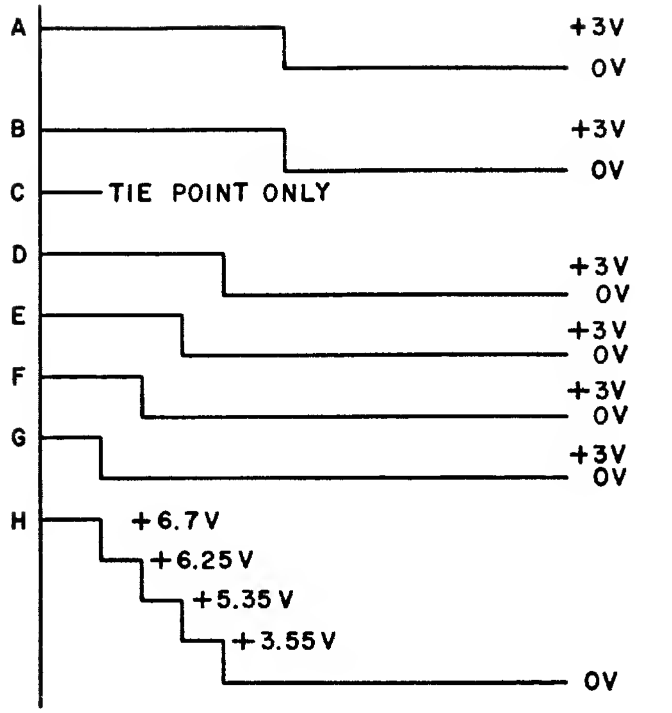
The GJK circuit consists of a bidirectional current pump, a filter, and a level shifter. The circuit converts TTL input signals from a comparator circuit and integrates these signals to produce a dc voltage level at output B. Because of the phase locked oscillator closed loop, the current pump drives the dc level at point D to reach a steady state when the signal at input A is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency (duty cycle) causes a change in average ac voltage across NRF.

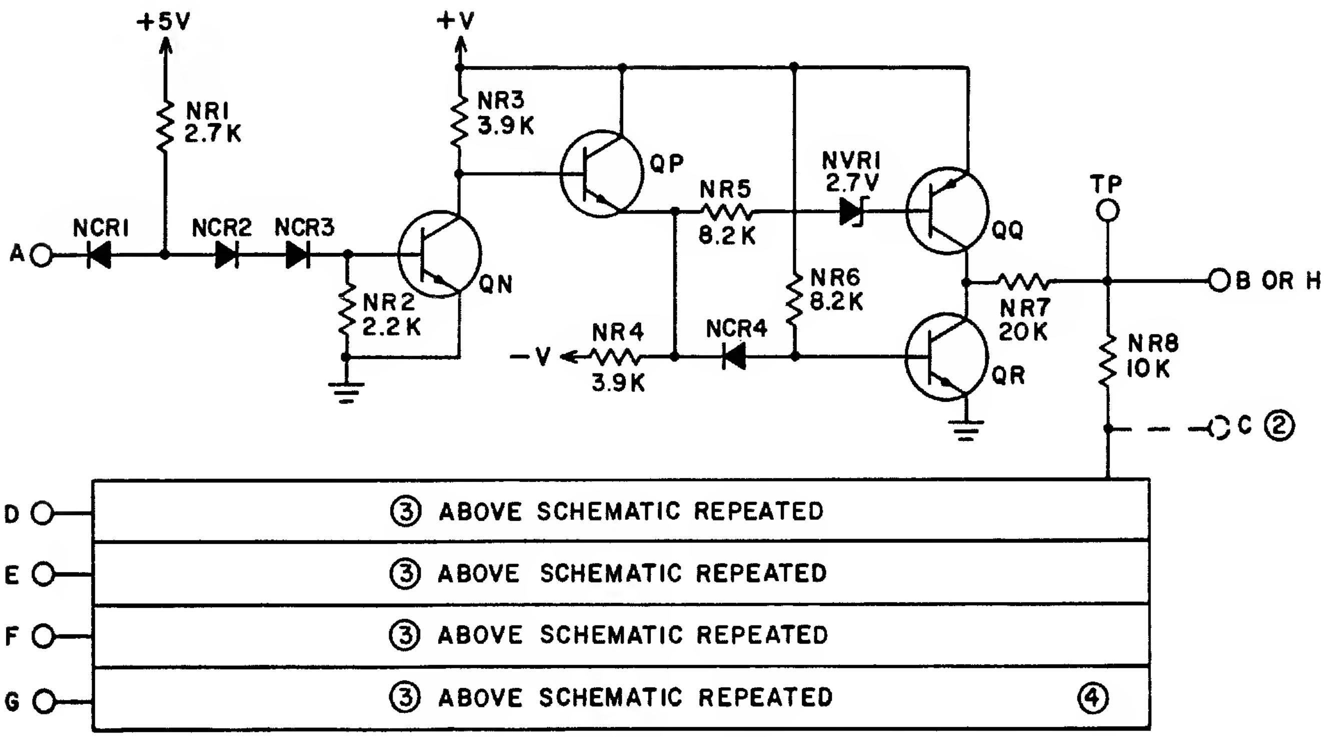
NRC, NVRA, and NRE form a reference voltage divider for the current pump. NRD and QP is the negative-going current sink. This sinks a current of approximately 2 ma continually. NCRA, NRA, NRB, and QN form a switchable current source of approximately 15 ma. When a square wave TTL logic level is applied to input A, NCA alternately is charged and discharged by 5 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times, therefore, the voltage across NCA has very little ac component in it.

Resistor NRF generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRF and the currents from the bidirectional pump. The net result at the base of QR is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QR, NCRB, NCRC, and NRG form a buffer and level shifting circuit. They shift the waveform at the base of QR negatively to a level appropriate for voltage control oscillator frequency.







NOTES: 1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.

② APPLICABLE TO GKA ONLY.

③ APPLICABLE TO GKB ONLY.

④ NR8 IN THIS SECTION IS 20K WITH LOWER END TO GROUND.

6T136

LEVEL TRANSLATOR - GKA AND DIGITAL TO ANALOG CONVERTER - GKB

The GKA and GKB circuits when used together comprise a 5-bit D/A converter. The GKB circuit used singly is a 4-bit converter.

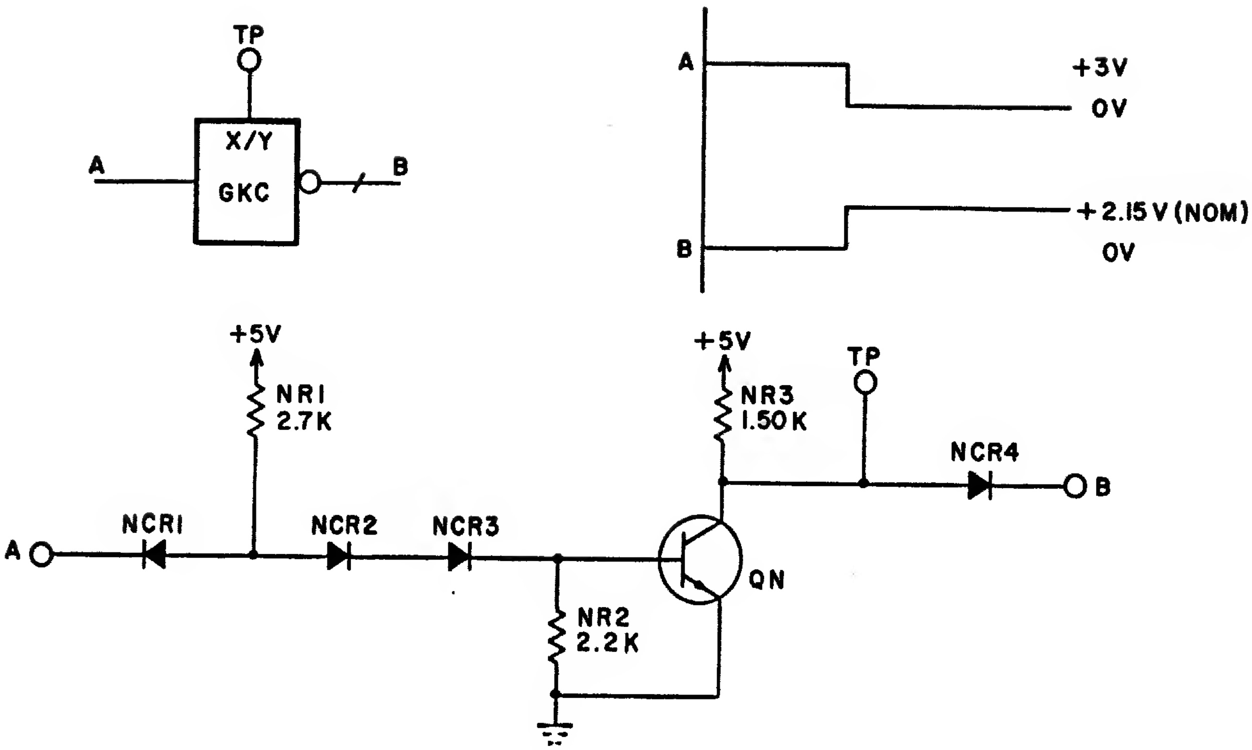
The GKB consists of four voltage switches and a 4-bit R-2R D/A ladder network. Each voltage switch circuit applies positive voltage to the related ladder input when its input is a logical 1. A voltage switch applies ground to the related ladder network input when its input is a logical 0.

In the GKB circuit, the digital inputs G, F, E, and D are ordered from least to most significant. When all digital inputs are "1's", the voltage at H is +6.7 v (assuming a 10k ohm load is provided by the following circuit). When all digital inputs are "0's" the analog output is 0v (except for a +6 mv, max., dc offset). The analog output for an increase of one in the digital input code is +446 mv, nominal.

QN and QP operate as a saturated switch and an emitter follower, respectively, in the voltage switch circuit. QQ and QR operate as low offset saturated switches, only one of which is on at a time.

The R-2R D/A ladder has a resistance of 10k ohms from any node to ground and divides by two the voltage at the next lower in significant note.

The GKA circuit is identical to one stage of the GKB.



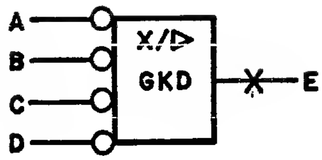
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

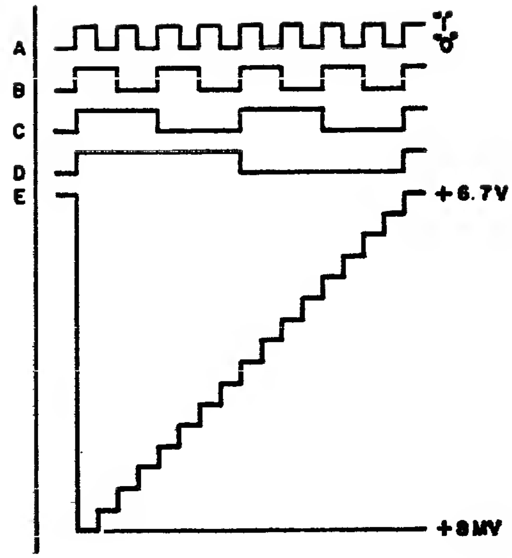
87136

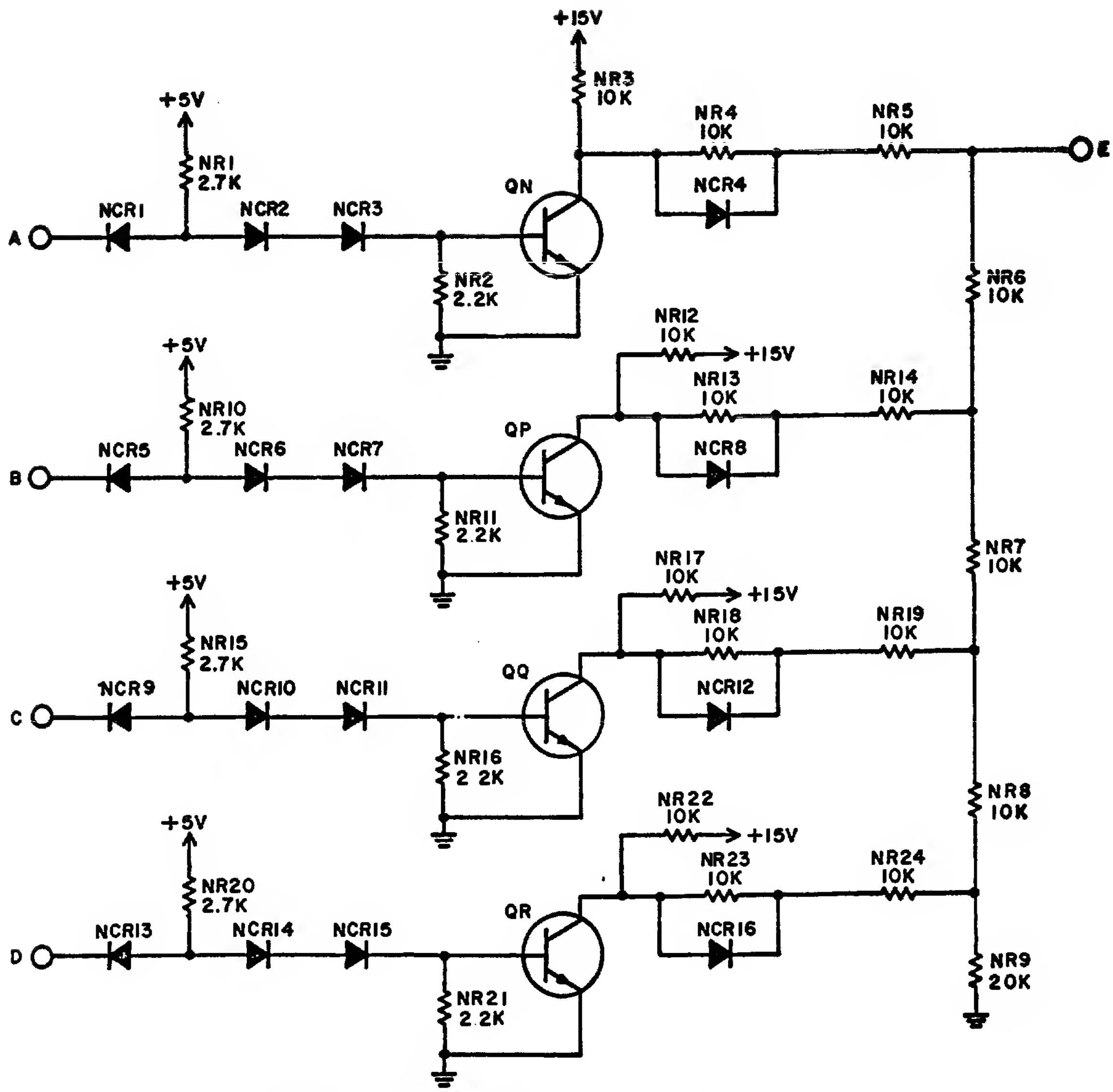
LEVEL TRANSLATOR - GKC

The GKC circuit converts a logical 0 to a +2.15 (nominal) level used to inject a current signal into the summing point of an operational amplifier. Typically a resistor is connected between point B and the operational amplifier summing point to establish the magnitude of this current.

When a logical 1 is present at input A, transistor QN saturates, the output diode NCR4 shuts off, and output B drops to 0 volts removing the current to the operational amplifier summing point.





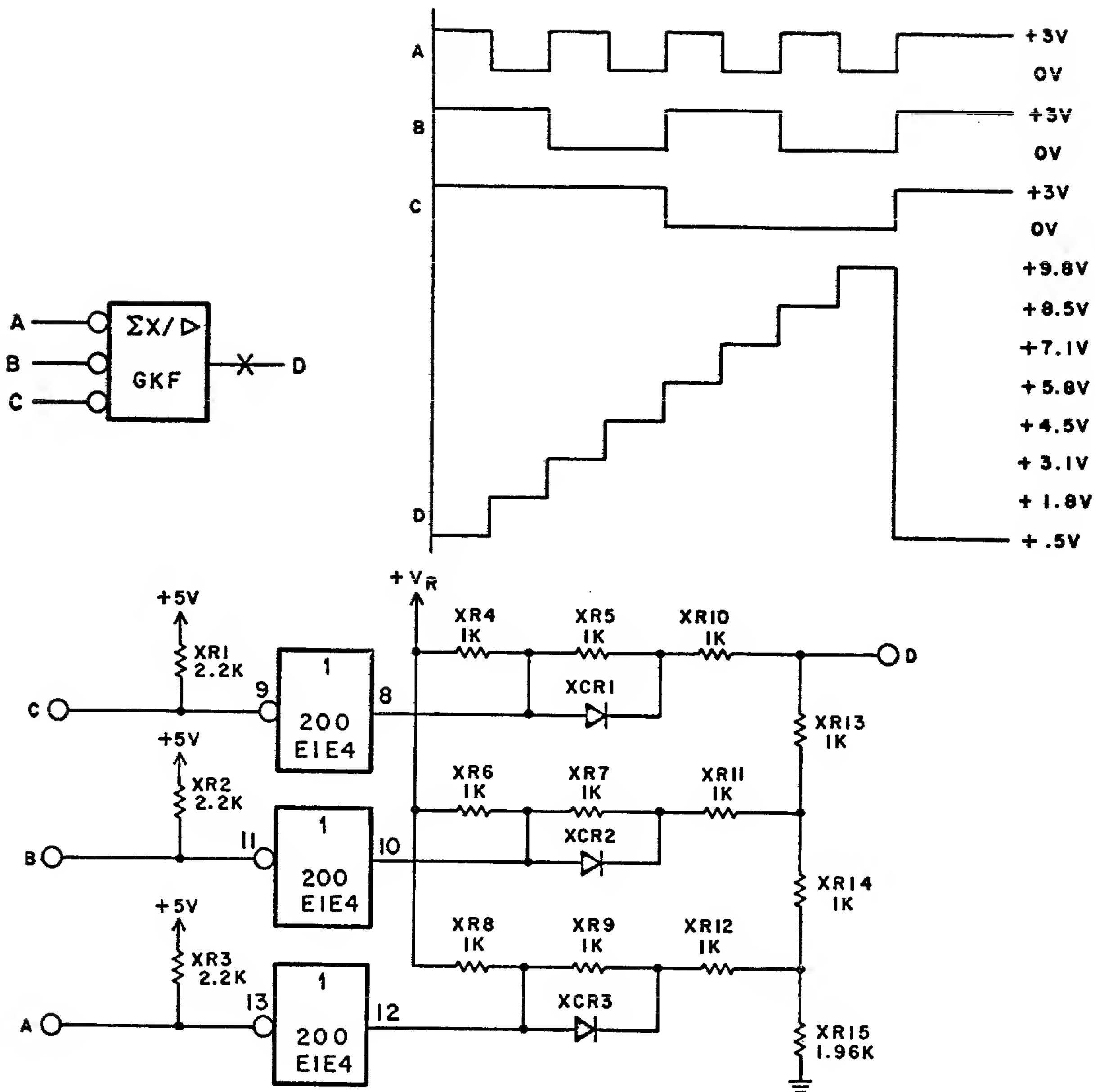


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DIGITAL TO ANALOG CONVERTER – GKD

The GKD circuit is a 4-bit digital to analog converter. The circuit consists of four voltage switches and a resistance ladder network.

The digital inputs A, B, C, and D are ordered from most to least significant. When all digital inputs are "0's", the output at E is approximately +6.7V. When all digital inputs are "1's", the output goes to approximately +8 mv. The analog output increases approximately 420 mv for an increase of one in the digital code.



NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY.

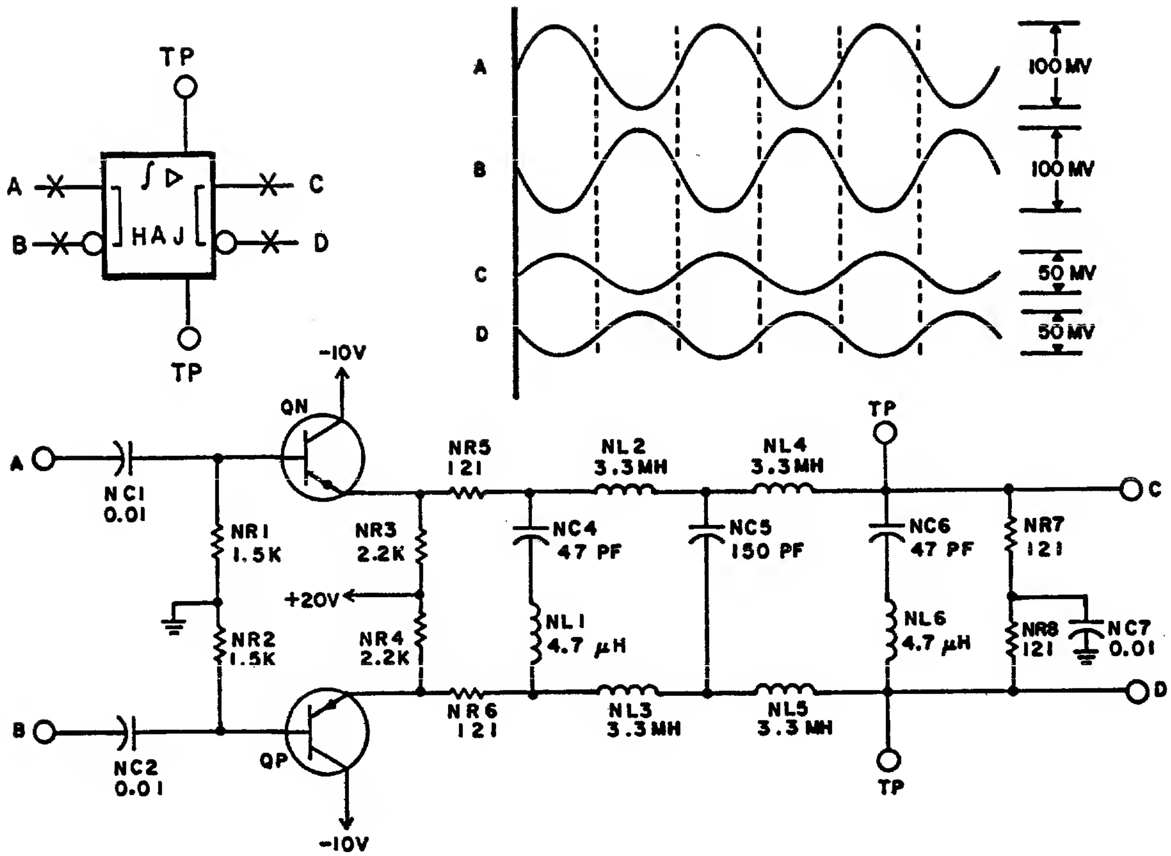
7J14

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

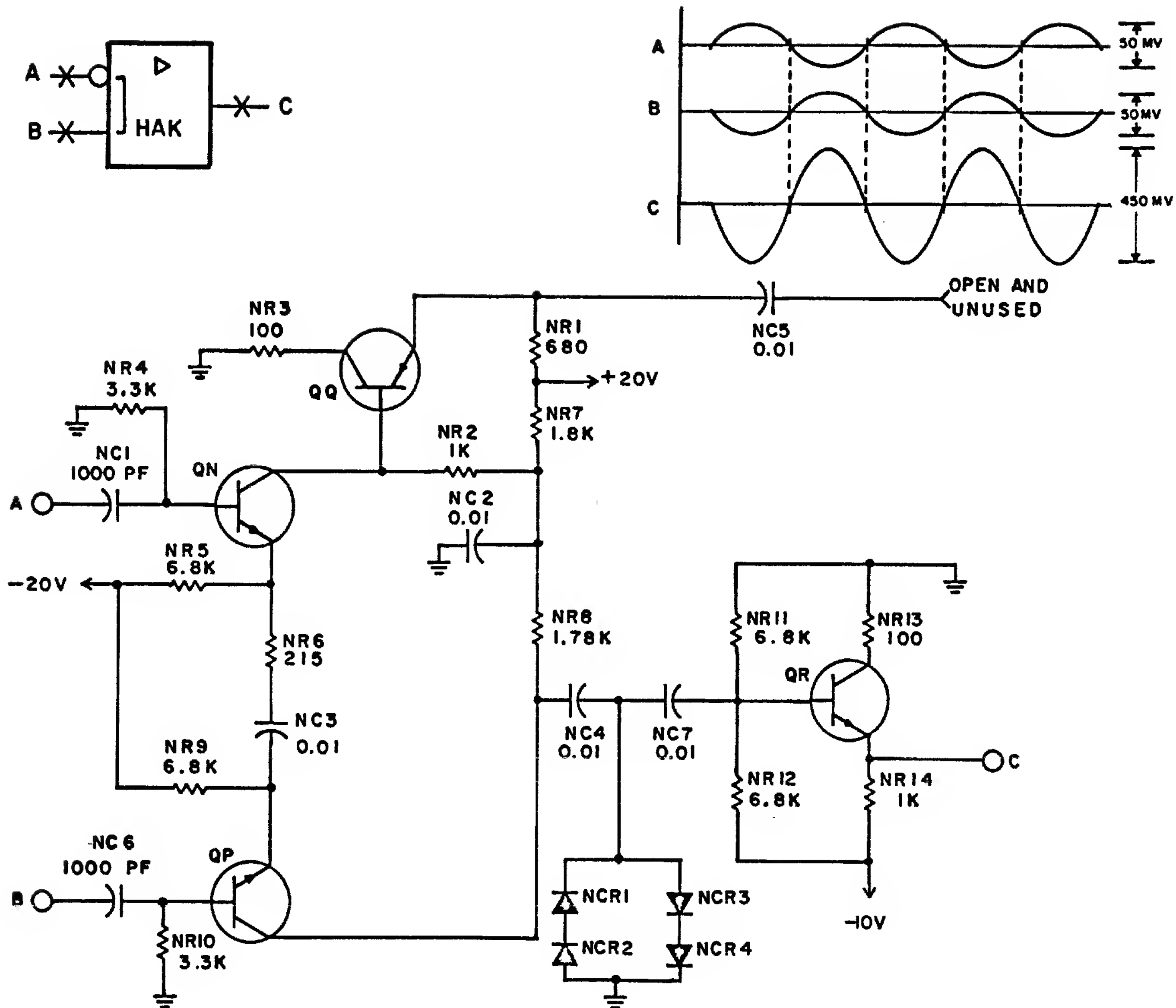
7J19A

Differential Low Pass Filter - HAJ

The HAJ circuit is a differential low pass filter buffered on the input by emitter followers.

The upper cutoff frequency of the filter is approximately 8.5 MHz at -3 db. Attenuation above the cutoff frequency is approximately -36 db/octave.

Input capacitors NC1 and NC2 in conjunction with resistor NR1 and NR2 give the circuit a low frequency cutoff of about 10 KHz at -3 db.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J16A

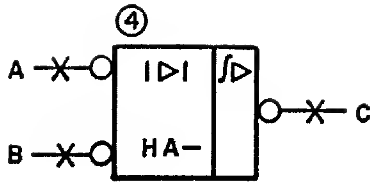
Amplifier - HAK

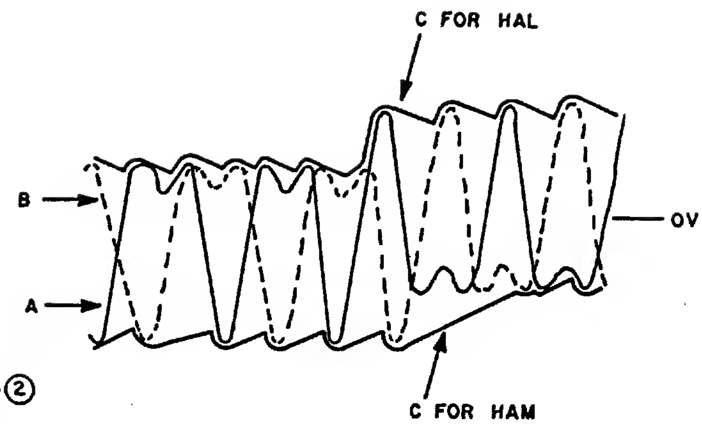
The HAK circuit is a differential input amplifier with a clamped single-ended output.

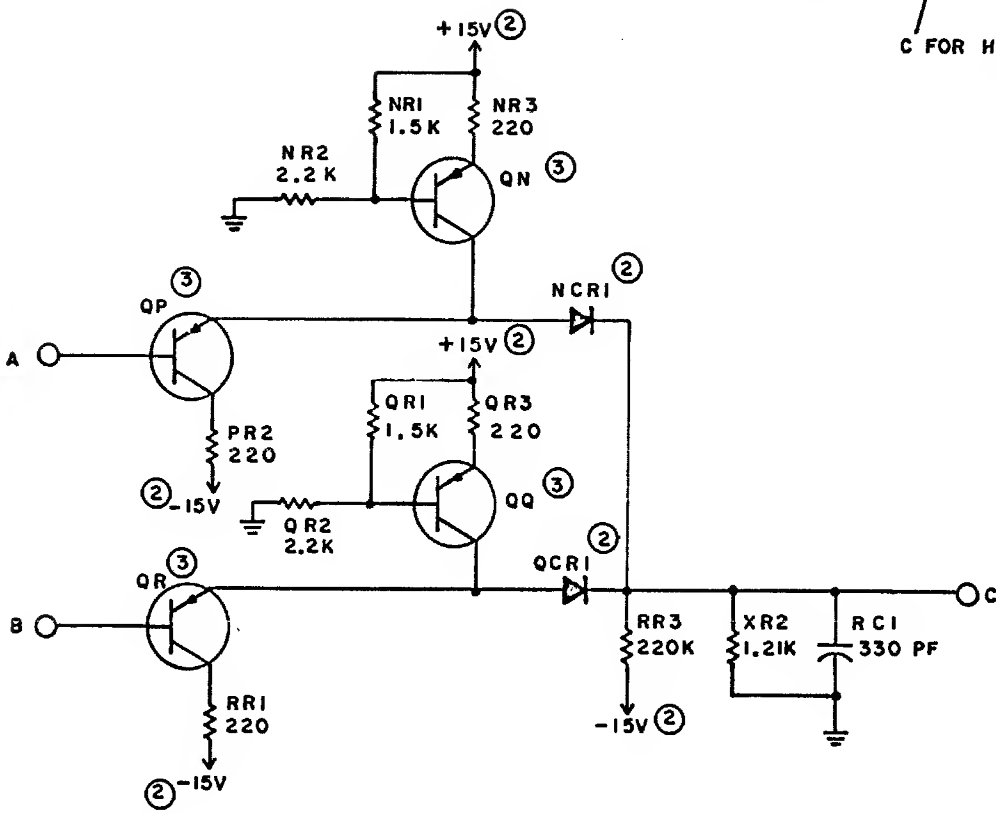
Points A and B are differential inputs to the circuit with NC1 and NC6 acting as coupling capacitors. QN and QP are the amplifying transistors in the common emitter configuration and QQ and QR are emitter followers providing a low impedance output.

NC4 and NC7 isolate DC voltages entering NCR1 through NCR4 from the collector circuit of QP and acts as a clamp to the amplified AC signal if it is larger than the diodes threshold voltage.

Output C is typically connected to the input (A) of the HAN circuit. Output C has a single-ended output to differential input voltage gain of approximately 10 (before clamping).







NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. POLARITY REVERSED ON HAM.
3. NPN USED ON HAM.
4. HAM RECTIFICATION IS NEGATIVE (−I▷I)

7J17

SUMMING RECTIFIER - HAL/HAM

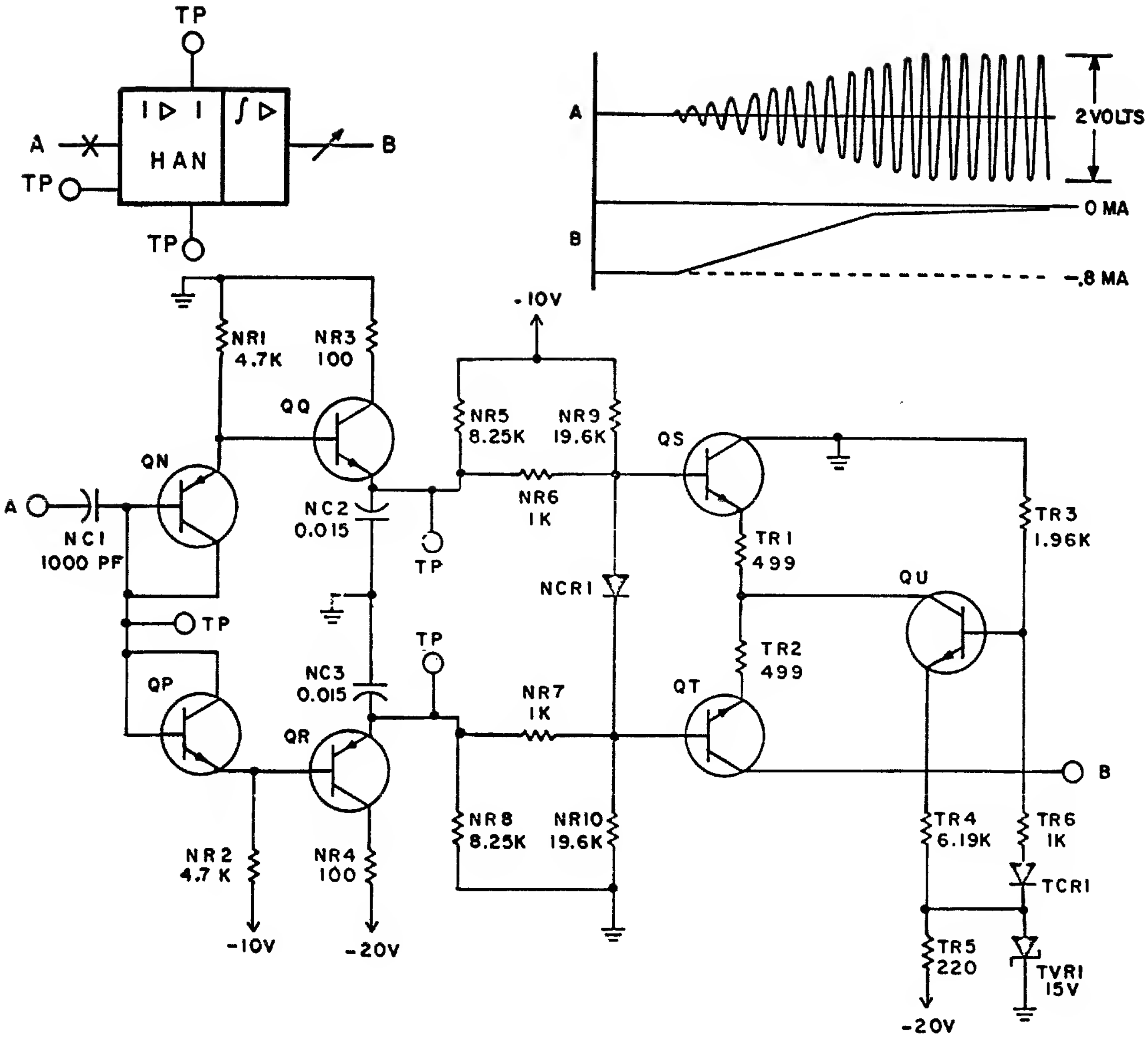
The HAL/HAM circuit is a summing rectifier that receives the MFM (modified frequency modulation) differentiated read signal and a delayed (150 ns) version of the same signal. The circuit OR's the two signals such that the output follows the more positive (HAL) or negative (HAM) signal excursion, giving the appearance of a rectified output. When the outputs of both circuits are observed simultaneously, what results is a silhouette of the two input waveforms. An output capacitor provides integration to maintain most of the positive (HAL) or negative (HAM) charge until the next peak arrives.

An emitter follower at each input receives the delayed or the nondelayed version of the differentiated read signal. Current generators tied to the emitters provide sufficient current for the input transistors and charge the output capacitor during a signal peak.

Assume a positive signal peak occurring at input A of the HAL circuit. As the signal increases toward a peak the QP emitter follows, causing diode NCR1 to turn on and conduct current from QN into the capacitor RC1. At this time the signal at input B is less positive than that at A. Since the QR emitter follows input B, diode QCR1 is back biased off. The capacitor voltage at output C follows the input A signal closely until it peaks. As the signal at A starts decreasing, diode NCR1 starts turning off, due to the stored capacitor charge. The capacitor begins discharging through XR2. At this time output C is more positive than either A or B, and both diodes are cut off.

Now assume the delayed signal at B approaches its peak and becomes more positive than C. The QR emitter follows and turns on diode QCR1 which conducts current from QQ into capacitor NC1. The capacitor voltage at output C now follows input B closely until it peaks. When B begins decreasing, diode QCR1 turns off and the capacitor again starts discharging through XR2.

The HAM circuit operates in a similar manner, except that all polarities are reversed.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

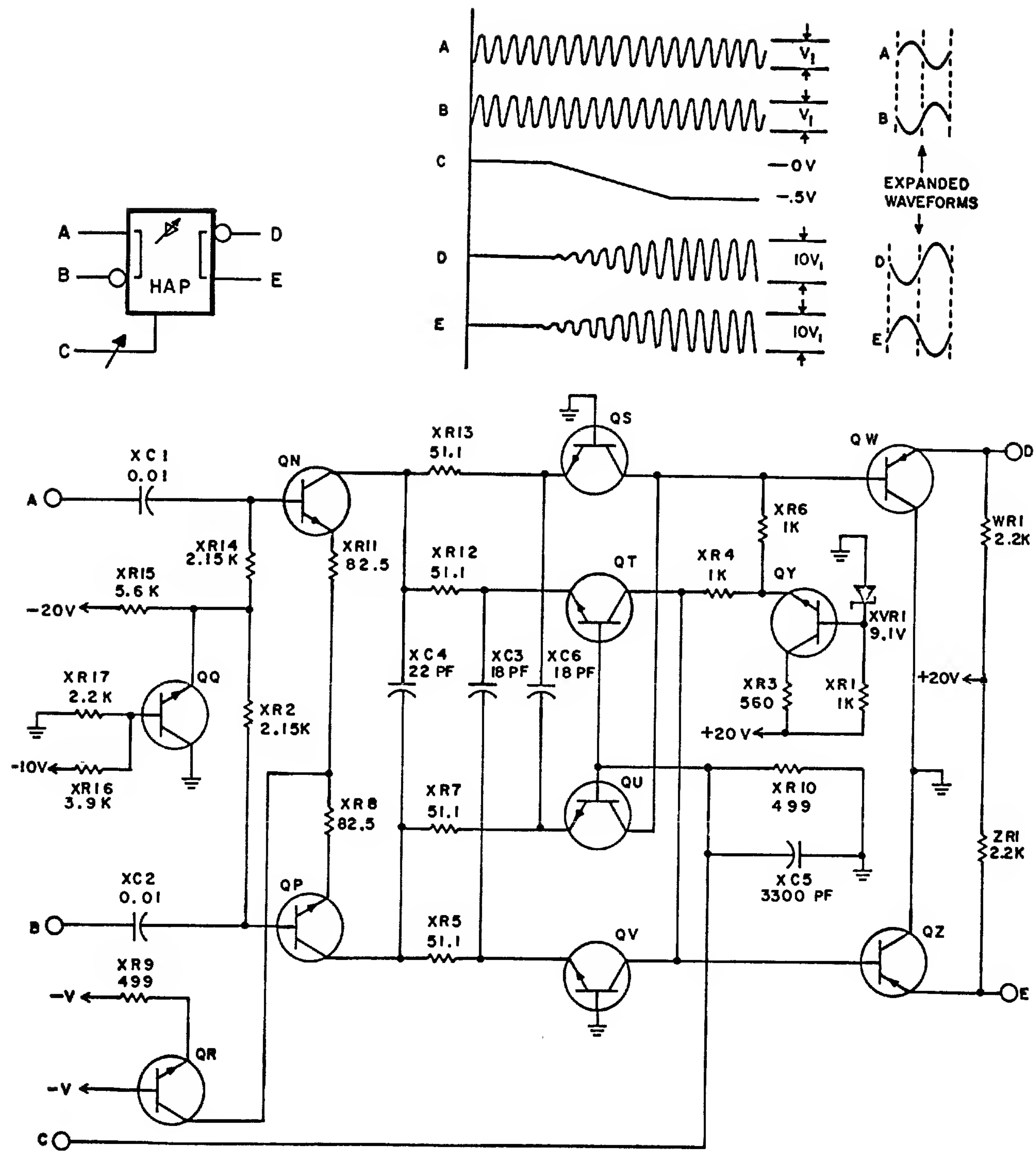
7J18A

Peak Holding Amplifier - HAN

The HAN circuit provides a DC sink current with a magnitude inversely proportional to the magnitude of the AC input signal. Typically the input signal at point A is an amplified read head signal coming from output C of the HAK circuit. Output B is connected to point C of the HAP circuit and controls the gain of that circuit.

QN, QQ, QP and QR form a positive and a negative rectifier. When an AC signal is applied to the input, QQ charges NC2 to a positive peak value and QR charges NC3 to a negative peak value. These peak values are held by the two capacitors which discharge with a time constant determined by NC3 and NR8 in parallel with NR7 and NR10. With a long time constant compared with the frequency of the input AC signal, the voltage on the two capacitors is a DC voltage.

The voltage difference across NC2 and NC3 is directly proportional to the peak-to-peak amplitude of the input waveform and is applied through resistor dividers to current amplifier QS and QT. With no signal at input A, the current amplifier is biased to permit QT to pass all the current supplied by current sink QU. As the AC input signal increases in amplitude the peak difference appearing across NC2 and NC3 is applied to the current amplifier, and QS starts to pass sink current which cuts down current flow through QT.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J19A

AGC AMPLIFIER - HAP

The HAP circuit is a differential amplifier with gain controlled by a negative voltage at input C.

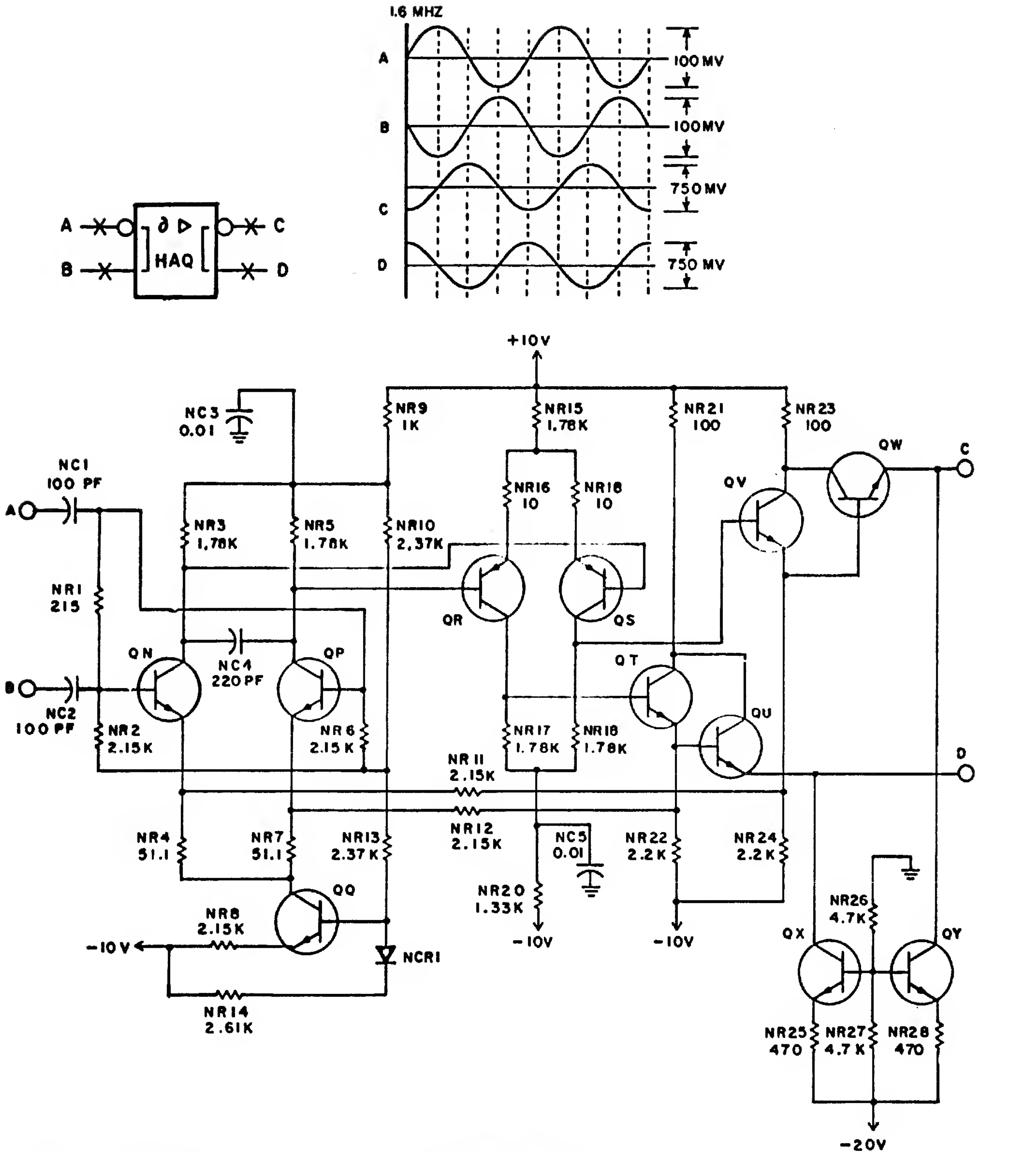
QN and QP are amplifying transistors with their maximum gain determined by the ratio of XR8 and XR11 to XR4 and XR6.

Common base amplifiers, QS, QT, QU, and QV pass amplified current signals to resistors XR4 and XR6. QS and QU pass out of phase signals to collector resistor XR6. Likewise, QT and QV pass out of phase signals to collector resistor XR4.

Control voltages on the bases of QT and QU control circuit gain. With 0 volts for control voltage, QS, QT, QU, and QV turn on equally, causing out of phase voltage to cancel, leaving a net output or gain of 0 volts. Increasing the control voltage negatively starts turning off QT and QU causing the amplifier gain to increase. Turning off QS, QT, QU, and QV requires that the control voltage be approximately -0.5 volts, which allows an amplifier gain of 10.

Emitter followers QW and QZ provide low output impedance.

QQ, XR15, QR16 and XR17 make up a current sink network which controls the collector current of QN and QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

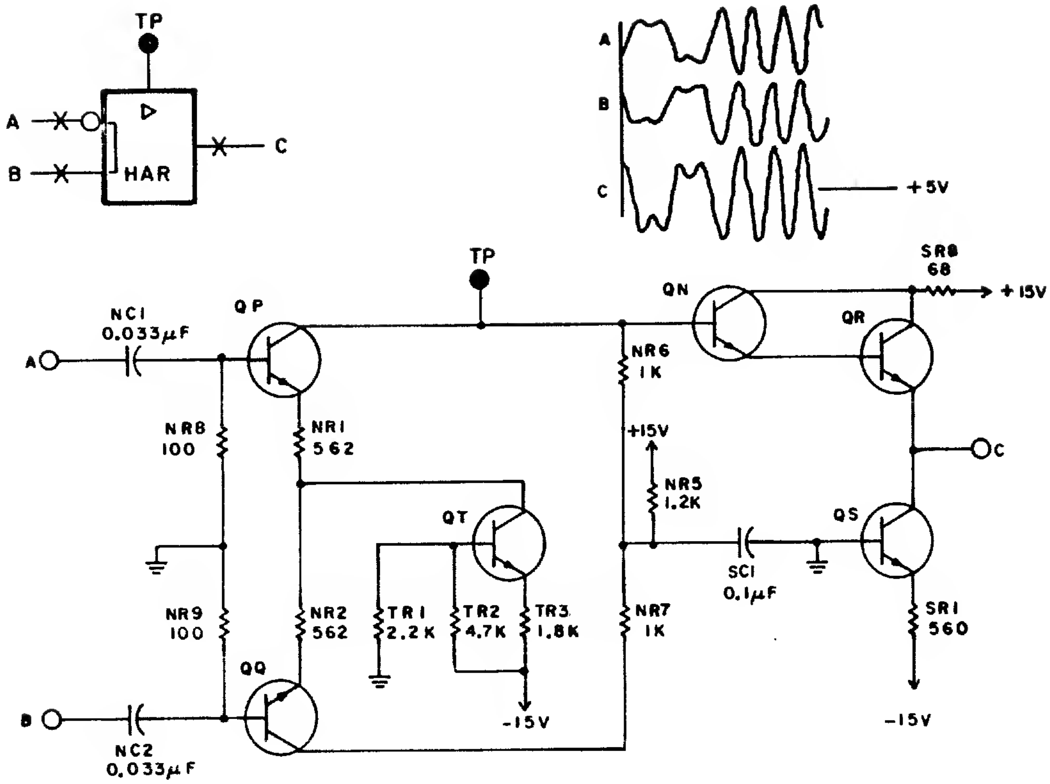
Differentiator/Amplifier - HAQ

The HAQ circuit consists of a passive RC network (used as a differentiator and a differential amplifier) to boost the attenuated signal level.

The HAQ, inputs A and B, are connected to outputs D and E of circuit HAP, which supplies an amplified read head signal. NC1, NR1 and NR2 make up the differentiator which has a break frequency at 15 MHz.

The two stage differential amplifier consists of first stage QN and QP with current sink QQ direct coupled to second stage QR and QS. QT, QU and QV, QW form darlington emitter followers for low output impedance capable of driving coax lines terminated by 100 ohm resistors. QX and QY are constant current sources.

NR11 and NR12 provide AC/DC feedback from the output to input emitters of the first stage. Closed loop voltage gain is proportional to the ratio, NR11 to NR4 (and NR12 to NR7). Capacitor NC4 provides rolloff at the upper cutoff frequency.



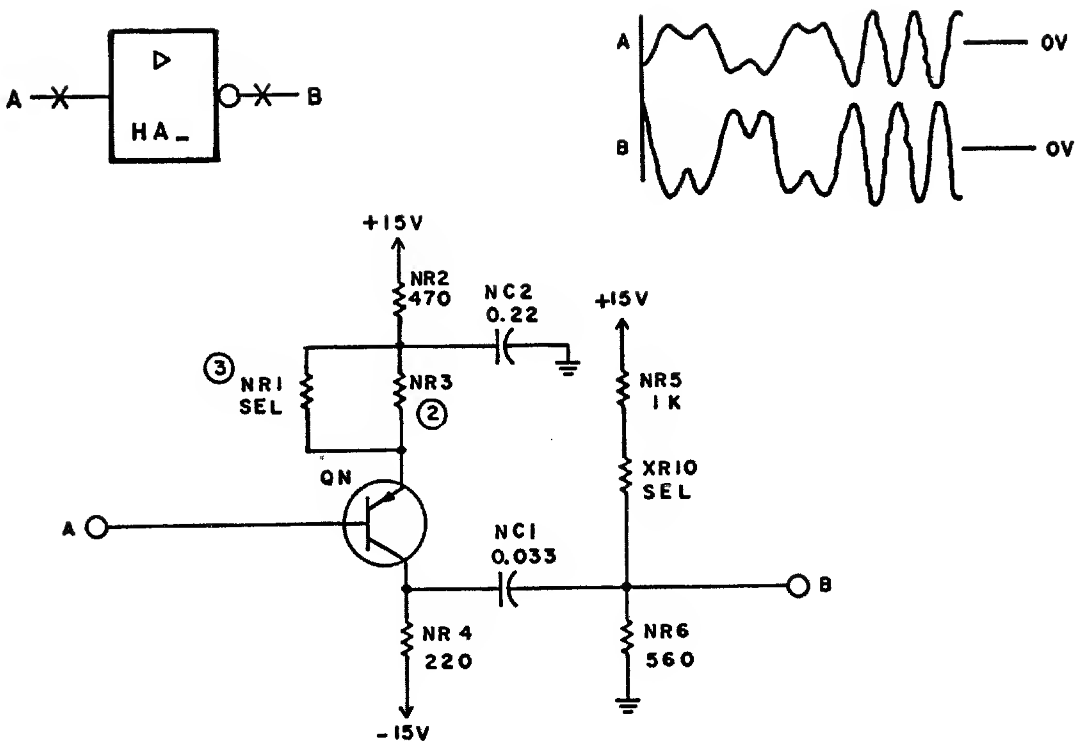
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY

7J21B

DIFFERENTIAL AMPLIFIER - HAR

The HAR circuit accepts a double-ended MFM (modified frequency modulation) differentiated signal and provides a single-ended output suitable for driving a delay line. The maximum input differential voltage is approximately 1.8 volts. The overall circuit gain is approximately 1.6.

Transistors QP, QQ and constant current source QT form the differential amplifier stage and give common mode signal rejection. Voltage gain is given approximately by NR6 divided by NR1 or NR7 divided by NR2. The collector of QP drives transistors QN and QR which are connected in a low loading Darlington pair (high current amplification configuration). This circuit in conjunction with a second constant current source, QS, gives a single-ended output.



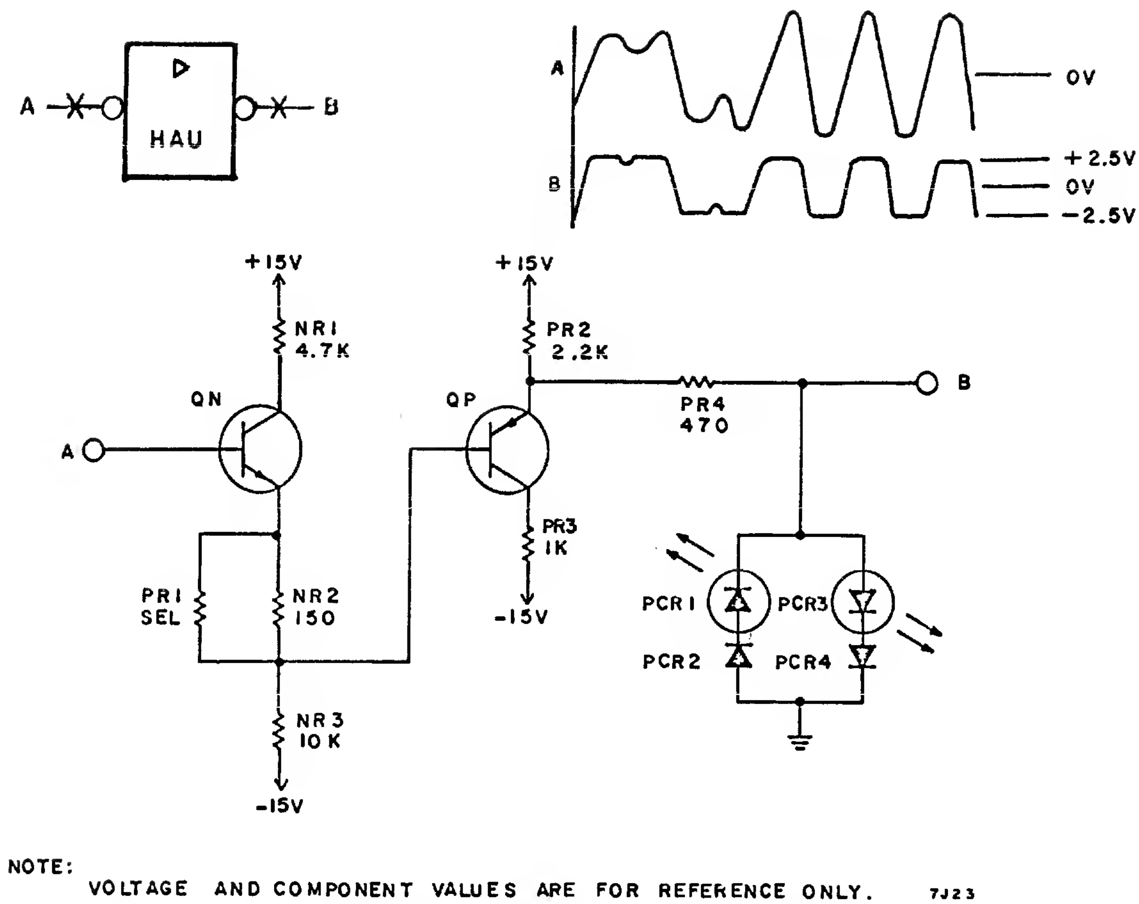
NOTES:
1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. 100-OHMS ON HAT, 22-OHMS ON HAS.
3. NOT USED ON HAS.

7J22

AMPLIFIER - HAS/HAT

The HAS/HAT circuit amplifies the MFM (modified frequency modulation) differentiated read signal. The circuit gain is approximately 6.5 for the HAS and 3 for the HAT.

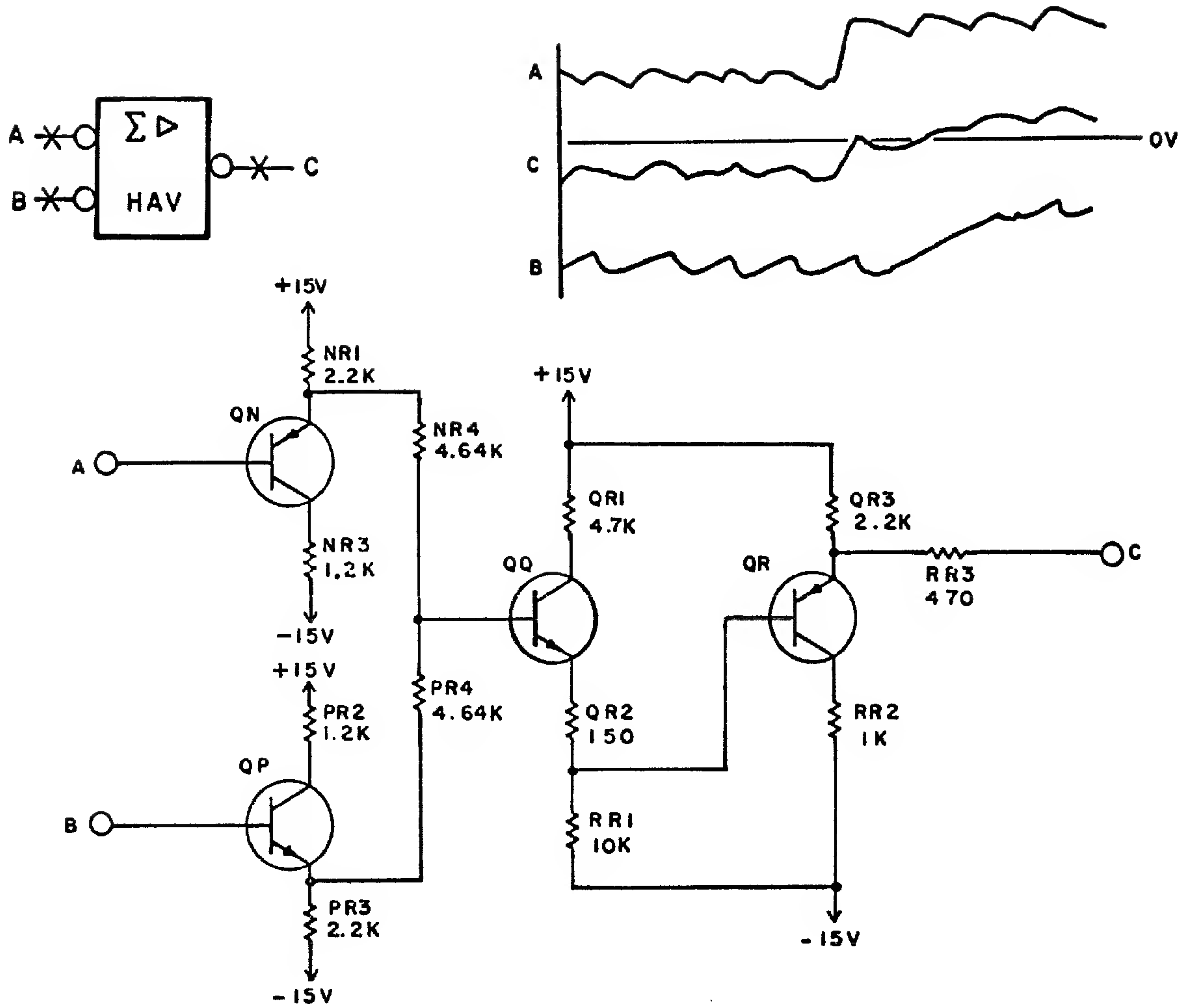
Transistor QN functions as a simple common emitter amplifier. Capacitor NC2 applies ac ground to the junction of NR3 and NR4. Capacitor NC1 provides ac coupling to the output and enables the output bias level to be adjusted to zero volts by selecting resistor XR10.



BUFFER AMPLIFIER - HAU

The HAU circuit incorporates two emitter followers in series to provide a buffer with high input impedance and low output impedance. The circuit is used to drive a zero crossover detector. Diode clamps are used to provide protection against large signal swings at the crossover detector input.

An MFM (modified frequency modulation) differentiated signal at the input encounters a silicon junction voltage drop at QN and a further voltage drop due to NR2 and the selected resistor PR1. This second drop is approximately 250 mv. A voltage rise is seen at QP such that the output is left biased approximately 180 mv negative. The selected resistor is chosen to match this dc bias with the bias at the output of the averaging amplifier, HAV. The diode clamps limit output signal amplitude to 2.5 volts above and below ground.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

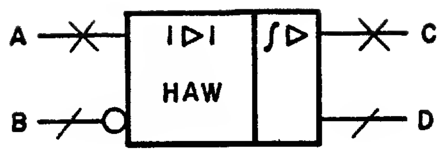
7J24

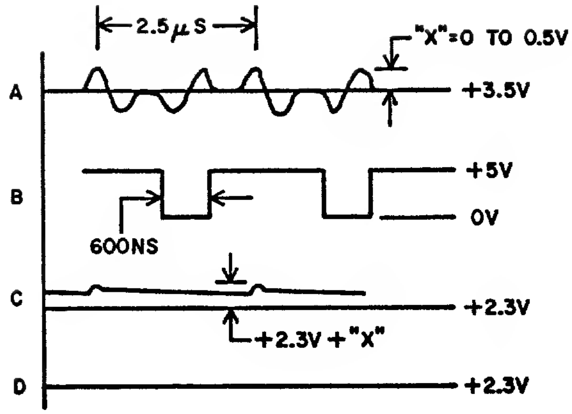
AVERAGING AMPLIFIER - HAV

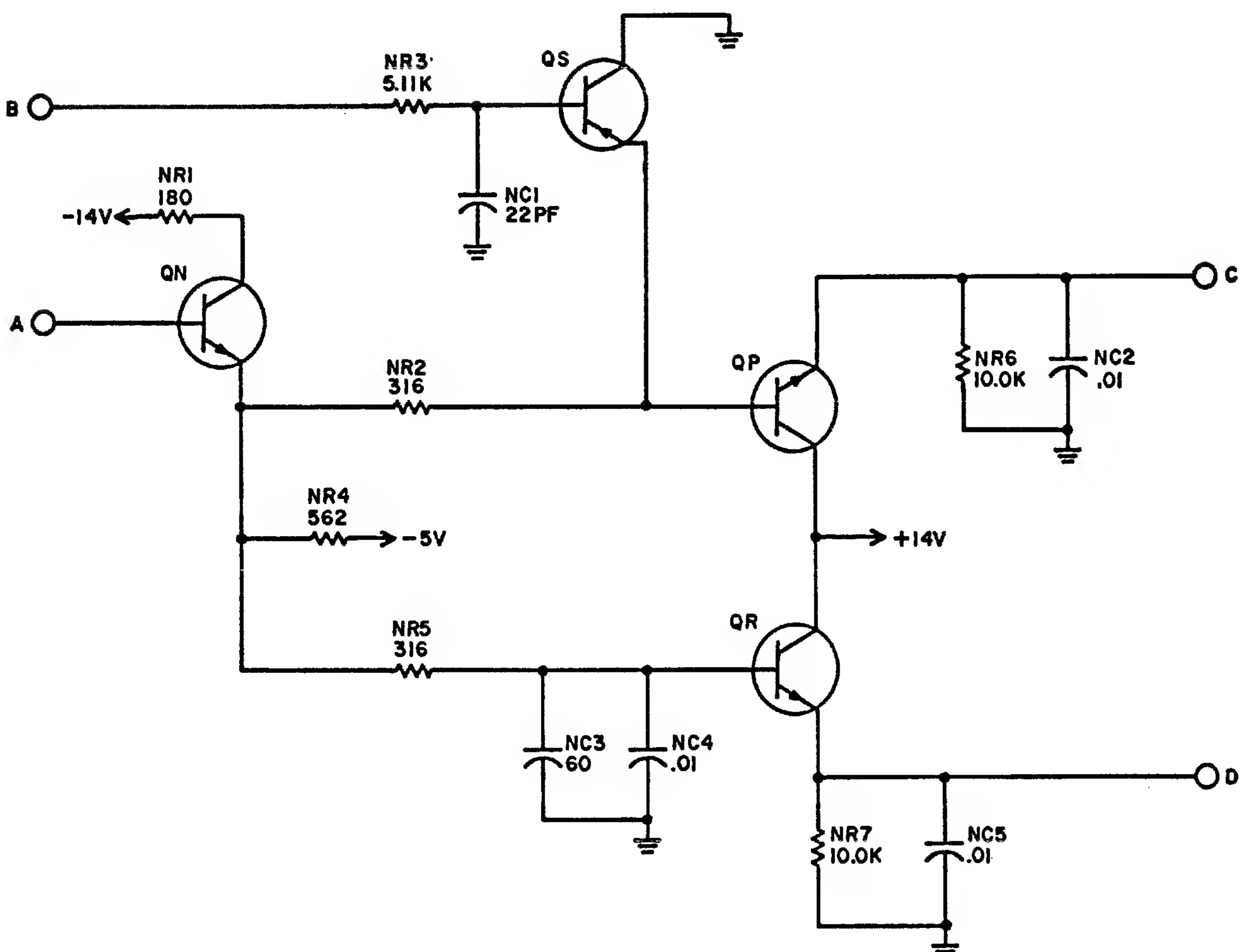
The HAV circuit is an averaging amplifier that receives two waveforms representing the differentiated MFM (modified frequency modulation) read signal peak amplitude. The circuit forms the instantaneous average or mean baseline of the two inputs. The mean baseline is used later in the read circuit to extract the information from the delayed differentiated read signal.

Input A is always biased in the positive direction. Input B is biased by a similar amount in the negative direction. The amount of biasing is a function of the peak amplitude of the amplified differentiated read signal. Transistors QN and QP are emitter followers which reduce the loading on the previous circuit. These elements feed a voltage divider formed by equal valued resistors NR4 and PR4. Since current through the divider is always in the direction from NR4 to PR4, the divider output voltage is the instantaneous average of the inputs.

Transistors QQ and QR form a buffer stage to reduce loading on the divider output. Transistor QR2 adds a slight negative dc bias to the output signal. The buffer output is suitable for driving a zero crossover detector.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J108

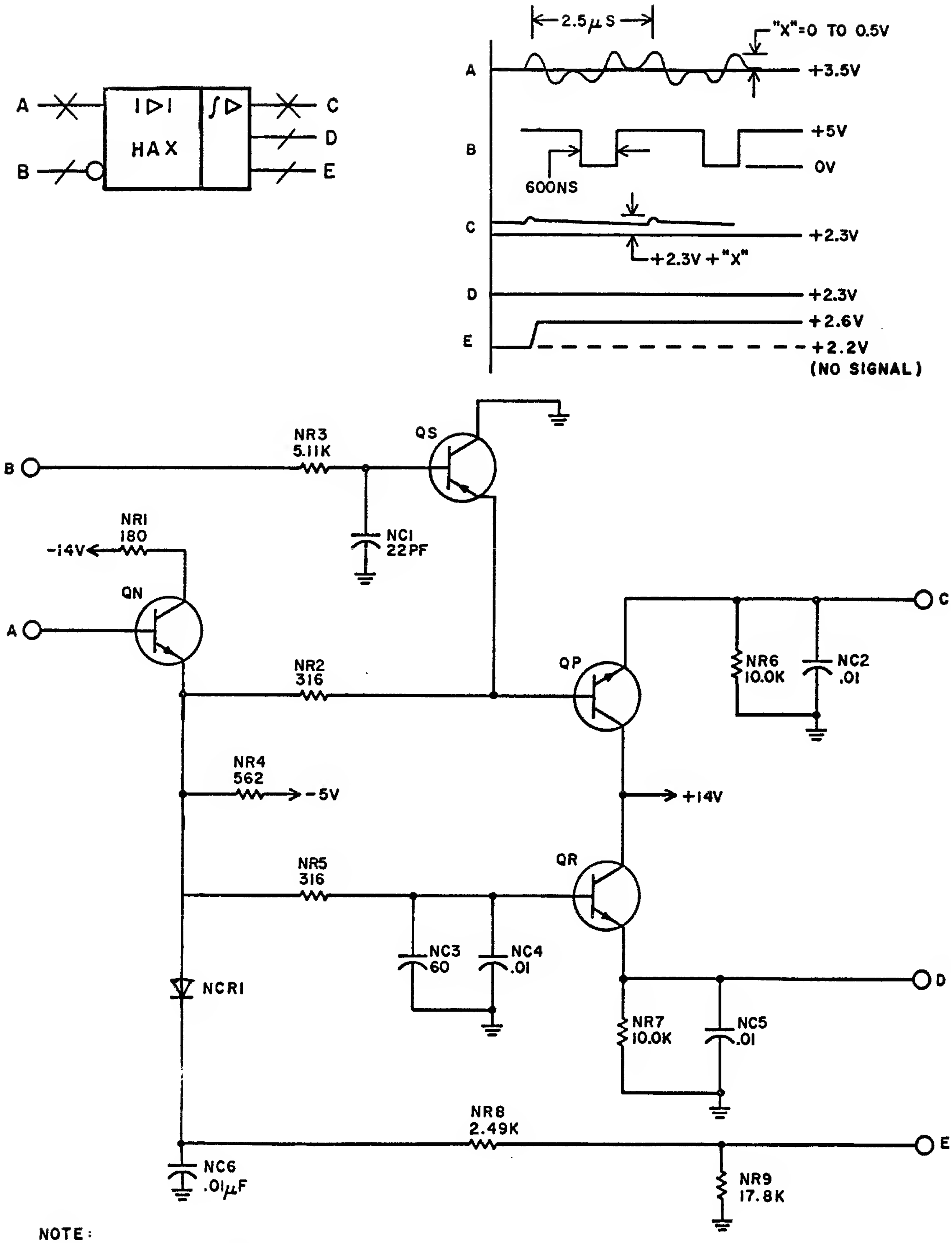
SUMMING RECTIFIER – HAW

The HAW circuit is a summing rectifier that receives the differentially-amplified dibit signals read from the servo head. The outputs are applied to an operational amplifier connected as a differential amplifier to generate a rectified signal proportional to the average amplitude of the dibit signal. The HAW circuit rectifies positive dibits and the HAX circuit rectifies negative dibits. These two output signals are applied to a summing amplifier to generate the track servo signal. When the servo head is centered between servo tracks providing positive and negative dibits, their relative amplitudes are equal. The track servo signal is then at null.

Input A receives the dibit signals. Buffer/driver transistor QN is connected as an emitter follower to provide isolation with a gain of one.

QP and QR are matched transistors in a single can, thus eliminating temperature and offset drifts from the peak detector. The signal passing through QR has the information pulses filtered out of it by NR5, NC3, and NC4 to generate the true base line voltage on output D. This same input signal fed to QR is also given to QP; however, the QP input is not filtered. This allows QP to respond to the highest peak values. Output C is, therefore, a voltage that is the baseline voltage plus the highest positive information peaks. The difference between C and D is the true information.

QS is used to gate out unwanted information. When input B is at +5V, QS is turned off to allow all signals to pass to QP. When input B is at ground, QS is turned off, thus shorting out all information on the base of QP. The waveform illustrates a typical application for the HAW circuit that rectifies the positive dibit signals. Note that the positive peaks of the negative dibits are now allowed to affect the output.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

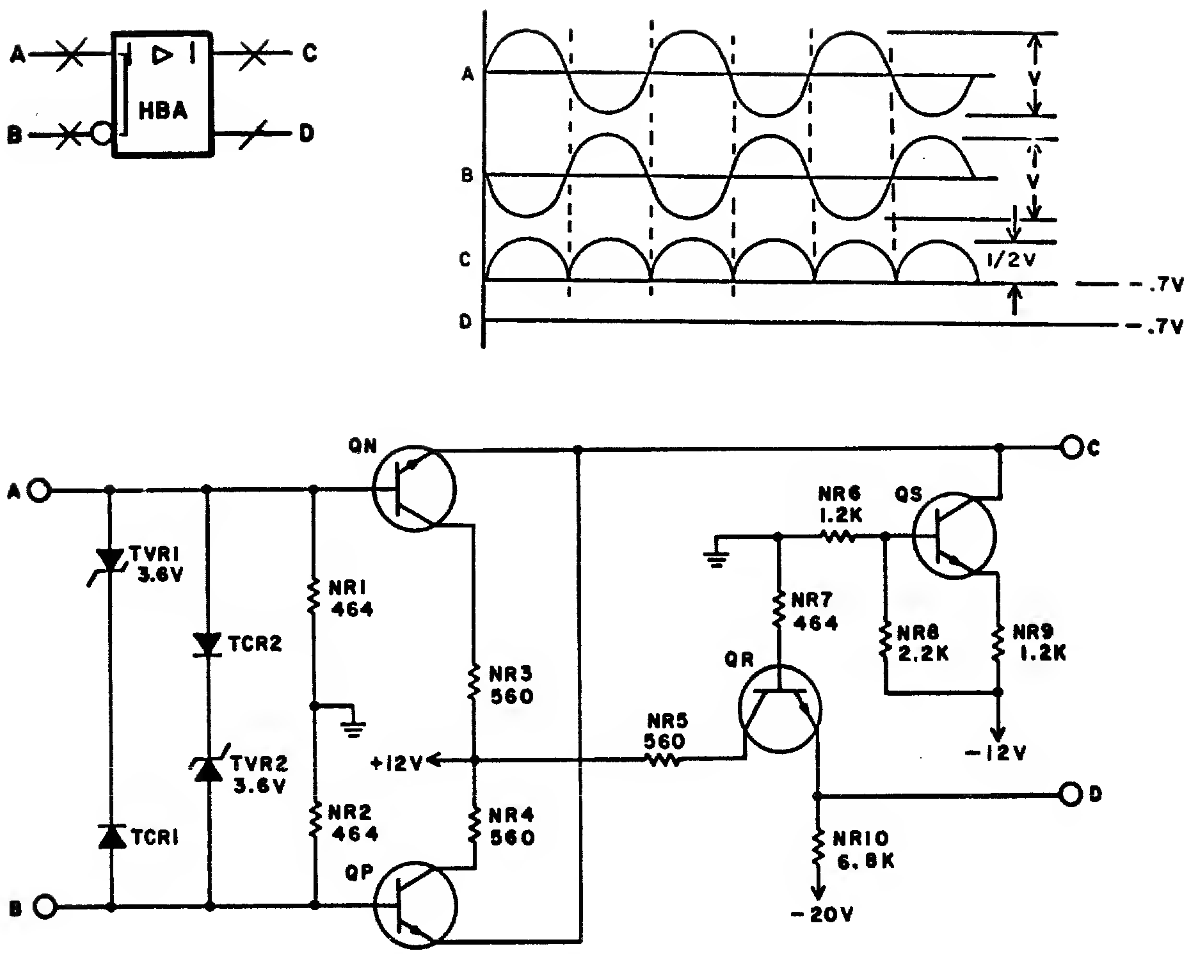
7J193

SUMMING RECTIFIER – HAX

The HAX circuit is identical to the HAW summing rectifier, except that output E and its associated circuitry has been added.

In its typical application, outputs D and E are applied to the inverting and noninverting inputs of an open loop operational amplifier. When the voltage at E is greater than the voltage at D, the op amp output indicates that dibits are being sensed.

NCR1 and NC6 rectify the signal applied to input A. The voltage on NC6 is equivalent to the peak voltage of the positive swing of the dibits. Before dibits are sensed, this voltage is equal to the input baseline voltage minus the diode drops across QN and NCR1. With NR8 and NR9 acting as a voltage divider, output E is less positive than output D. When dibits are sensed, NC6 is charged by the dibits, driving output E to a more positive value.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J104

RECTIFIER - HBA

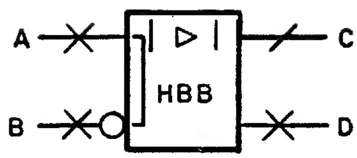
The HBA circuit performs full wave rectification on a differential input signal.

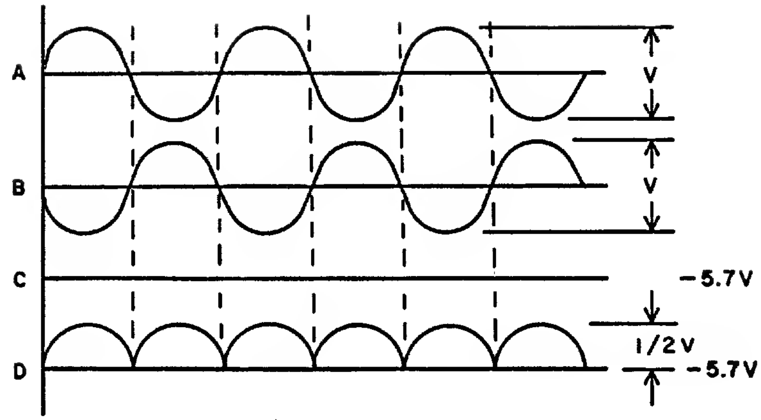
The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at ground potential by NR1 and NR2. With no signal input, point C rests at -.7 volts. NR6, NR8, NR9, and QS form a current sink network which provides the collector-emitter current for QN and QP.

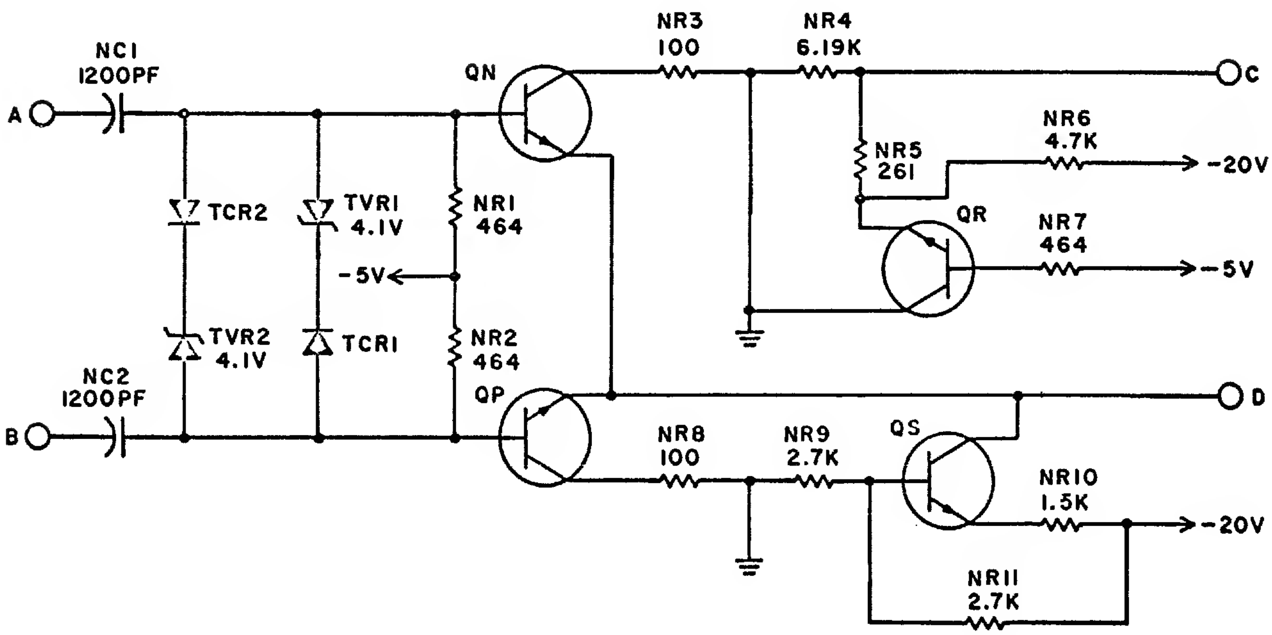
When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point C (waveform C).

Network NR5, NR7, NR10, and QR set up a DC reference voltage at point D which matches the "no signal" DC voltage at point C (QN, QP, and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent over-voltage damage to reverse biased base-emitter junctions of QN and QP.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J103

RECTIFIER - HBB

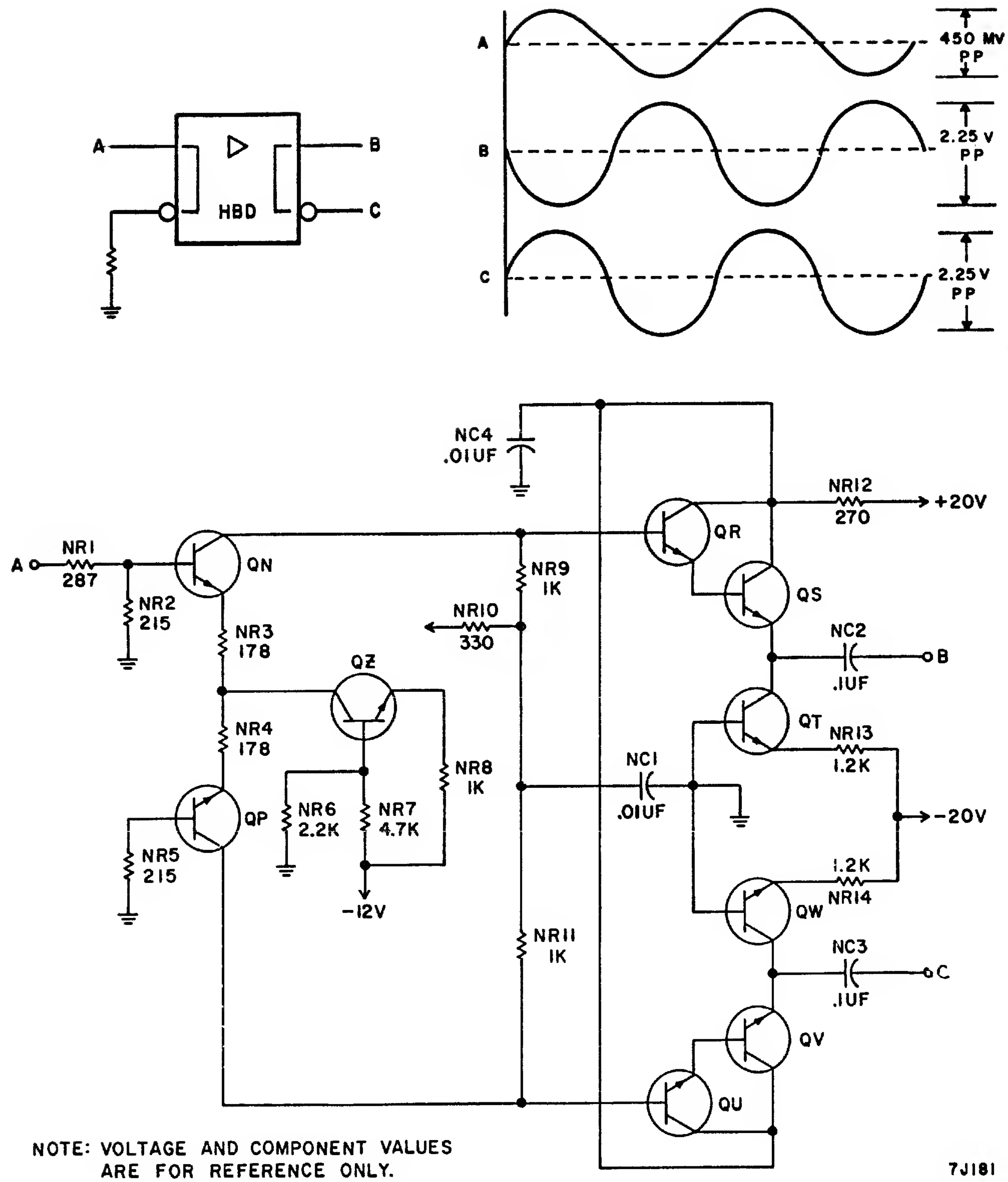
The HBB circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at -5 volts by NR1 and NR2. With no signal input, point D rests at -5.7 volts. NR9, NR10, NR11, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point D (waveform D).

Network NR4, NR5, NR6, NR7, and QR set up a DC reference voltage at point C which proportionally tracks the "no signal" DC voltage at point D (QN, QP and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent overvoltage damage to reverse biased base-emitter junctions of QN and QP.



A
B
C
HBD
450 MV PP
2.25 V PP
2.25 V PP
NC4 .01UF
NR12 270
+20V
NR1 287
NR2 215
QN
QR
QS
NR9 1K
NR10 330
NC2 .1UF
NR3 178
QZ
QT
NR13 1.2K
NR4 178
NR8 1K
NC1 .01UF
-20V
QP
NR6 2.2K
NR7 4.7K
NR5 215
-12V
1.2K NR14
QW
NR11 1K
NC3 .1UF
QV
QU
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
7J181

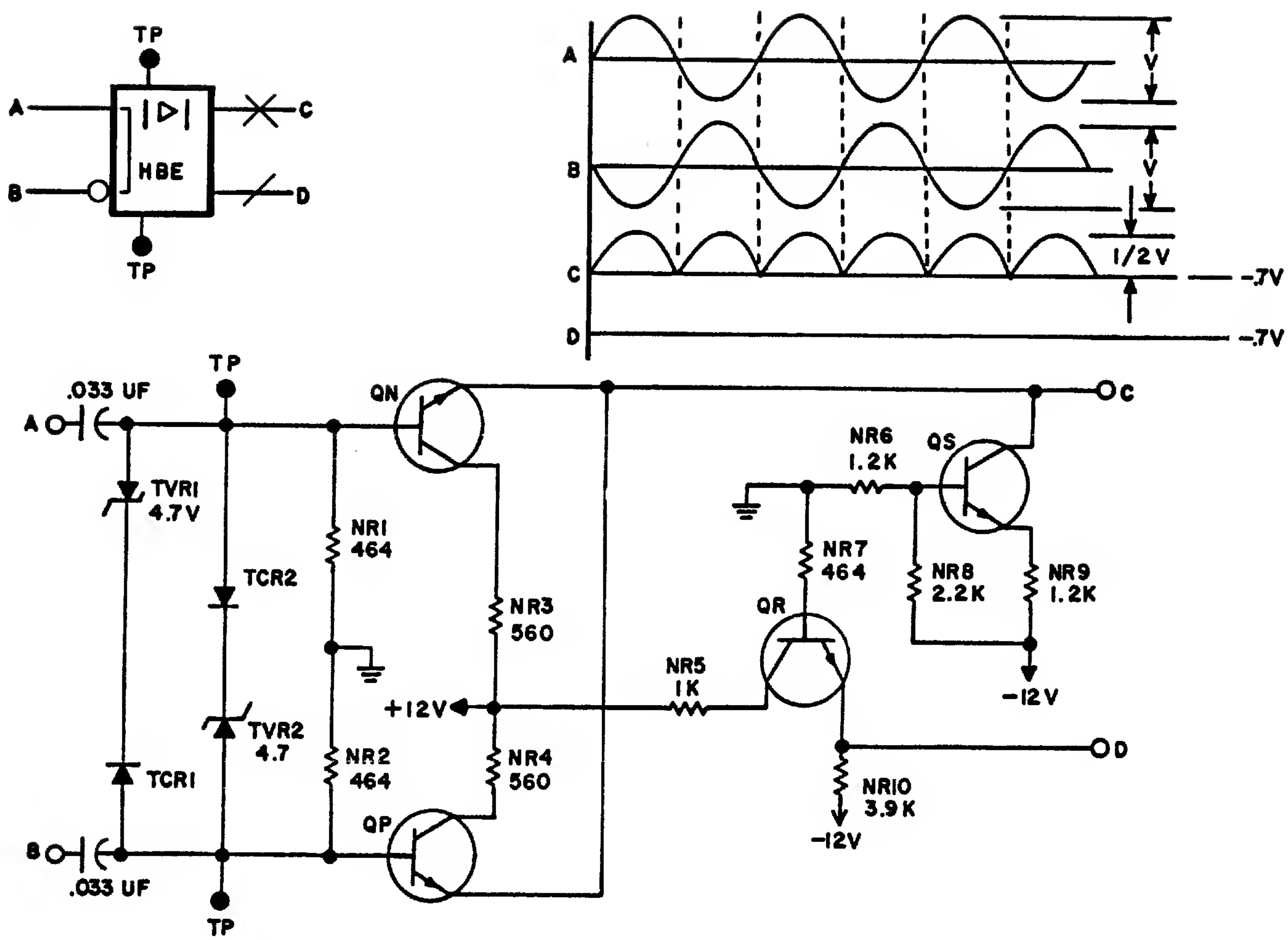
BUFFER AMPLIFIER - HBD

The HBD circuit is a single input, differential output buffer amplifier.

QN and QP are the amplifying transistors. The gain of the circuit is largely determined by the ratio of NR9 to NR3 and NR11 to NR4. Because the base of QP is at ground potential, the voltage at the collector of QP proportionally follows the voltage at the emitter of QN.

QZ, NR6, NR7, and NR8 are a current sink network which provides collector current for QN and QP.

Each output consists of two transistors connected as a common emitter darlington pair (QR and QS, QU and QV) with current supplied from a current sink (QT and QW).



NOTE;

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J148A

RECTIFIER - HBE

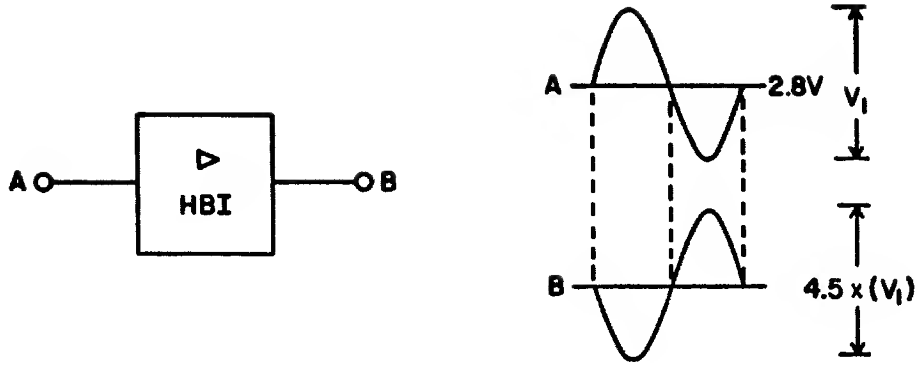
The HBE circuit performs full wave rectification on a differential input signal.

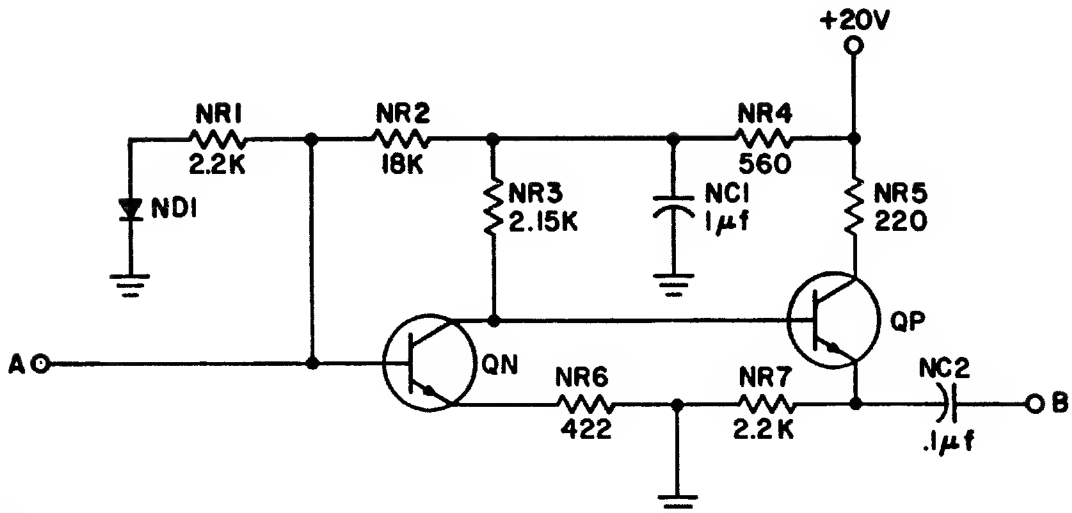
The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at ground potential by NR1 and NR2. With no signal input, point C rests at -.7 volts. NR6, NR8, NR9, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point C (waveform C).

Network NR5, NR7, NR10, and QR set up a DC reference voltage at point D which matches the "no signal" DC voltage at point C (QN, QP, and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent over-voltage damage to reverse biased base-emitter junctions of QN and QP.





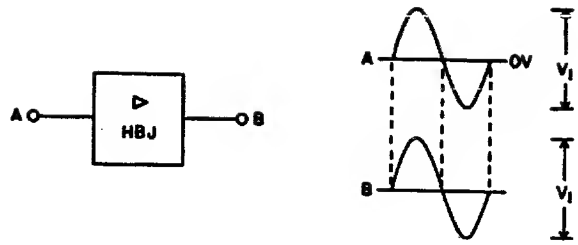
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

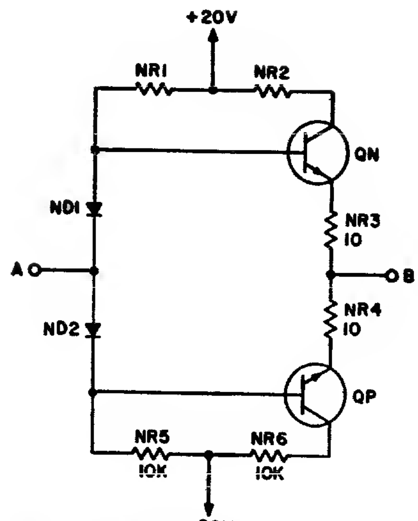
8D48

AMPLIFIER - HBI

The HBI circuit is a low gain amplifier with a fixed gain of 4.5. NR1, NR2, and ND1 form a biasing network for transistor QN. QN is the amplifing transistor with voltage gain determined by the ratio of NR3 to NR6.

Transistor QP is an emitter follower to provide a low output impedance. NC2 is a ac coupling capacitor which provides dc isolation between circuits.





NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

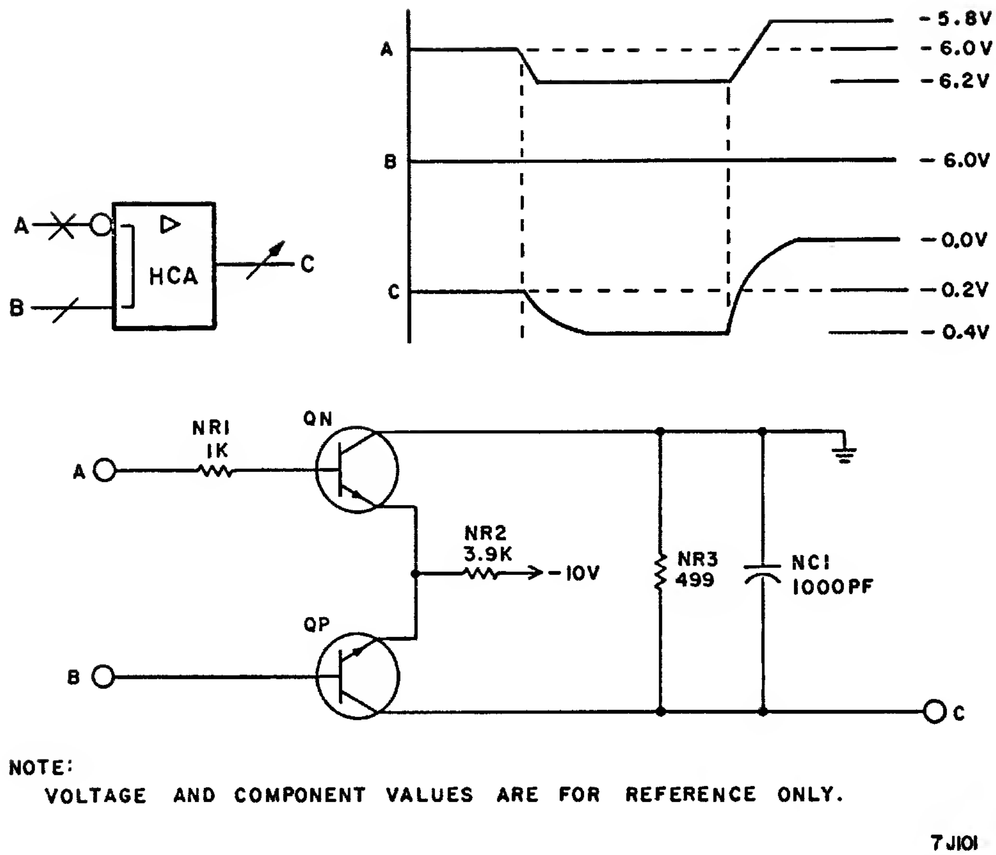
8D47

BUFFER AMP - HBJ

The HBJ circuit is a current/buffer amplifier used for buffering a high impedance output signal source from a low impedance source with an increase in output drive capability.

NR1, ND1, ND2, and NR5 form a biasing network for QN and QP. The voltage drop across the base-emitter junction of QN. Similarly, the voltage drop across ND2 compensates for the voltage across the base-emitter junction of QP.

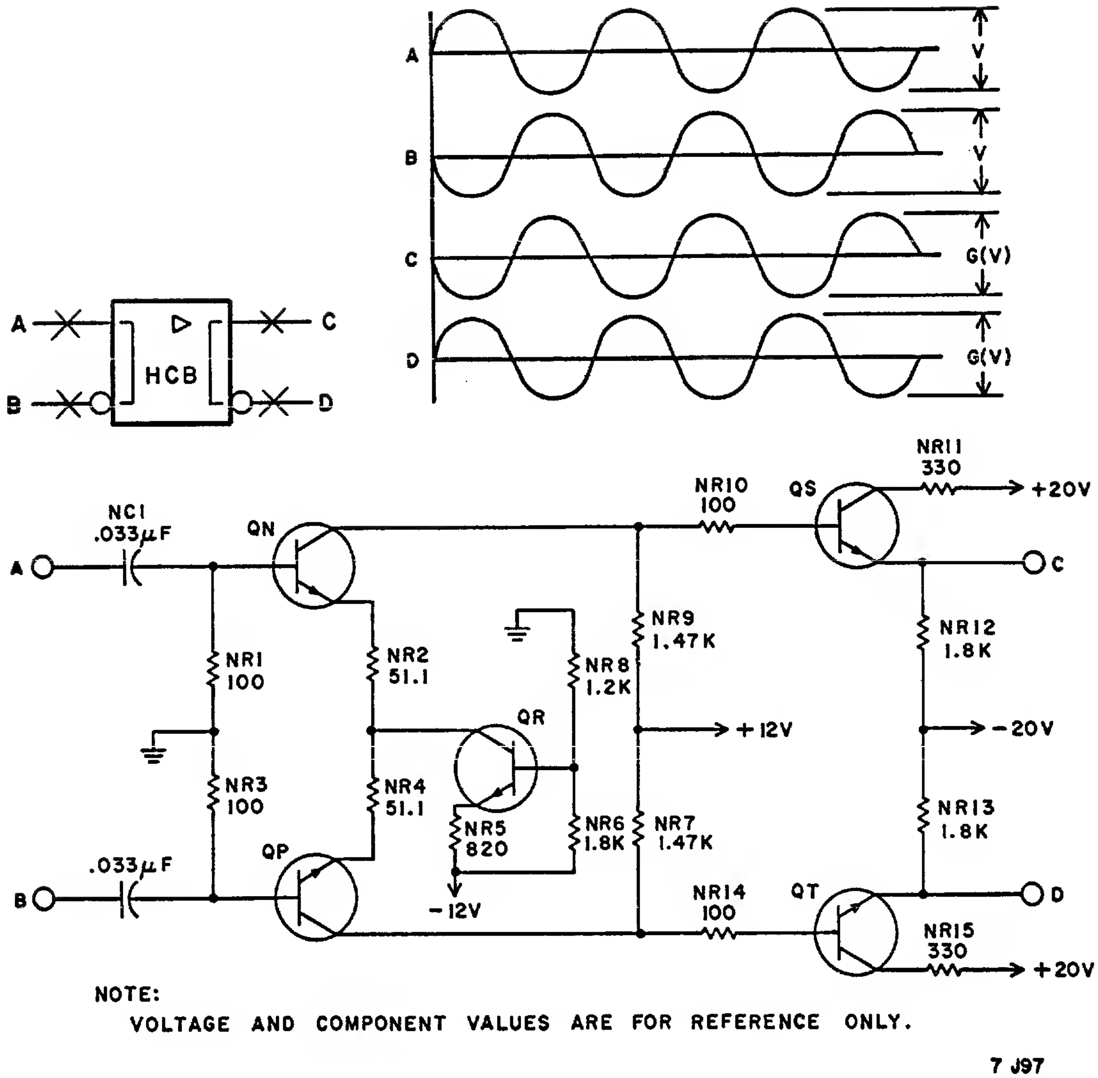
The biasing networks of QN and QP allow the voltage level at output B follows the voltage level at input A.



DIFFERENTIAL AMPLIFIER - HCA

The HCA circuit is a differential amplifier which is used as a control element in an AGC amplifier feedback loop.

Input B is connected to a fixed reference voltage and input A is connected to an integrated DC voltage which is proportional to the output amplitude of an AGC amplifier. When the voltage on input A is greater than that at input B, the current from emitter resistor NR2 goes through QN to ground. When the voltage on input A is less than at B, the current from NR2 goes through QP to output C. When input A equals input B, the current from NR2 is split between QN and QP. The voltage at point C is established by the current through QP times resistor NR3. Point C is the control voltage input for input E on the HCU (AGC amplifier) circuit. NC1 is used as an integrator and helps stabilize the response time.



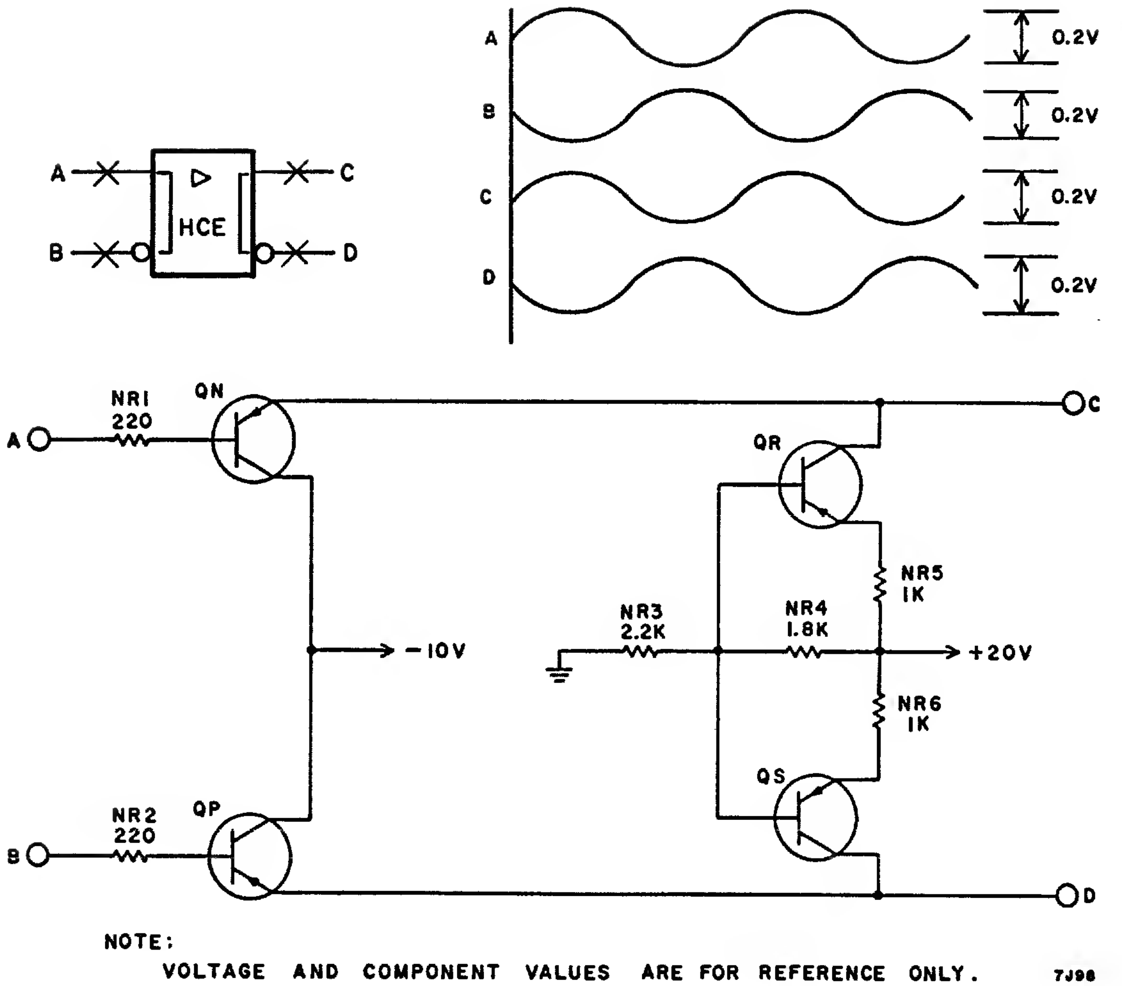
DIFFERENTIAL AMPLIFIER - HCB

The HCB circuit is a single stage differential input, differential output amplifier.

QN and QP are the amplifying transistors. The gain of the amplifier is largely determined by the ratio of NR9 to NR2 and NR7 to NR4.

QR, NR5, NR6, and NR8 are a current sink network which provides collector current for QN and QP.

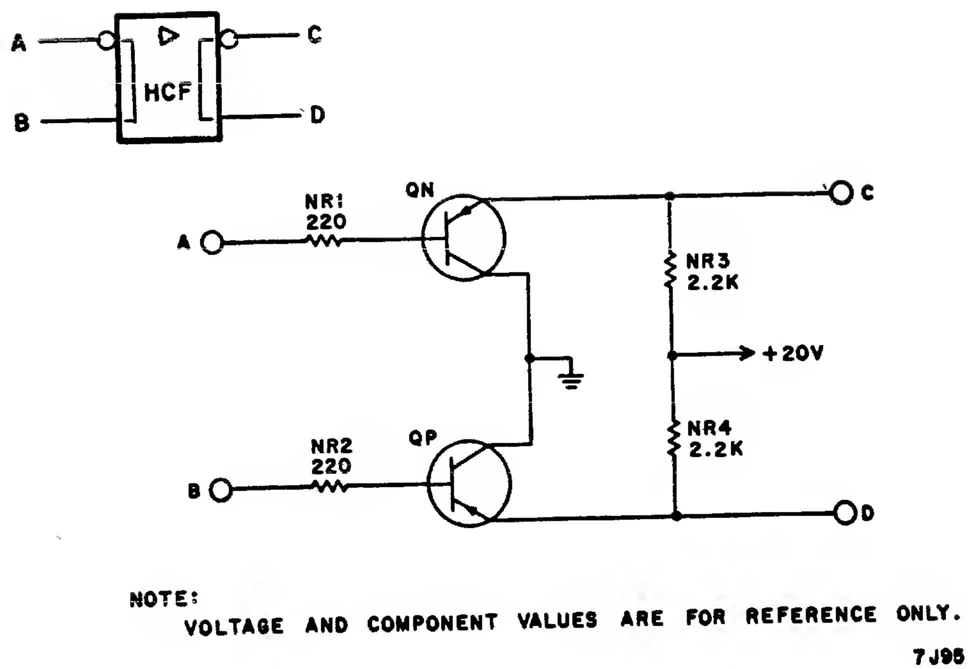
QS and QT with emitter resistors NR12 and NR13 are emitter followers for low impedance outputs.



BUFFER AMPLIFIER – HCE

The HCE circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

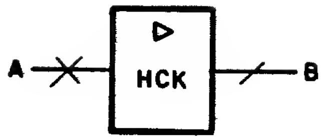
Emitter followers QN and QP present comparatively high input impedance at A and B, and low output impedance at C and D. Current sources QR and QS with NR3, NR4, NR5, and NR6 supply constant emitter current to QN and QP.

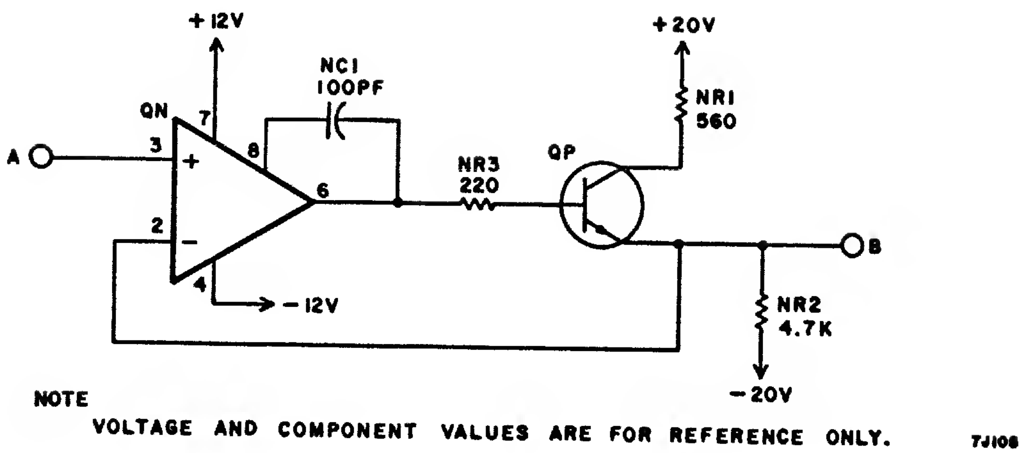


BUFFER AMPLIFIER – HCF

The HCF circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

QN and QP are emitter followers which present comparatively high input impedance at A and B, and low output impedance at C and D.

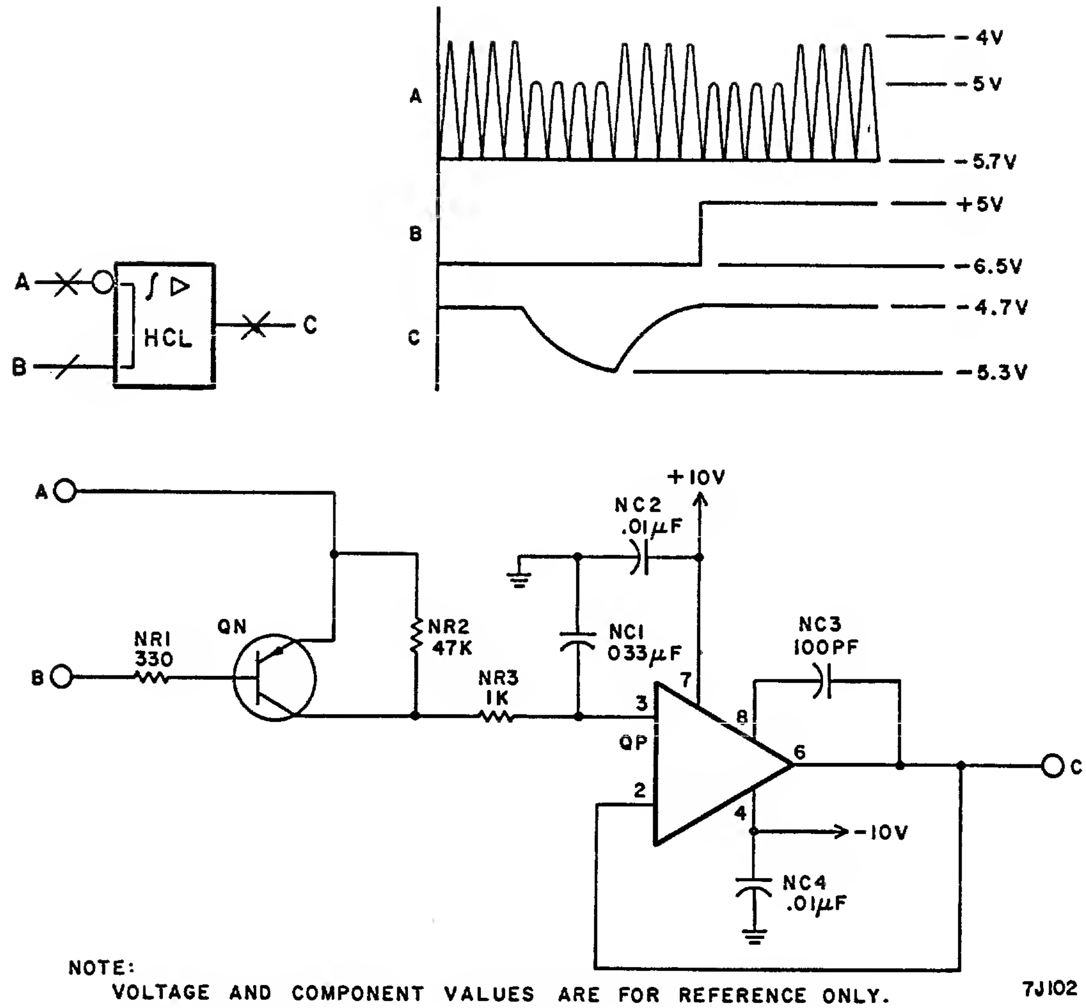




VOLTAGE FOLLOWER – HCK

The HCK circuit consists of an operational amplifier in a voltage follower configuration. An NPN emitter follower (QP) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QP in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QP.

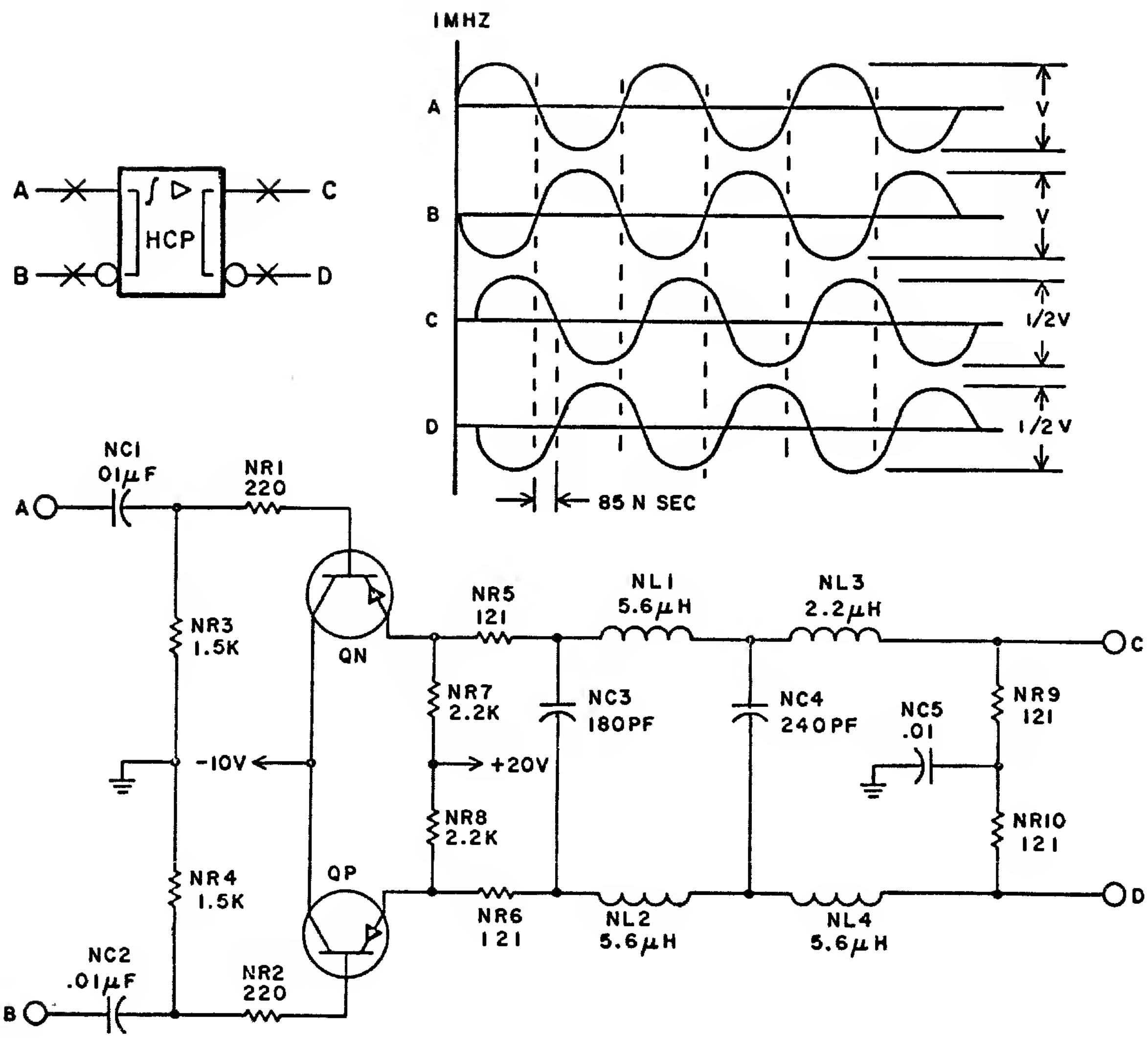
NR2 provides a minimum load current for QP under no output load conditions. NR1 is a current limit resistor. Resistor NR3 and capacitor NR1 stabilize the circuit.



INTEGRATING AMPLIFIER - HCL

The HCL circuit converts a rectified signal input to a DC output that is an average value of the input signal waveform.

The integrating elements are NR2, NR3, and NC1. The analog signal (recrified waveform) is entered at input A. With digital voltage control at input B, QN can be turned on which would bypass NR2. This would leave (NR3) X (NC1) to determine the relatively short response time of the integrator. When QN is turned off, NR2 is included in the integrating circuit and the (NR2 + NR3) X (NC1) long response time results. QP (element 531) is an operational amplifier connected in a voltage follower mode of operation and acts as a buffer amplifier. NC3 is a compensation capacitor for QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J106

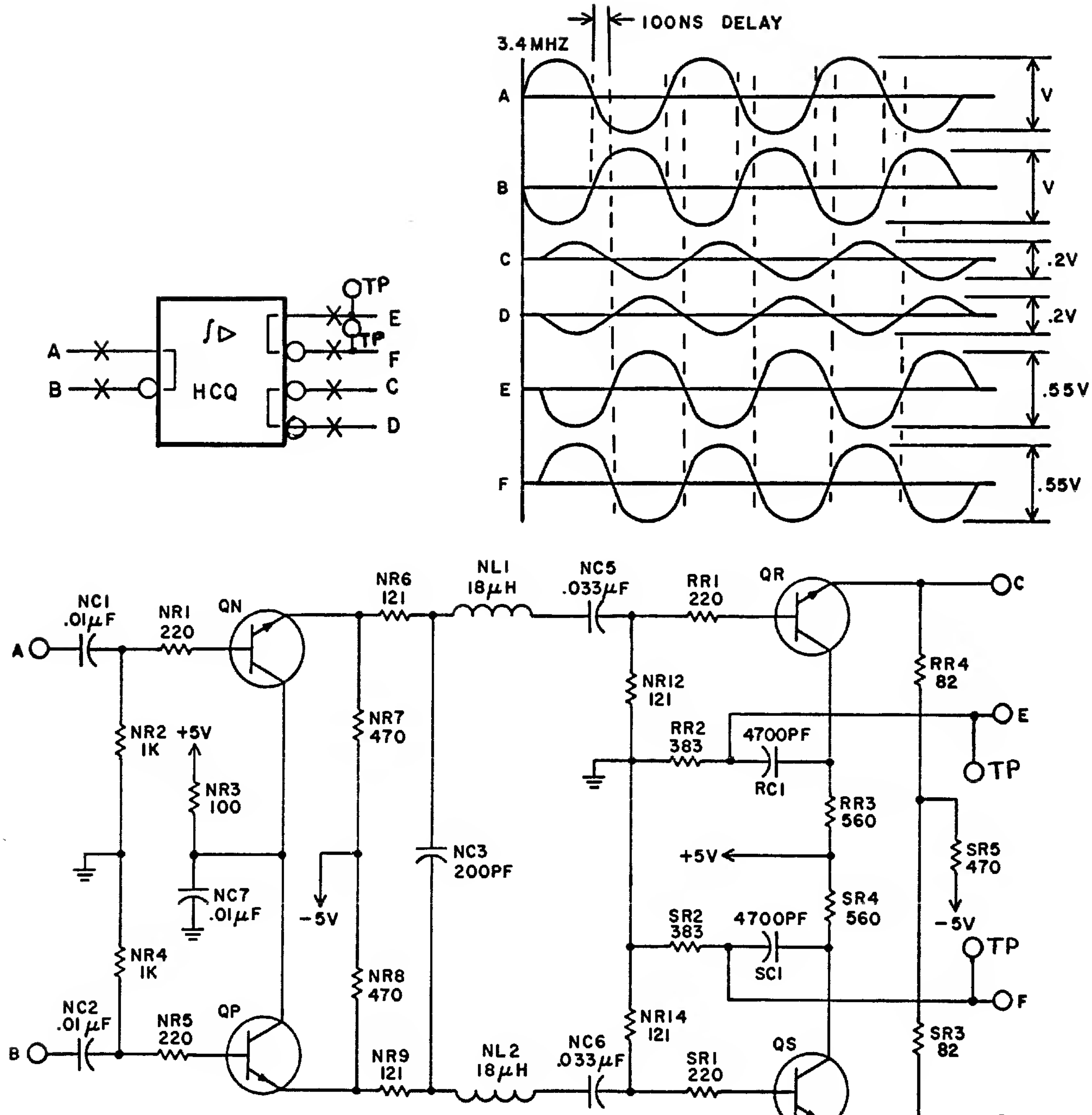
LOW PASS FILTER - HCP

The HCP circuit is a low pass differential filter with a buffer amplifier input (emitter followers). The filter provides attenuation of high unwanted frequencies (noise) in the read back signal with a linear phase response over the frequencies concerning read data.

NL1, NL2, NC3, NC4, NL3, and NL4 make up the differential filter with outputs at C and D. NR9 and NR10 are terminating (impedance-matching) resistors for the filter. NR5 and NR6 are impedance matching resistors to the input of the filter.

QN and QP with their emitter and base resistors form the buffer amplifiers for driving the relatively low input impedance filter.

The upper cutoff frequency of the filter is approximately 5.5 MHz (media compatible data rate of 6.44 MHz). The signal attenuation from inputs A, B, to outputs C, D is about 50% at 1 MHz.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J112A

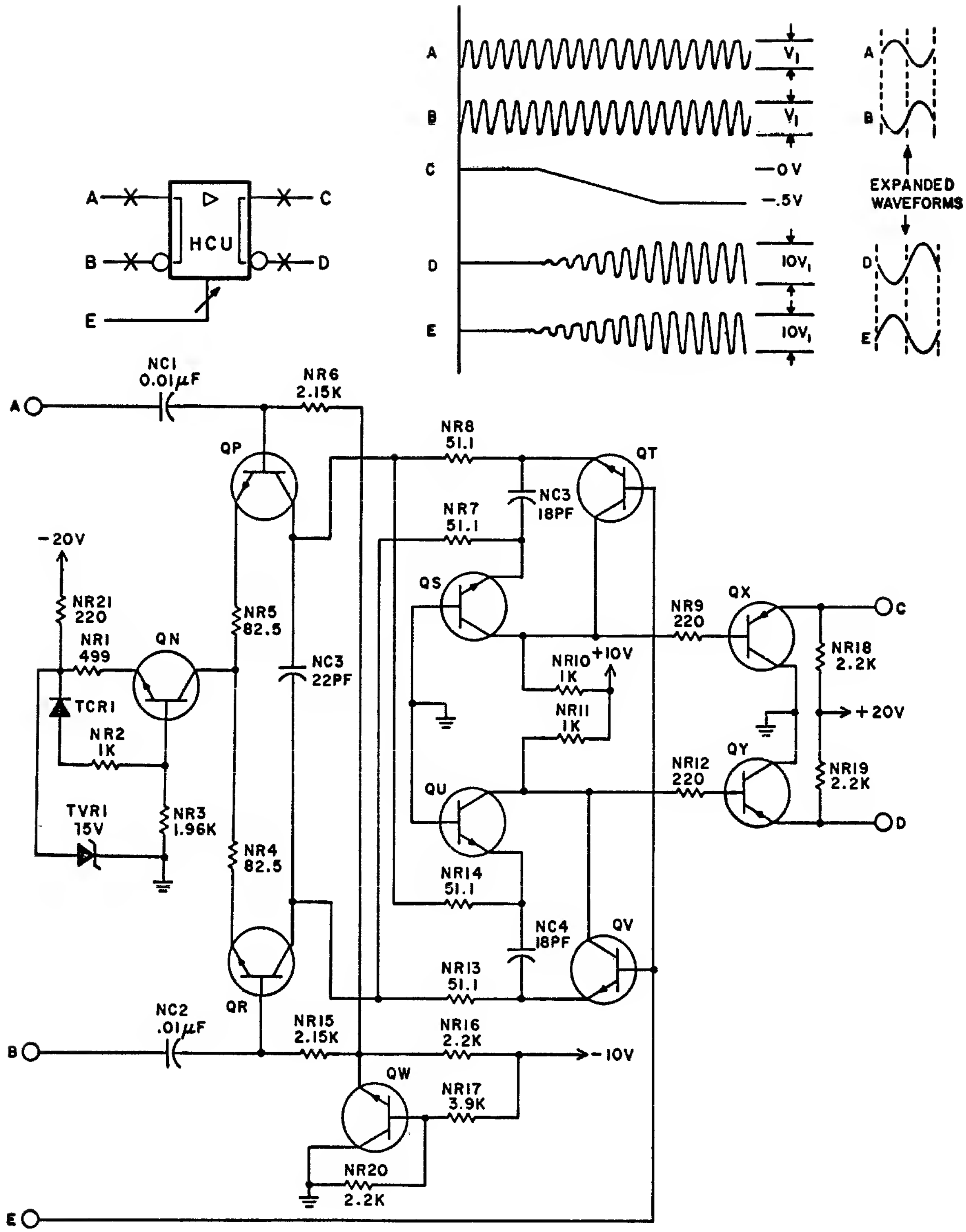
FILTER AND AMPLIFIER - HCQ

The HCQ circuit is a differential, 2 pole low pass filter followed by a differential amplifier with a gain of approximately 2.5.

NL1, NC3, and NL2 make up the 2 pole low pass filter. The upper cutoff frequency is approximately 2.5 MHz for media compatible data rate (6.44 MHz). NR6, NR9, NR12 and NR14 are impedance matching resistors for the filter.

QN and QP are buffer amplifiers (emitter followers) for driving the relatively low impedance filter.

QR, QS, and their associated circuitry perform dual roles as differential buffer amplifiers (emitter followers) and as differential amplifiers. Outputs C and D are the buffered outputs that connect to level detection circuitry with further amplification. Outputs E and F are amplified outputs which connect to a zero cross network (low resolution channel). This signal channel is amplified to make up for the attenuation loss of the filter. The gain of the amplifier is largely determined by the ratio of RR2//RR3 to RR4 and SR2//SR4 to SR3.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J1158

AGC AMPLIFIER - HCU

The HCU circuit is a differential amplifier with gain controlled by a negative voltage at input E.

QP and QR are amplifying transistors with their maximum gain determined by the ratio of NR10 to NR5 and NR11 to NR4.

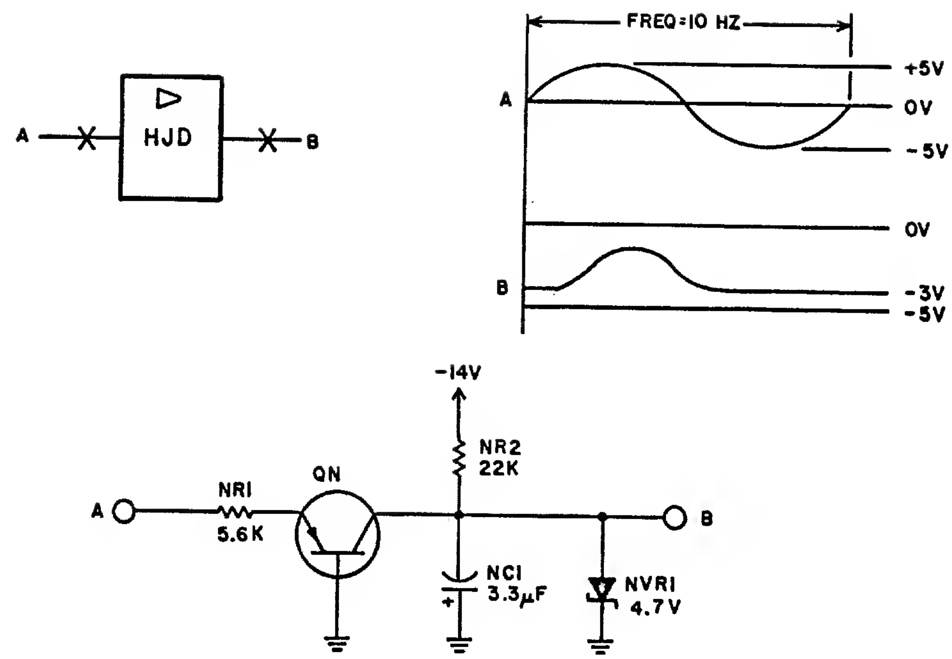
Common base amplifiers, QS, QT, QU, and QV pass amplified current signals to resistors NR10 and NR11. QS and QT pass out of phase signals to collector resistor NR10. Likewise, QU and QV pass out of phase signals to collector resistor NR11.

Control voltages on the bases of QT and QV control circuit gain. With 0 volts for control voltage, QS, QT, QU, and QV turn on equally, causing out of phase voltage to cancel, leaving a net output or gain of 0 volts. Increasing the control voltage negatively starts turning off QT and QV causing the amplifier gain to increase. Turning off QS, QT, QU, and QV requires that the control voltage be approximately -0.5 volts, which allows an amplifier gain of 10.

Emitter followers QX and QY provide low output impedance.

QN, NR1, NR2, NR3, and TCR1 make up a current sink network which controls the collector current of QP and QR.

NR21 and TVR1 form a -15 volt regulated voltage for the current sink circuit.



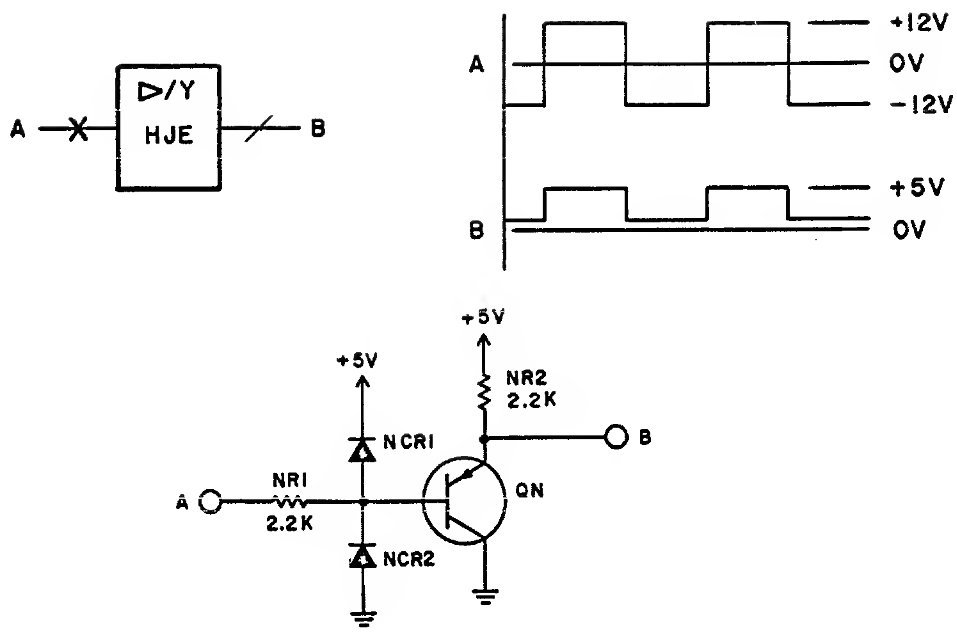
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY

6T167A

AMPLIFIER/LEVEL TRANSLATOR - HJD

The HJD circuit is an amplifier that provides a half-wave rectifier, shifted output signal.

The output signal at B increases in a positive direction from a -3 vdc level. The output signal controls a N-channel JFET in an AGC loop that regulates the amplitude of the fine position servo signal.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

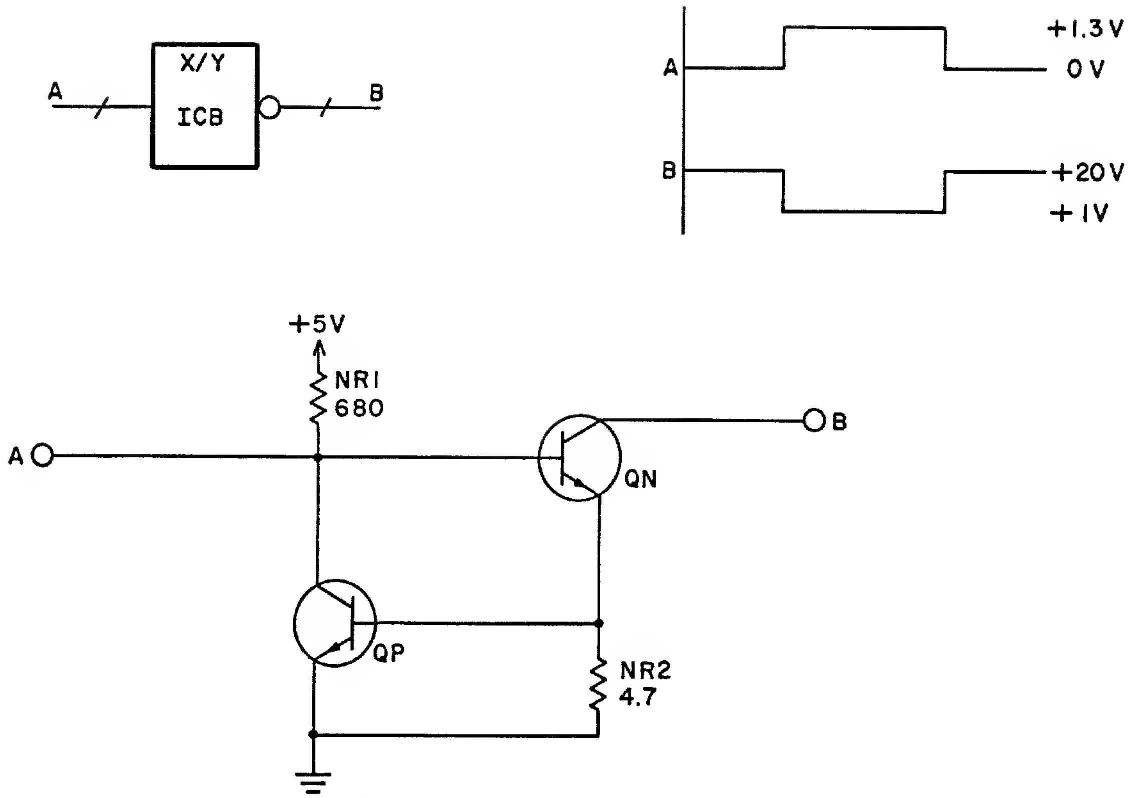
6T166A

LEVEL TRANSLATOR - HJE

The HJE circuit converts the output of an operational amplifier to a standard logic level.

When input A is at -12 volts, transistor QN is on. Diode NCR2 limits the input voltage at the base of QN to approximately -0.7 volt. Since the base to emitter voltage of QN is +0.8 volt, output B is at a level of approximately +0.1 volt.

When input A switches to +12 volts, QN becomes reverse biased and output B approaches +5 volts. The base voltage of QN is limited to approximately +5.7 volts by diode NCR1.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T148

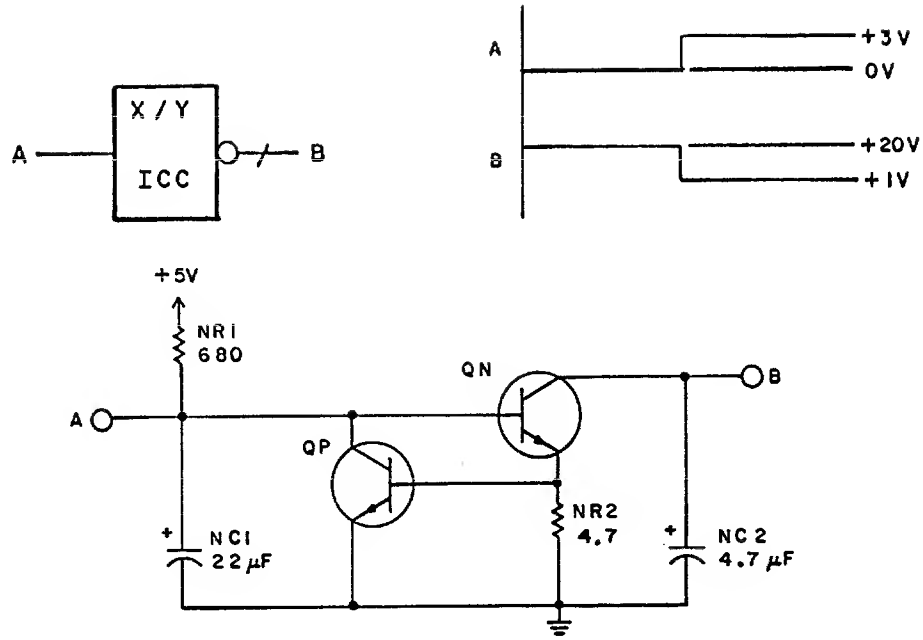
LAMP DRIVER - ICB

The ICB circuit drives a lamp which terminates at +20 volts. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

QP and NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

When a high, logic 1, is provided to the circuit input, transistor QN (and the lamp) turns on.

A low (logical 0) at the input turns QN off causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off.



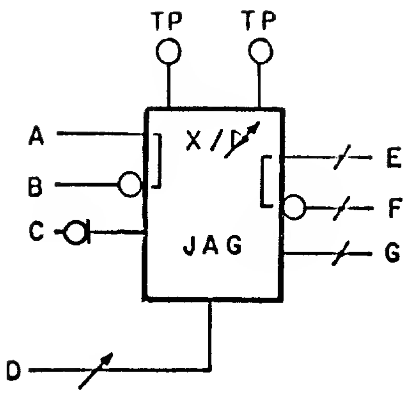
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J25

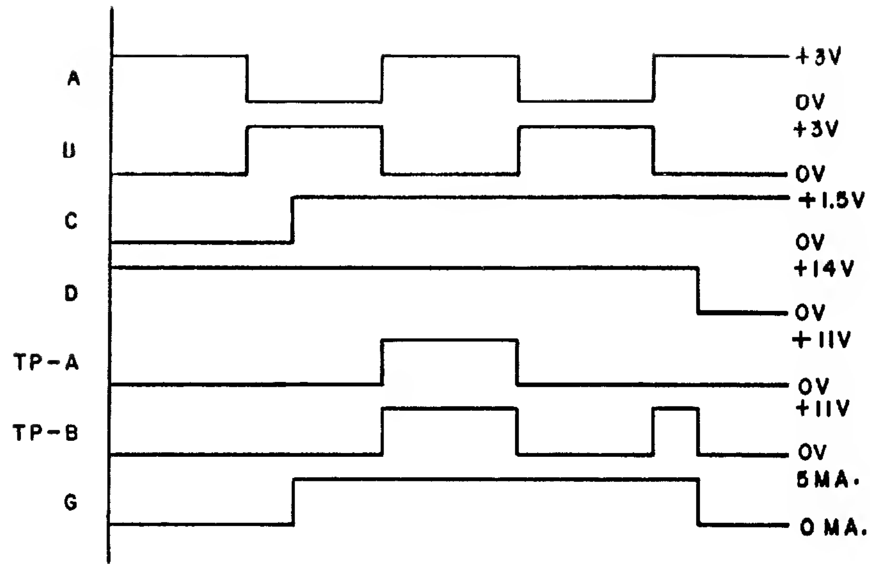
LAMP DRIVER - ICC

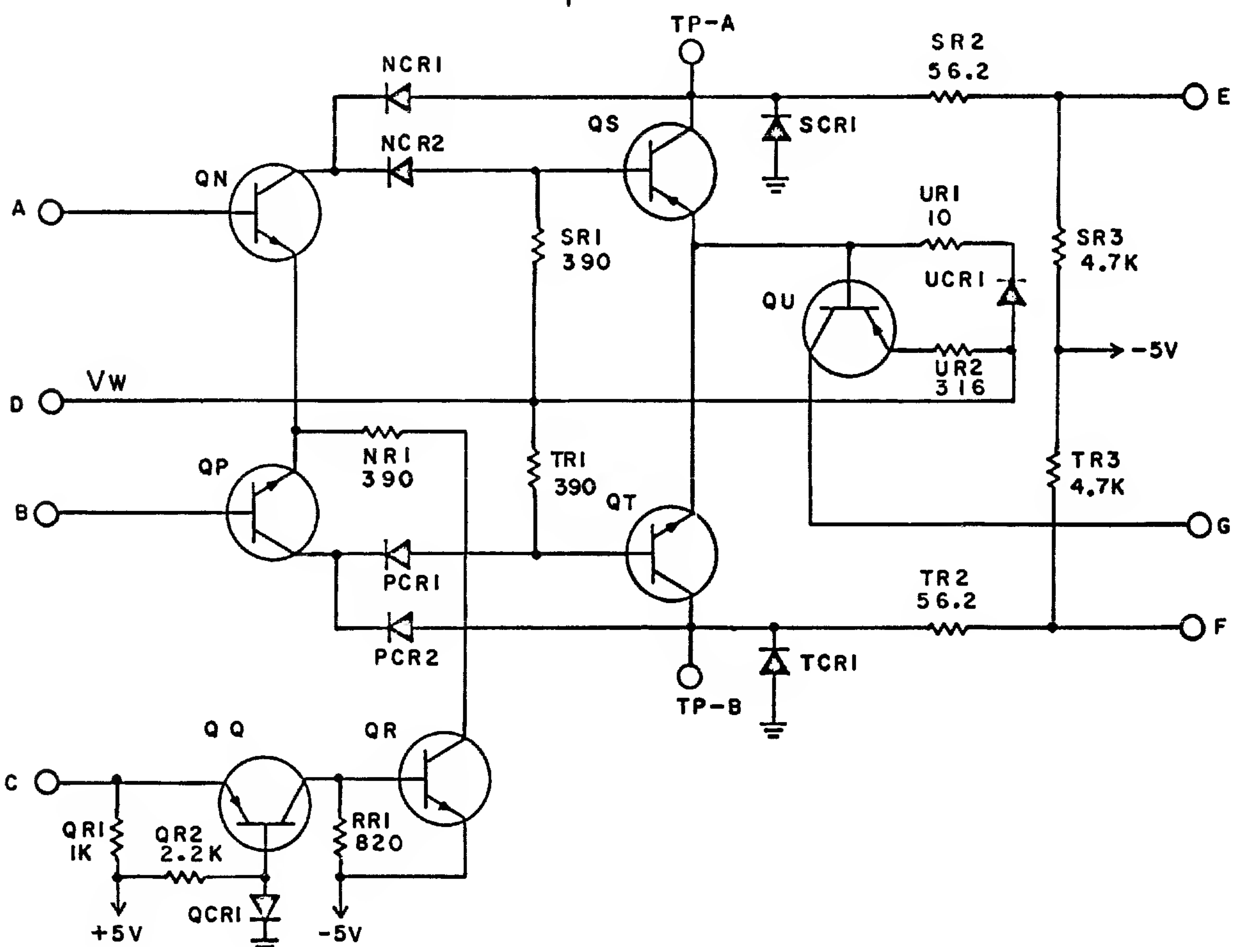
The ICC circuit drives a lamp which terminates at +20 volts. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

When a high, logic 1, is provided to the circuit input, transistor QN (and the lamp) turns on. Transistor QP and resistor NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

A low, logic 0, at the input, turns QN off causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off. Capacitors NC1 and NC2 are used to slow the rise and fall times of the output voltage swings at B.







NOTE:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

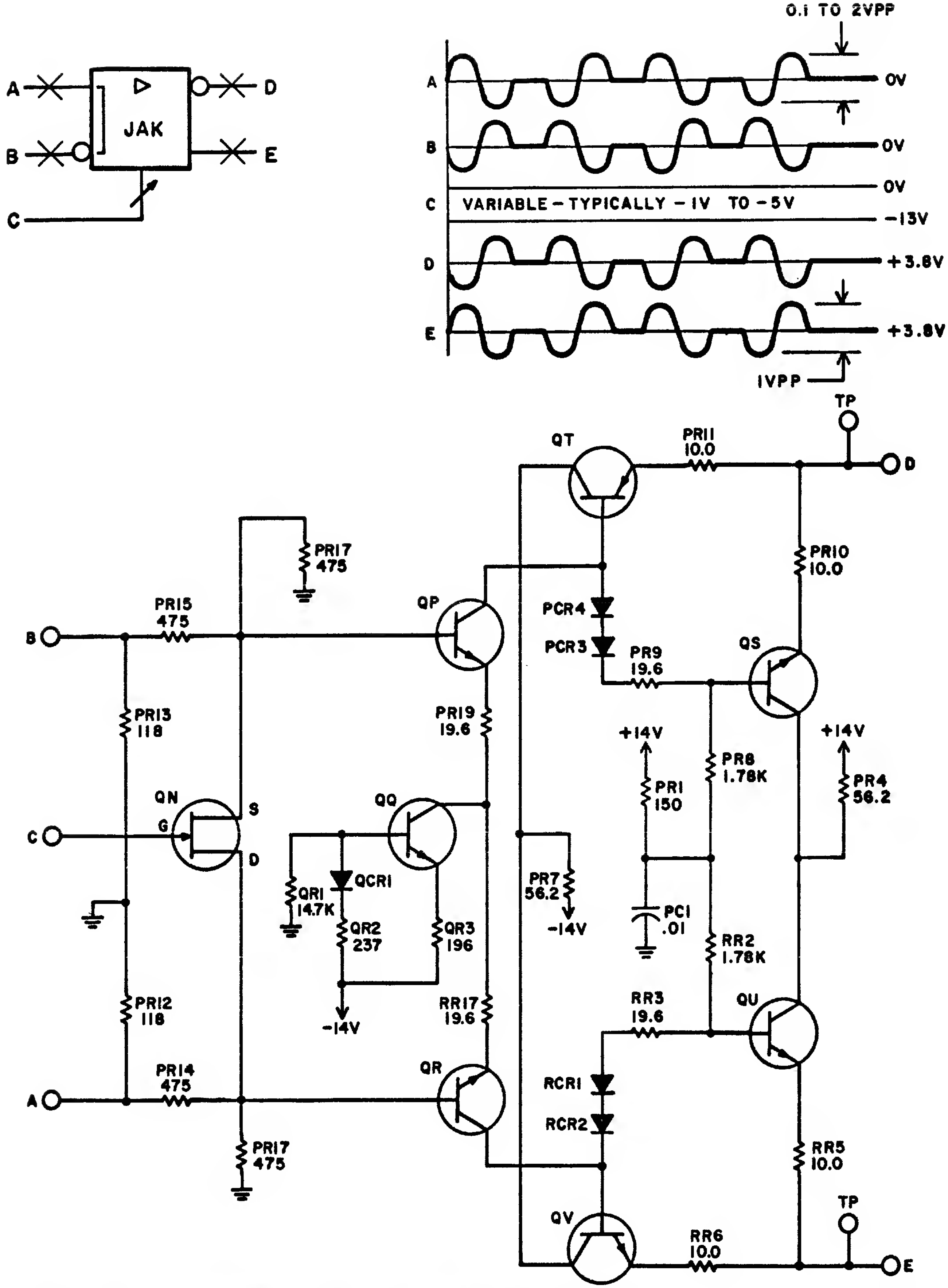
7J26

2. WAVEFORMS ABOVE ARE FOR REFERENCE ONLY AND VALID ONLY WHEN OUTPUTS E AND F ARE CONNECTED TO A READ/WRITE HEAD WITH CENTER TAP TO GROUND.

WRITE DRIVER - JAG

Write driver JAG is a differential voltage switch which converts voltage (across termination resistors) to current to drive a differential recording head.

Circuit operation is dependent upon signal level shifter QQ converting an open collector TTL output of "0" or "1" to turning QR "off" and "on". With QR on, -5 volts flows through QR and NR1 to supply current for the differential switches QN and QP. With input A high and B low, QN turns on and QP is off. QN turning on causes QS to turn on which applies a voltage (from D through UCR1 and UR1) to termination resistor SR2 and current to output E. When A is low and B is high QN and QS turn off, QP and QT turn on applying voltage to termination resistor TR2 and current to output F. Current sensing network UR1, UR2, UCR1 and QU supply current at G which is used for fault detection. NCR1, NCR2, PCR1, PCR2 prevent QS and QT from saturating when the write driver is turned off. SCR1, SR3, TCR1, and TR3 provide back biasing of the write matrix diodes during a write operation.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J107

AGC AMPLIFIER – JAK

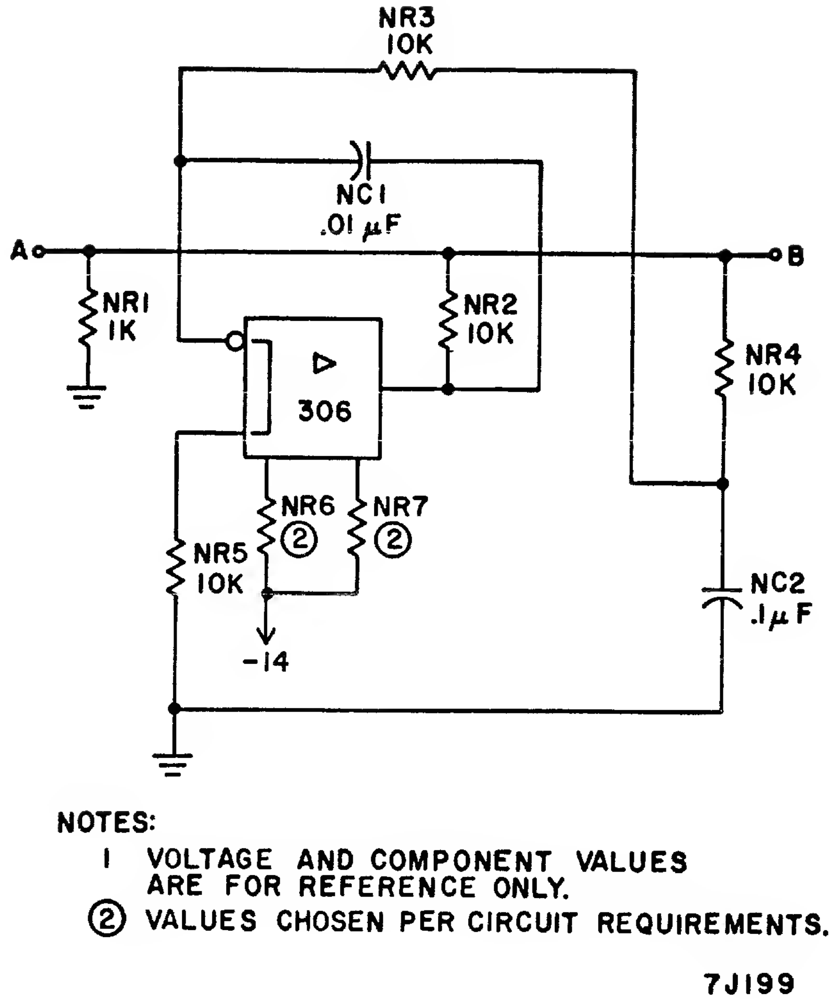
The JAK circuit amplifies the differential dibit signal read from the servo head. This AGC amplifier is a differential in, differential out amplifier with a variable input attenuator.

The differential signals are applied to inputs A and B. Resistors PR12 and PR13 are line terminating resistors.

AGC action is provided by input C. This control voltage, generated farther down the servo signal chain, is proportional to the amplitude of the dibit signals. The stronger the signal, the less negative the AGC voltage. Resistors PR15, PR17, PR14, and PR16, along with N-JFET QN form a balanced differential attenuator. The more negative the input, the greater the effective source-to-drain resistance across QN. This reduces the attenuation of the network. The voltages available at C can vary from 0V to -13V. At 0V, the D-S resistance is about 40 ohms; practically shorting out the input to reduce the net gain available. At -13V, the D-S resistance is about 50 megohms, permitting full gain. In actual practice, the servo action of the loops holds input C at about -1V to -5V.

Transistors QP and QR form the inputs to a differential amplifier. Transistor QQ functions as a high-resistance common current source; diode QCR1 provides temperature compensation. The resultant constant-current source greatly reduces common mode error.

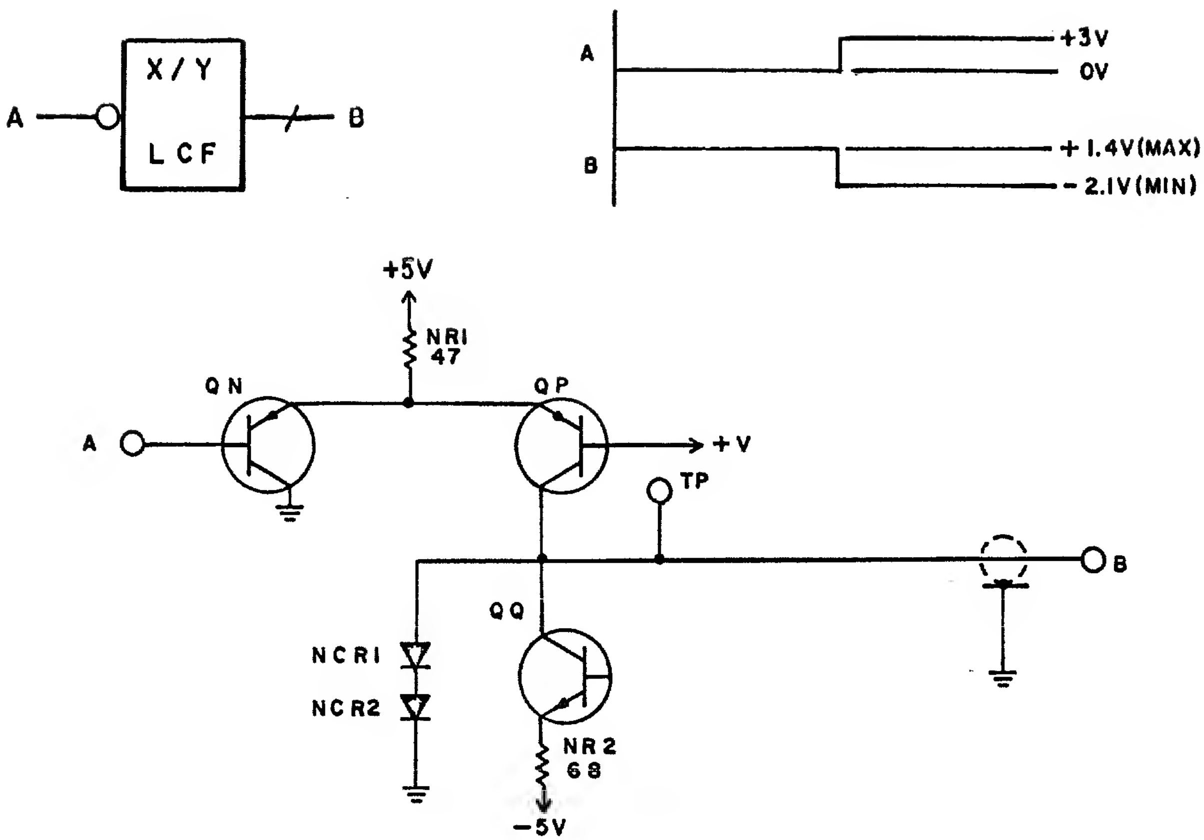
Transistor pairs QS/QT and QU/QV form unity-gain, noninverting power drivers for outputs D and E.



Auto Null Circuit – JAM

The JAM circuit provides a DC null for the AC signal on line AB. This circuit compensates for a fluctuation in DC reference of the AC signal due to temperature and chip-to-chip parameters.

The operational amplifier senses the DC level on line AB and compares this voltage level against a zero volt reference. It then supplies the proper DC current to maintain a DC null on line AB.

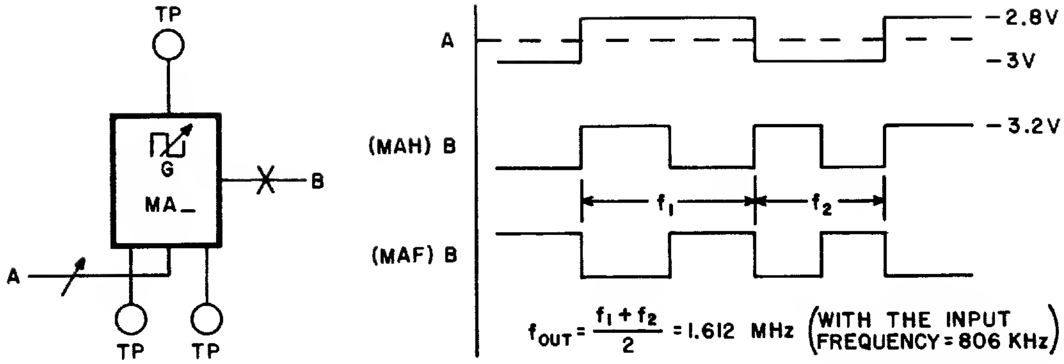


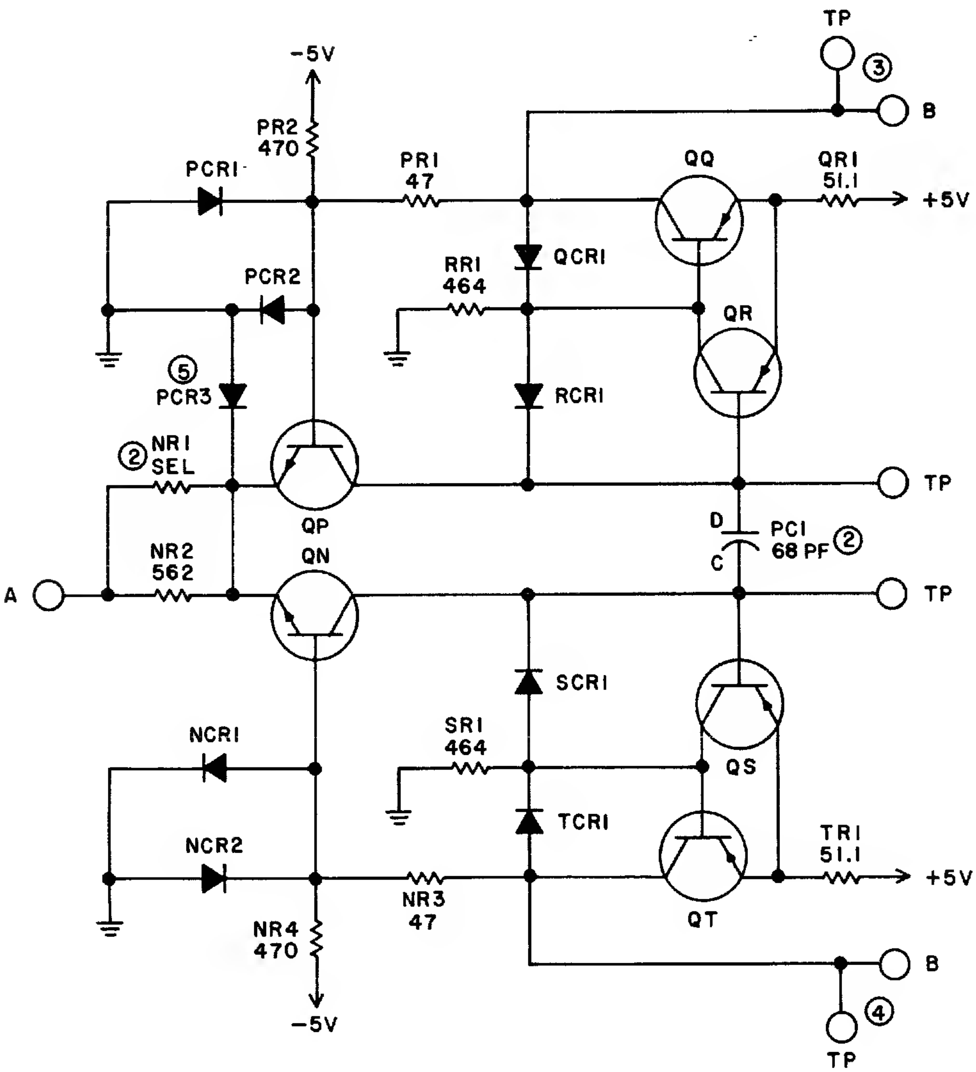
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J27

TRANSMITTER - LCF

The LCF circuit provides a sink current at output B when the input at A is low. When the input is high, the output current becomes a source current. Input A is driven by a standard TTL logic gate. Resistor NR1 and transistors QN and QP operate as a switch. When the voltage at A goes below +V, transistor QN turns on and QP turns off. The constant current circuit, QQ and NR2, sinks current through the line and terminator and drives the voltage at the collector of QQ negative. External resistors and Zener diodes between the plus and minus voltage supply lines serve as a voltage divider common to all LCF circuits on a given card and provide bias voltage to the bases of QP and QQ. The sink current level is determined by -V, VBE of QQ, and NR2.

When the voltage at A goes above +V, transistor QN turns off and QP turns on. A source current is now developed by +V, VEB of QP, and NR1. The current level is such that it is greater than the sink current into QQ by an amount sufficient to drive the output positive. This positive voltage excursion is limited by diodes NCR1 and NCR2. Limiting is necessary to keep QP from saturating. Because of the nonsaturating mode of operation, the propagation delay through LCF is small. Accidental grounding of the test point or output of the circuit has no damaging effect on the circuit.





NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. VARIES WITH DATA FREQUENCY. THESE COMPONENTS CONTROL FREQUENCY.
3. OUTPUT LOCATED ON MAH CIRCUIT.
4. OUTPUT LOCATED ON MAF CIRCUIT.
5. DIODE PCR3 ON MAH ONLY.

7J28A

VOLTAGE CONTROLLED OSCILLATOR - MAF/MAH

The MAF/MAH circuit consists of two Schmitt trigger circuits (QQ, QR and QS, QT) and a differential switch/current limiter circuit (QN, QP, NR1, AND NR2). The values of capacitor PC1, resistors NR1 and NR2, and the input voltage, determines the output frequency of the circuit. Operating frequency is listed on the Logic Diagram (see Section 5).

For the following discussion, assume that voltage E3 is more positive than E2, E2 is more positive than E1, and E0 is the lowest voltage (refer to Figure 1).

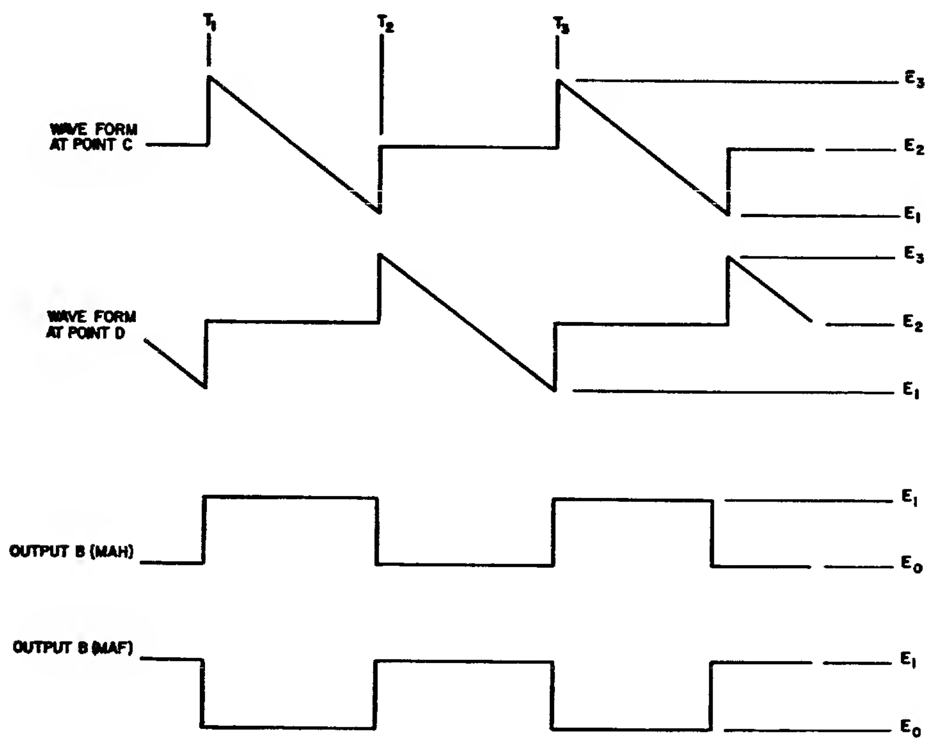


Figure 1

Assume that point C of PC1 is more positive than point D. At this time, QP and QS are both conducting and QT is off (base-emitter junction is reverse biased). The output voltage at B is high. The other half of the circuit (QN, QQ, and QR) is in the opposite state at this time.

The D terminal of capacitor PC1 is held low by the forward drop of the base-emitter junction of QR. Therefore, current through PC1 alters its charge linearly until the voltage at C reaches the high output voltage. At this point, the lower Schmitt trigger circuit (QS, QT) switches off and the output voltage at B goes to ground. QP now switches off and point C is driven rapidly positive by the forward biased base-emitter junction of QS.

At the instant that the lower Schmitt trigger circuit switched off, the voltage at point D was at E3. The sudden increase of point D to E3 potential reverse biases the base-emitter junction of QR and triggers the upper Schmitt trigger circuit. Therefore, QN and QQ turn on and draw current from terminal D of capacitor PC1. When the voltage at D reaches E1, the upper Schmitt trigger circuit switches off. QN switches off and point C is again raised to E3. This completes the multivibrator cycle and brings it back to the initial condition. The cycle is then repeated.

As input A becomes more negative the output frequency at B, increases linearly (refer to Figure 2).

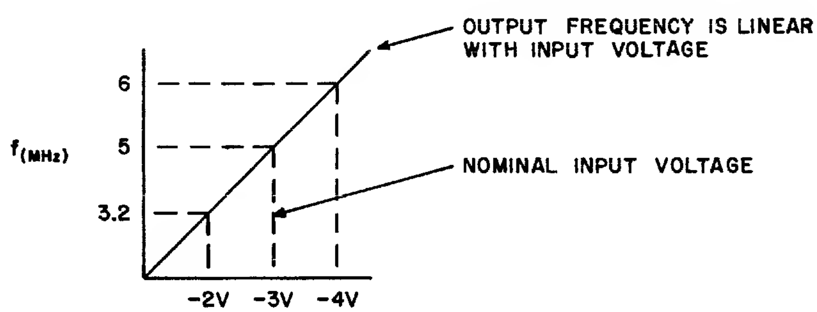
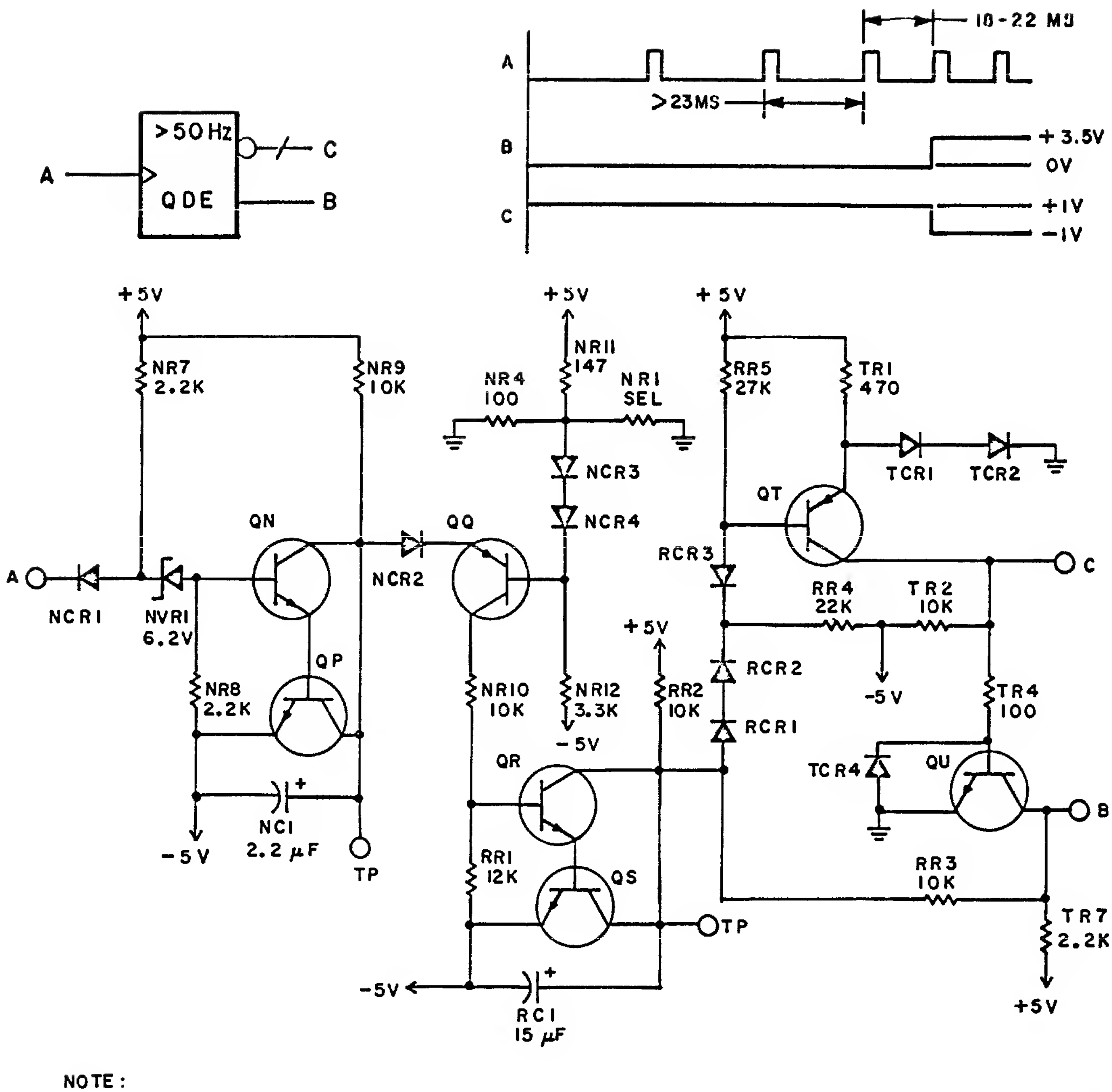


Figure 2

Diode PCR3 prevents the emitters of QN and QP from falling to a voltage that would cause both transistors to conduct when power is first applied. Such a condition would prevent the circuit from oscillating. Diodes QCR1, RCR1, SCR1, and TCR1 prevent the Schmitt transistors (QQ, QR, QS, and QT) from going into full saturation. This helps the circuit to oscillate at the higher frequencies.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J29

SPEED DETECTOR - QDE

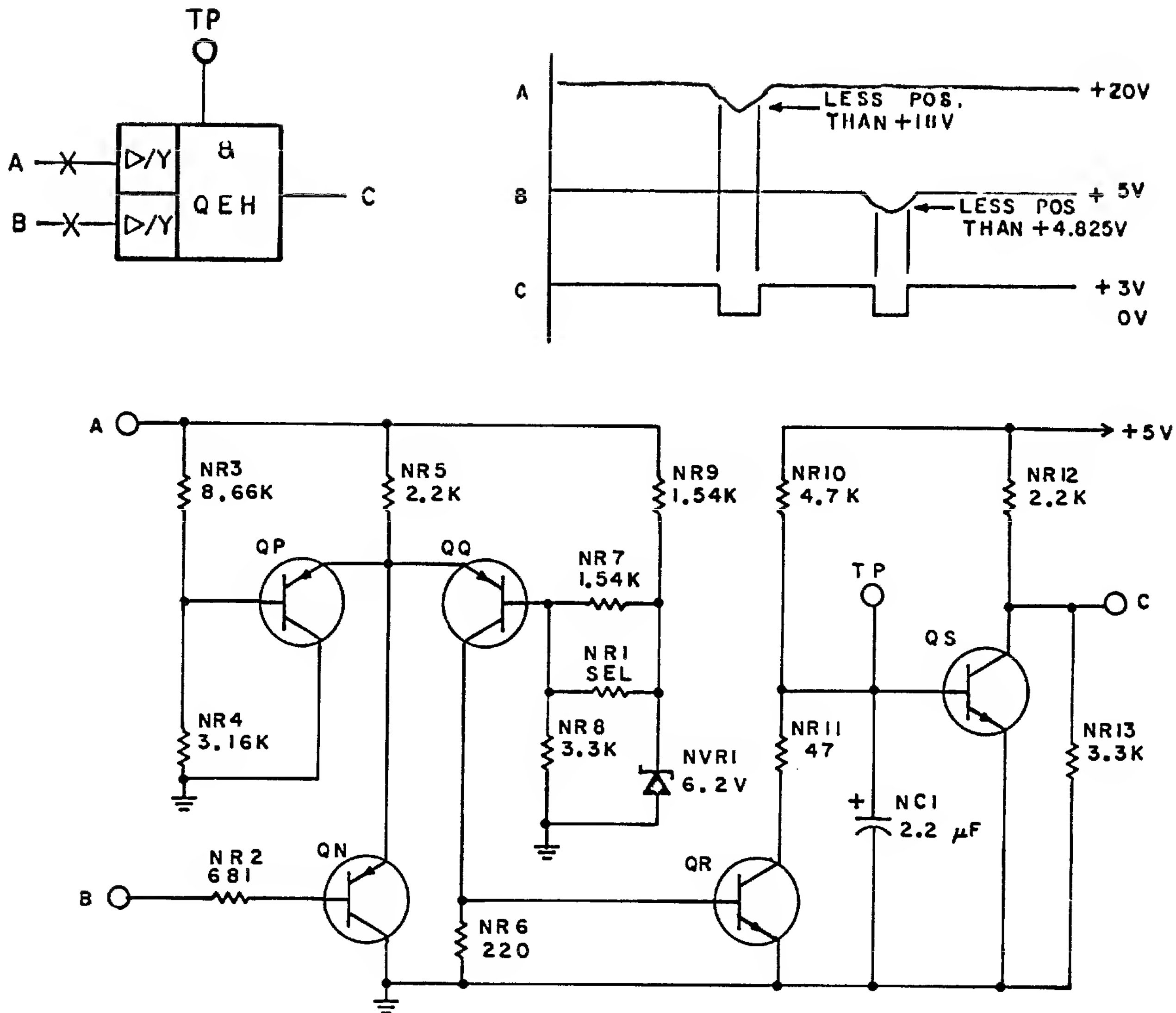
The QDE circuit monitors the sector pulses to determine whether or not the spindle is at a specified speed.

Each time a sector is sensed, a 55-μsec pulse appears at input A. Transistors QN and QP conduct and completely discharge capacitor NC1 to -5v. When the pulse drops, NC1 begins charging through NR9. When the voltage on the collectors of QN and QP reaches the threshold of NCR2 and QQ, QQ turns on. This causes transistors QR and QS to conduct and discharge RC1. With QR and QS on, RCR1 and RCR2 are back biased and the voltage at the base of QT drops, turning QT on. The collector voltage of QT rises enough to turn QU on and the output voltage at B goes low to indicate a not up to speed condition.

If the disk pack is below speed, pulses at input A are at low repetition rate. Capacitor NC1 discharges and charges turning transistors QQ, QR, and QS off and on, respectively. This in turn causes RC1 to charge and discharge. Every time NC1 charges to the threshold, QQ, QR, and QS turn on and discharge RC1. This prevents RCR1 and RCR2 from ever becoming forward biased. As a result, QT remains on and the output at B remains low, indicating not up to speed.

When the disk pack reaches the required speed, the charging time of NC1 is such that the charging voltage on NC1 remains below the threshold of NCR2 and QQ, keeping QQ, QR, and QS off. Now RC1 has time to charge and when RCR1 and RCR2 become forward biased, the voltage at the base of QT increases sufficiently for QT to turn off. The resulting reverse bias on QU turns QU off and the output at B goes high. The feedback through RR3 reduces the charge time of RC1 and the switchover goes to completion with the high output at B indicating an up to speed condition. The output signal at C is always complementary and is used by a relay driver circuit.

The voltage on the base of QQ is determined by the voltage divider comprised of NR1, NR4, NR11, NR12, NCR3, and NCR4. Resistor NR1 is a test selected resistor to fine tune the threshold of NCR2 and QQ and to compensate for the tolerances of NR9 and NC1.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J30

VOLTAGE CHECKER - QEH

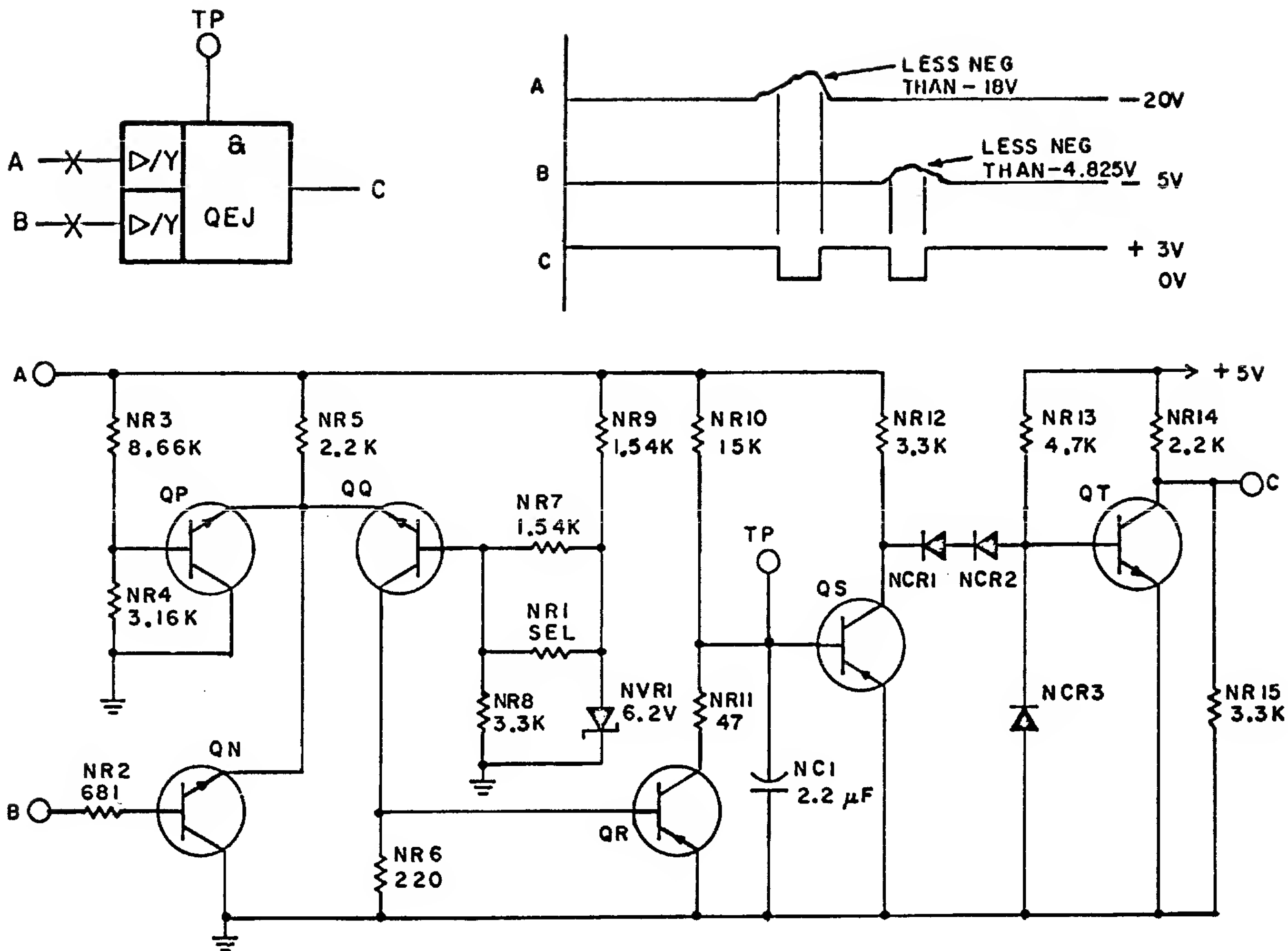
The QEH circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

1. +5 volt supply becomes less positive than +4.825 volts, or
2. +20 volt supply becomes less positive than +18.0 volts

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at +4.825 volts. If the positive supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting positive level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop to near zero volts switching QS off and establishing a +3 volt level at output C.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less positive than the base voltage on QQ (+4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS positive and turning it on. As a result, output C approaches a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the +20 volt input at A goes less positive than +18 volts, transistor QP turns on and output C goes low.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J31

VOLTAGE CHECKER - QEJ

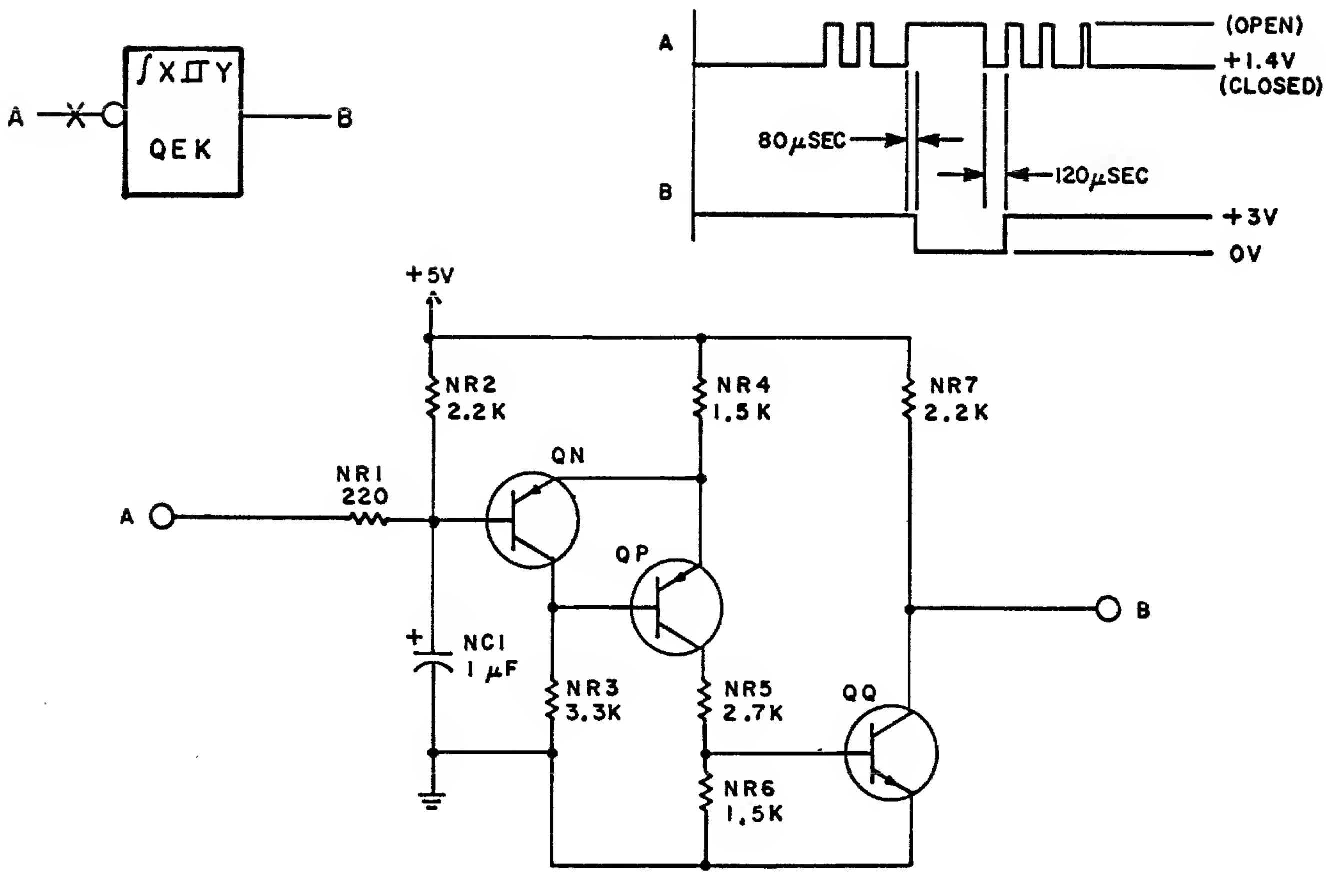
The QEJ circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

1. -5 volt supply becomes less negative than -4.825, volts or
2. -20 volt supply becomes less negative than -18.0 volts

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at -4.825 volts. If the negative supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting negative level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop to near zero volts switching QS off and developing a reverse bias across diode NCR3. This turns off transistor QT and sets the output at C to +3 volts.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less negative than the base voltage on QQ (-4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS negative and turning it on. Diodes NCR1 and NCR2 raise the base voltage of transistor QT to a point where it turns on and causes output C to approach a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the -20 volt input at A goes less negative than -18 volts, transistor QP turns on and output C goes low.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J32

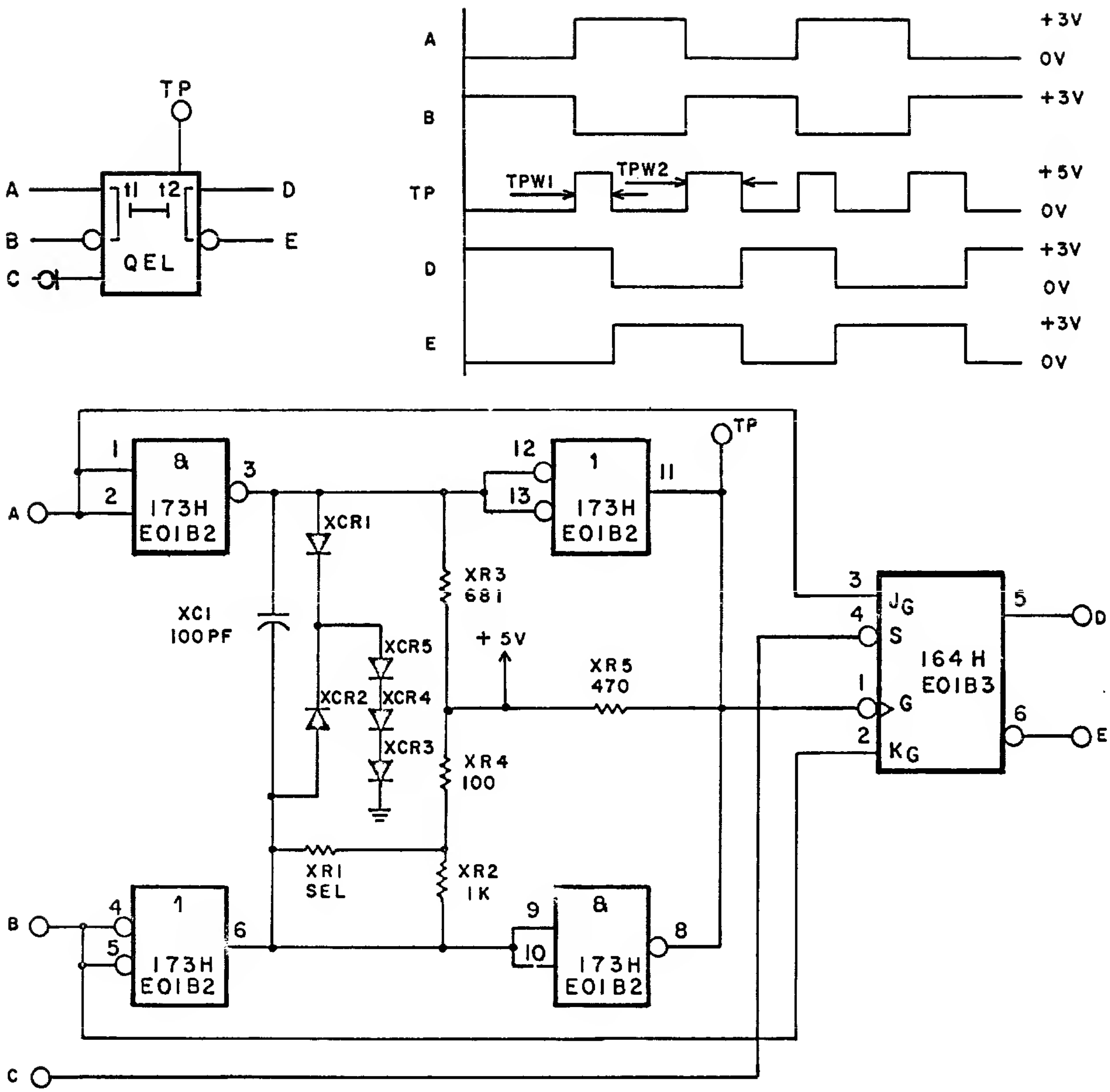
SWITCH RECEIVER - QEK

The QEK circuit produces a "1" (+3v) output at B when the solid-state switch connected to input A is closed. When the switch is open a "0" (0v) appears at output B.

A transistor switch is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN turns off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR5. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage flow through NR1, the switch, and across NC1 increases rapidly because of the short time constant of NR1 and NC1. Any spurious switching that precedes the state change increases the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP decreases and QP begins to turn off. As QP turns off, the current through NR4 decreases due to the higher lead resistance (NR3) of QN compared with QP (NR5). The current drop through NR4 causes a decrease in the voltage drop across NR4. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is turned off. With QP off, the base of QQ is near ground, causing QQ to turn off. This allows the +5v supply to flow through NR7 to output B raising the output to +3v, "1".

When the transistor switch driving the input is not conducting, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Again, any preliminary switching that precedes the actual state change will hold NC1 well below the switching level of QN. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of the positive feedback. The output then becomes "0".



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J33

SEMMETRY RESTORER-QEL

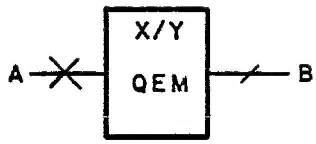
In a write driver chain where complementary TTL input signals become asymmetrical by ±8 nsec, the QEL circuit is used to restore symmetry to these signals.

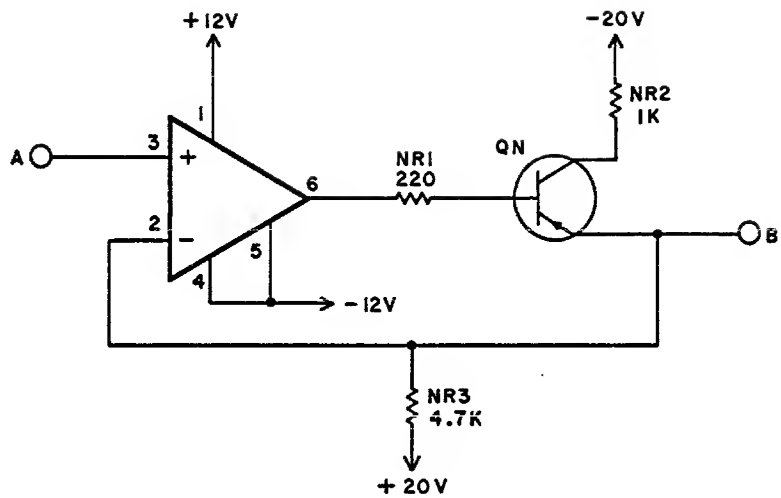
A "0" TTL level at point C will set the flip-flop insuring the same start-up conditions on inputs D and E when released by a "1" level at C.

With input A high and B low, pin 3 of 173H goes to ground and pin 6 goes to +5v through XR1, XR2, and XR4. The ground transition at pin 3 is coupled through XC1 and forces a negative spike on pin 6. Starting from a negative potential pin 6 voltage rises toward +5 volts at an RC time rate determined by XC1 and the combination of XR1, XR2, and XR4. This causes the pulse to be delayed in reaching the switching threshold of the following inverter (pins 9 and 10), and produces a positive pulse at "ored" pins 8 and 11 for the duration of the delay. The negative edge of this pulse triggers pin 1 of flip-flop 164H changing the state of outputs D and E.

The opposite conditions on inputs A and B (A low and B high) form the positive pulse at "ored" points 8 and 11 which is determined by the RC combination of XC1 and XC3. Thus, the negative edge which triggers the J-K flip-flop is controlled by alternate RC time constants, one of which can be adjusted by selection of XR1 with reference to the other resistors.

Diodes XCR1, XCR2, XCR3, XCR4, and XCR5 clamp the positive excursion on pins 3 and 6 at +2.5 volts to make delays insensitive to frequency variations up to data rates of 4 MHz.





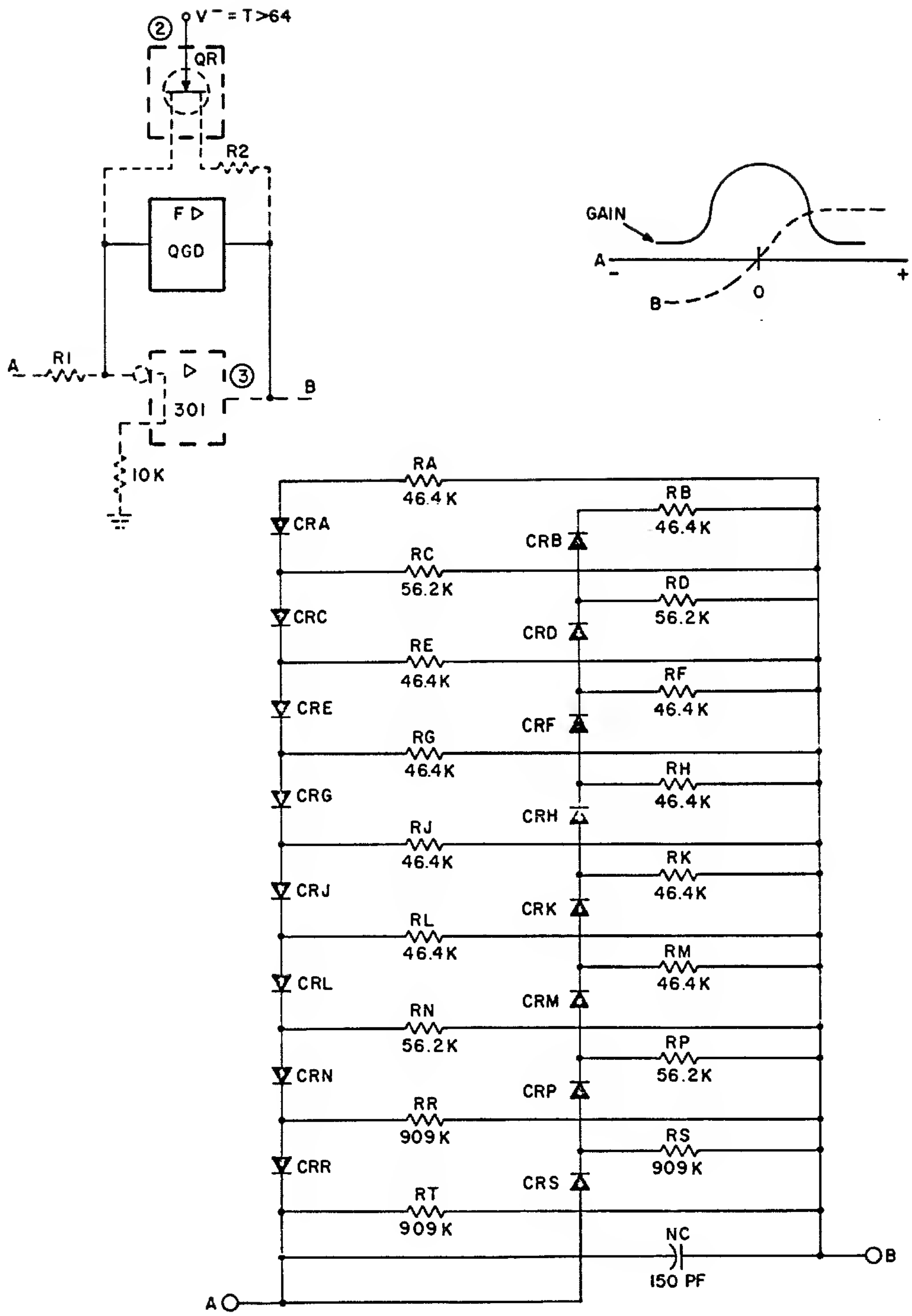
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J100

VOLTAGE FOLLOWER – QEM

The QEM circuit consists of an operational amplifier in a voltage follower configuration. A PNP emitter follower (QN) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QN in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QN.

NR3 provides a minimum current to the emitter of QN under no load conditions. NR2 is a current limit resistor. NR1 is a buffer resistor to eliminate possible oscillation tendencies.



NOTES: 1 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
② PART OF GJB CIRCUIT (REF ONLY). NEG INPUT TURNS QR OFF.
③ SHOWN FOR REFERENCE ONLY.

6T139A

FUNCTION GENERATOR - QGD

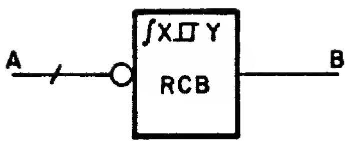
The QGD circuit is a nonlinear feedback network used as the gain determining element of an operational amplifier.

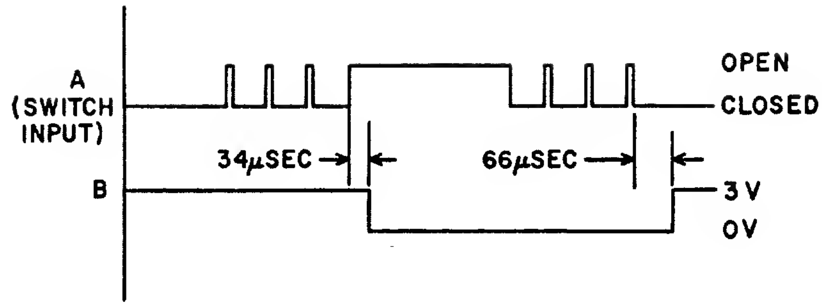
In actual circuit use, the op amp generates a voltage proportional to the desired velocity of the read/write head positioner. The amplitude of this signal is the analog representation of the number of tracks to go (position error) and will be compared with velocity to achieve maximum deceleration control without overshoot of the positioner when on cylinder (T=0).

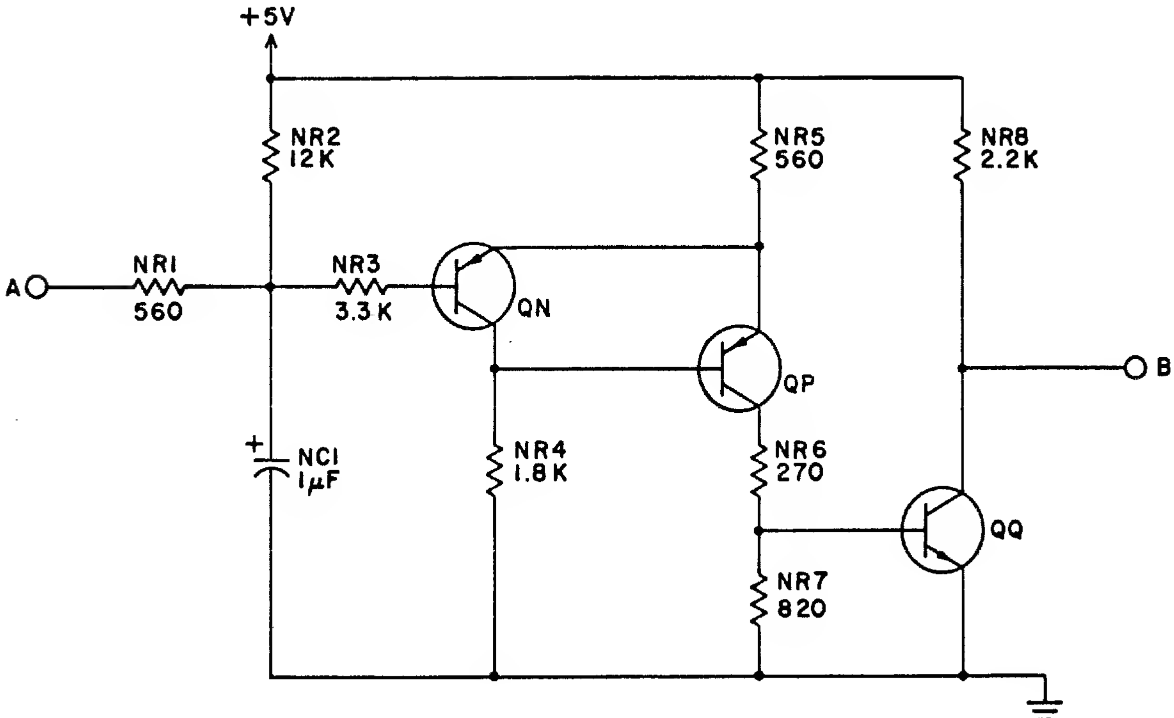
Field effect transistor QR is part of the GJB circuit to function as a logic switch. Prior to T=64, the input is at ±10 volts with the switch open. With this input voltage, the voltage drops across all of the forward-biased diodes are overcome so that the equivalent resistance of the parallel resistor network in the QGD circuit is about equal to the input resistor R1. The gain is, therefore, unity (output is 10 volts, inverted from input).

When there are less than 64 tracks to go, the input to the gate of QR changes from a negative voltage to ground potential. QR turns on, adding R2 into the feedback loop. R2 has the same resistance as R1. This reduces the feedback resistance to one-half of its former value, thus reducing the gain by 50% (output = ±5 volts).

After T=32, input A begins to decrease in proportion to the remaining position error. The QGD/op amp circuit maintains an output voltage for optimum deceleration. The optimum deceleration is obtained by taking the square root of the position signal and comparing it with the velocity signal. The resistor-diode circuits in the QGD supply the position signal: as the input is reduced, the output is reduced correspondingly. Fewer diodes conduct, removing some of the parallel resistors in the QGD circuit from the feedback loop. This increases the effective feedback resistance, increasing circuit gain. Gain is maximum (but not greater than one) when the output is below about ±0.5 volt.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T146

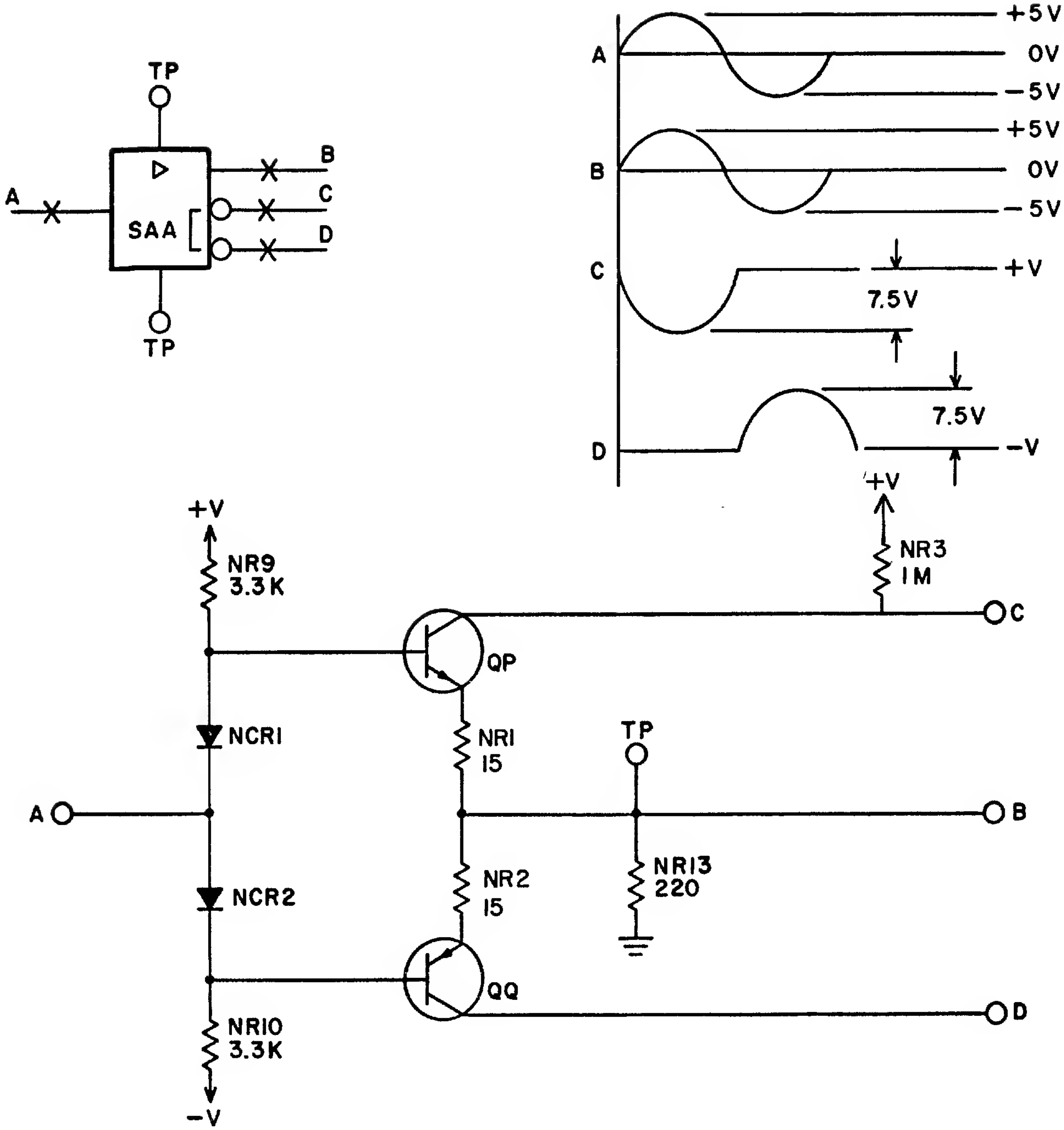
SWITCH RECEIVER - RCB

Switch Receiver RCB produces a "1" (+3v) output at B when the grounded switch connected to input A is closed. When the switch is open a "0" (0v) is felt at output B.

A switch to ground is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN is shut off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR6. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage across NC1 rapidly increases through NR1 and the switch to ground because of the short time constant of NR1 and NC1. Any contact bounce on the switch will increase the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP is decreased and QP begins to turn off. As QP turns off, the current through NR5 decreases due to the higher lead resistance (NR4) of QN compared with QP (NR6). The current drop through NR5 causes a decrease in the voltage drop across NR5. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is shut off. With QP off, the base of QQ is near ground, causing QQ to shut off. This allows the +5v supply to flow through NR8 to output B raising the output to +3v, "1".

When the switch is opened again, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Any contact bounce on the switch will hold NC1 well below the switching level of QN until the bouncing ceases. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of this positive feedback. The output then returns to "0".



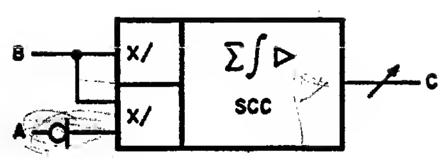
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

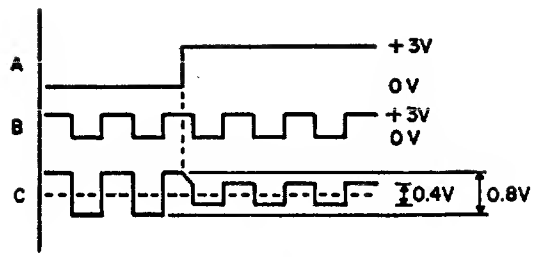
6T140

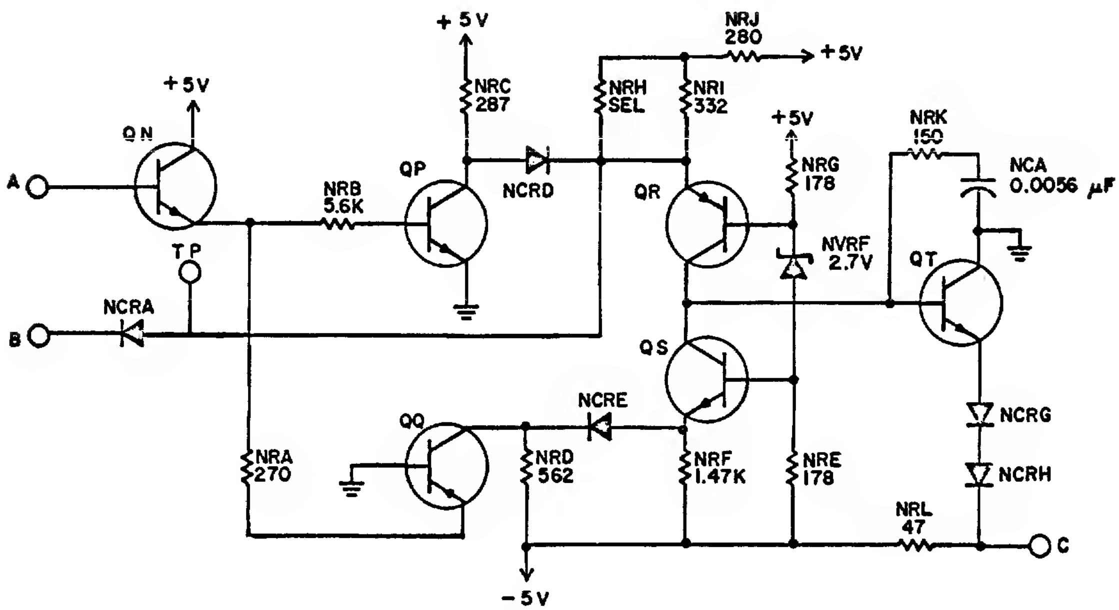
BIPOLAR CURRENT BUFFER - SAA

The SAA circuit is a power output stage for an operational amplifier. Transistors QP and QQ comprise a complementary output driver and are always biased slightly on by diodes NCR1 and NCR2.

The quiescent current in the output driver is nominally 6.5 ma and the maxinum signal amplitude for the circuit is ±5 volts.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. TJ348

LOW PASS FILTER AND AMPLIFIER - SCC

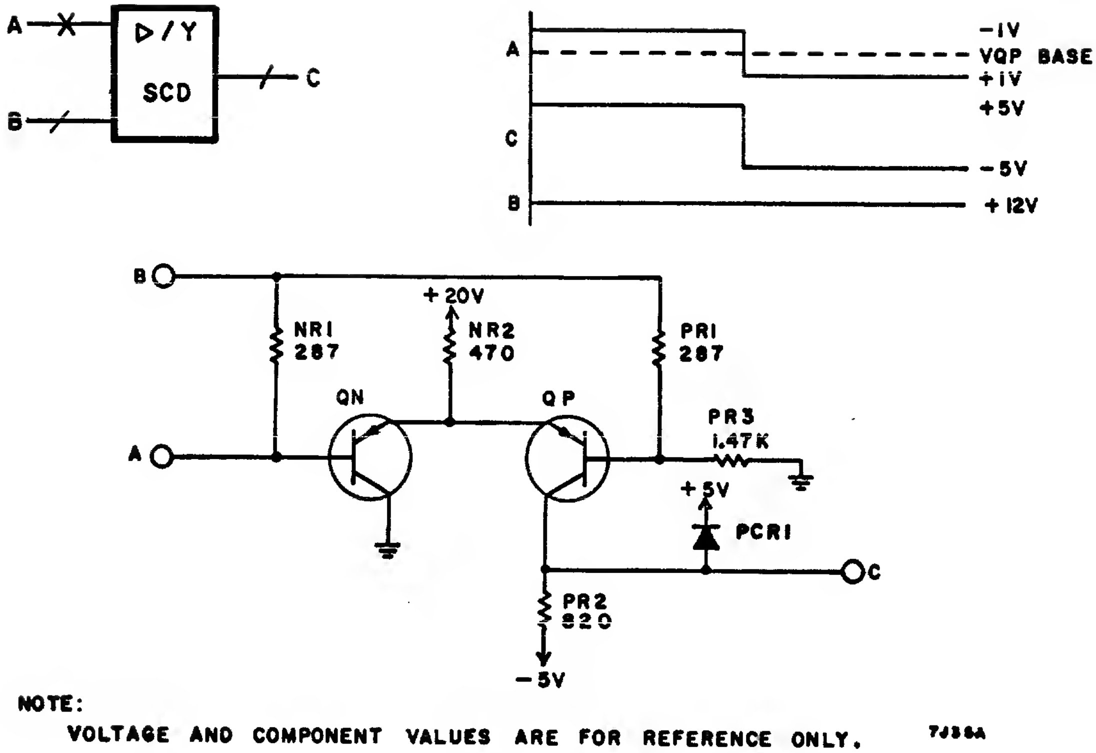
The SCC circuit consists of a bilevel current switch with a bidirectional current pump, a filter capacitor, and a level shifter. The circuit converts TTL input signals from a comparator circuit to produce a dc voltage level at TPB. Because of the phase locked oscillator closed loop, the current pump drives the dc level at TPB to reach a 50/50 duty cycle when the signal at input B is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency causes a change in voltage at TPB. A separate TTL input signal selects one of two possible current levels for the current pump.

QN, QP, QQ, NRA, NRB, NRC, NRD, NCRB, and NCRC form the bilevel current switch. For fast frequency synchronism, input A is a TTL "zero", turning all three transistors off and forward biasing NCRB and NCRC. This adds the current from NRC and NRD to the normal current pump level resulting in a high drive current. In the normal operating mode, input A is a "one", turning on QN, QP, and QQ. This back biases NCRB and NCRC, resulting in normal current pump drive.

NRG, NVRF, and NRE form a reference voltage divider for the current pump. NRF and QS is the negative-going current sink. This sinks a current of approximately 2 ma continually. NCRA, NRH, RNI, and QR form a switchable current source of approximately 5 ma. When a square wave of TTL logic level is applied to the zero "OR" gate of input B, NCA alternately is charged and discharged by 2 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times; therefore, the voltage across NCA has very little ac component in it.

Resistor NRK generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRK and the currents from the bidirectional pump. The net result at output C is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

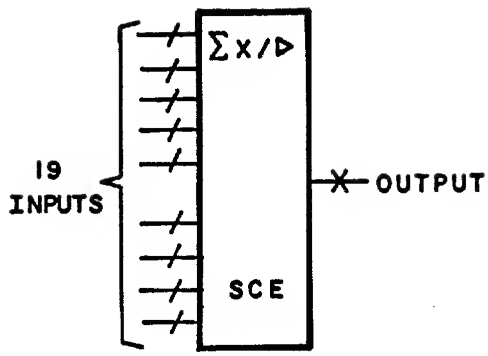
QT, NCRE, NCRF, and NRL form a buffer and level shifting circuit. They shift the waveform at base of QT negatively to a level appropriate for controlling the voltage controlled oscillator.

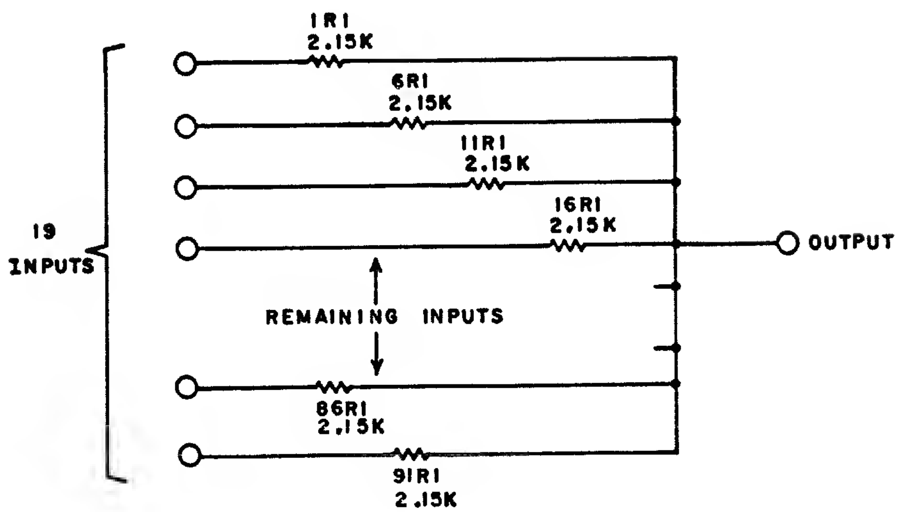


VOLTAGE COMPARATOR - SCD

The SCD circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

Input A typically is connected to the output of circuit SCE. Input B is typically +12 volts, and normal or "no fault" condition would be for 0 or 1 of the inputs of the summing ladder (SCE) to be grounded and the remaining inputs to be open. SCE would then output a voltage (to input A) higher than the reference voltage at the base of QP. QN then would be turned off and QP turned on driving output C to +5 volts. An abnormal or "fault" condition would be for 2 or more inputs of the summing ladder (SCE) to be grounded with the remaining inputs open. This would cause the voltage at point A to be lower than the reference voltage at the base of QP. QN would then be turned on and QP turned off. Point C would then switch to -5 volts.

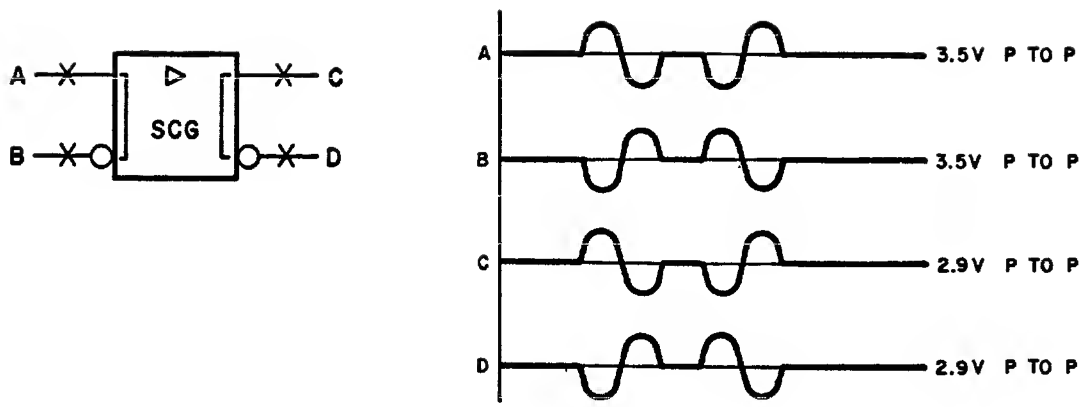


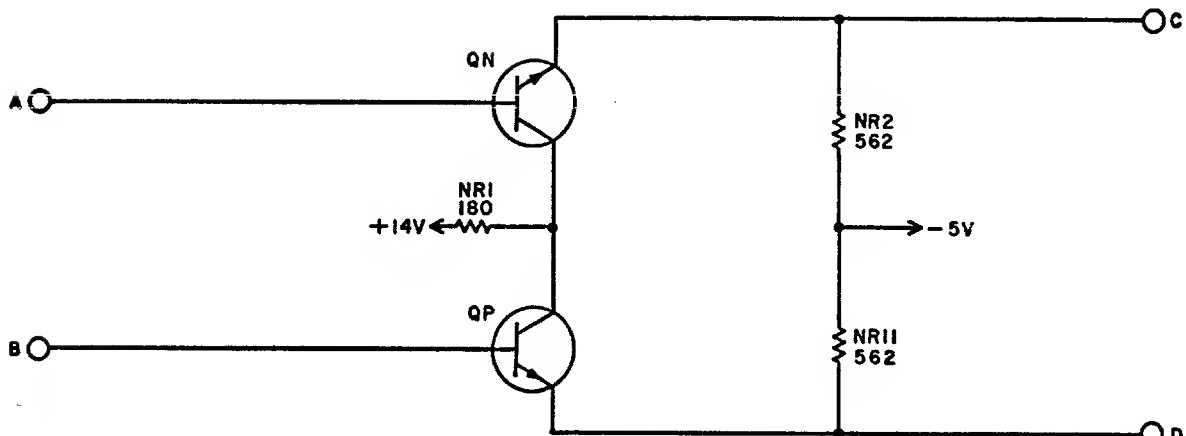


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J36A

Summing Ladder - SCE

The summing ladder SCE circuit is a network of resistors with the output connected to a voltage source through a common resistor such as input A on the SCD circuit. This forms a resistor divider circuit with an output voltage dependent upon the number of inputs (resistors) being connected to ground potential. One or more comparators could be connected to the output to check for a particular number of inputs being connected to ground.





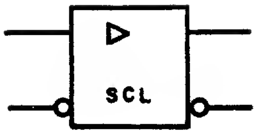
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

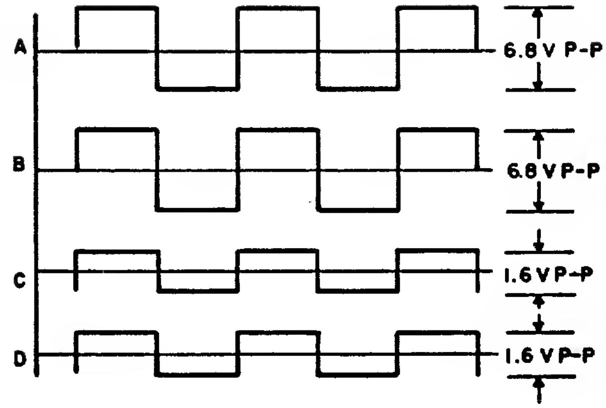
7J113A

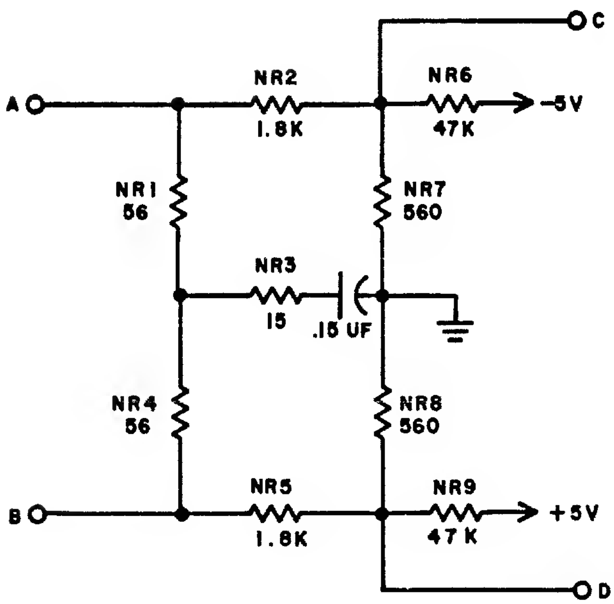
BUFFER AMPLIFIER - SCG

The SCG circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal read from the servo head.

QN and QP are emitter followers that present comparatively high input impedance and low out impedance.





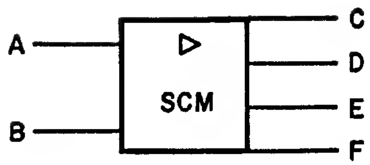


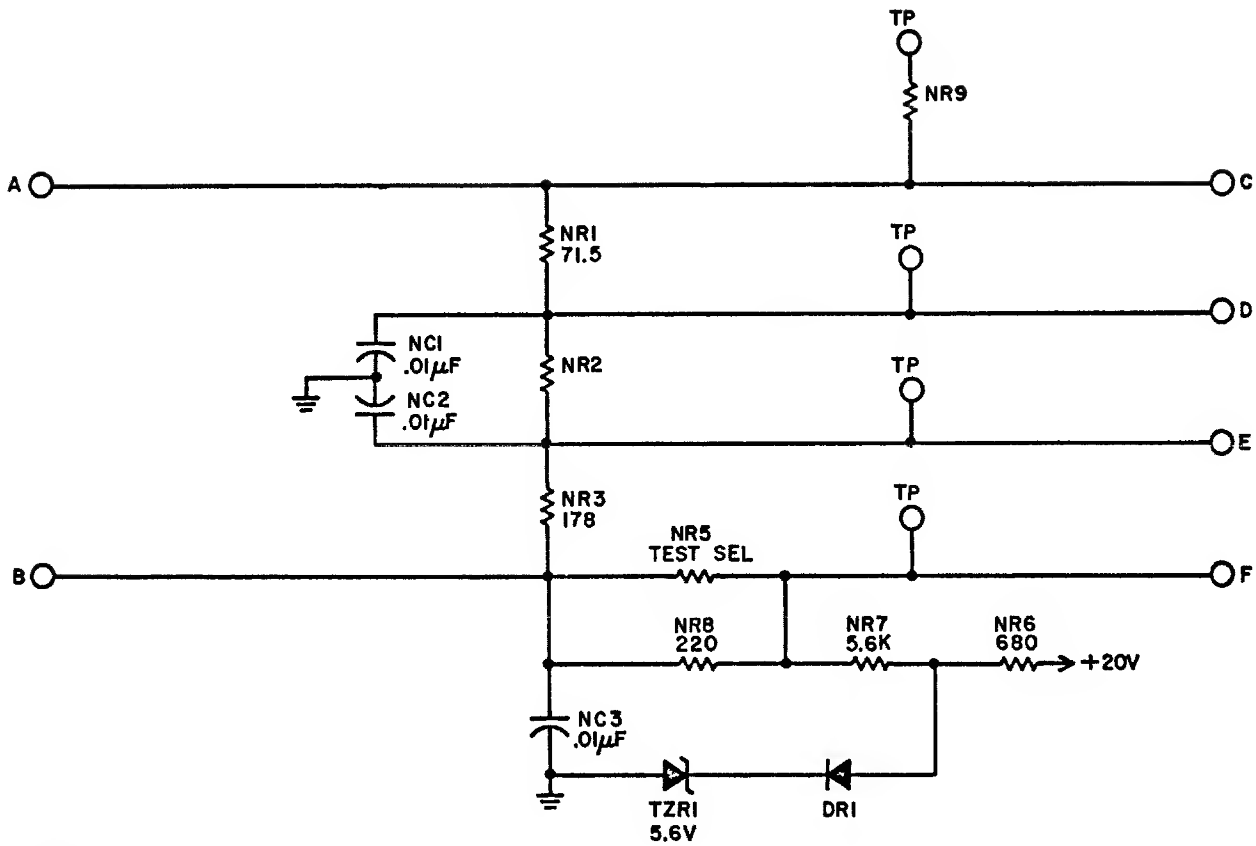
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J166A

TERMINATOR/DIVIDER SCL

The SCL circuit consists of a line terminator network (NR1 and NR4) and a resistor divider network (NR2, NR5, NR7, and NR8). Resistors NR6 and NR9 supply a bias voltage to outputs C and D. This bias voltage insures a definite state for the following receiver circuit.

NR3 and NC1 offer a high DC resistance and provide a low AC impedance to ground.





NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

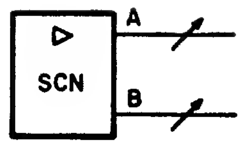
7J110

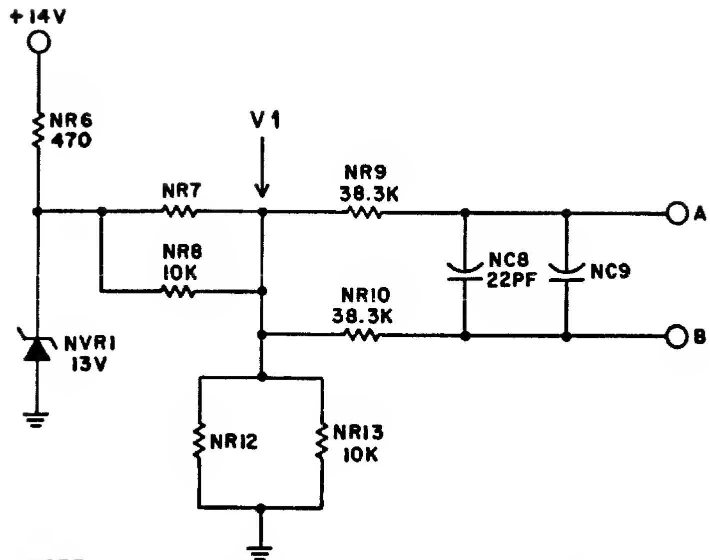
DIVIDER NETWORK – SCM

Resistor divider network SCM supplies various reference voltages for comparator circuits.

Input B (V_B) is typically -.7 volts. Input A (V_A) varies from -.7 to +1.5 volts, depending on read back voltage amplitude.

Output D will be .72 x (V_A - V_B). TZR1, DR1 and NR6 provides a regulated voltage which keeps the reference voltage at output E stable after NR5 has been test selected. Output E will be approximately -.6 volts.



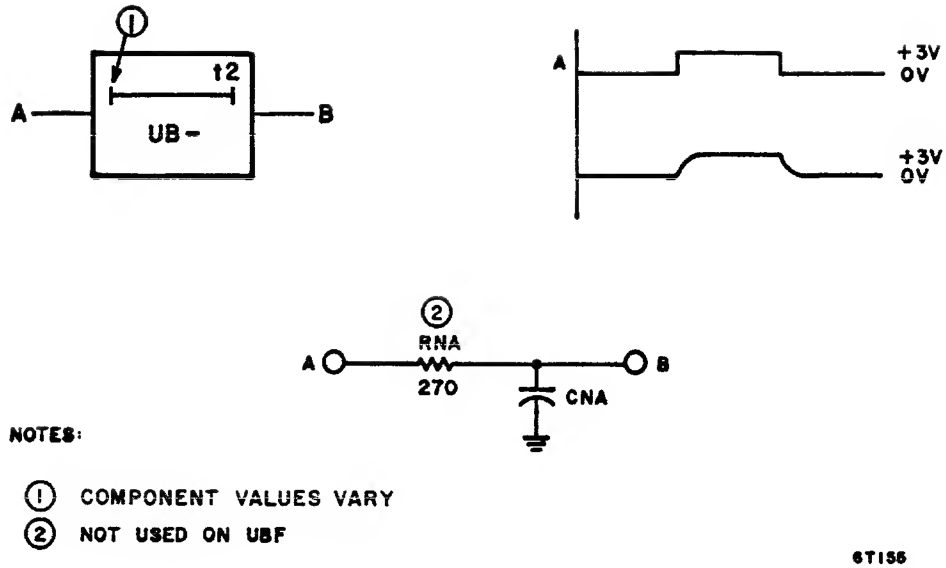


NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

FREQUENCY CONTROL NETWORK - SCN

The SCN circuit is used to control the free-running frequency of the type 579 voltage controlled oscillator integrated circuit. The free-running frequency is the nominal frequency of the 579 without data inputs. The actual frequency of the 579 will deviate from nominal because of minor variations in the disk pack rotational speed.

Resistors NR7 and NR12 are selected (both may not be required) to set the voltage at V1 equal to +6.5 volts. This voltage, plus the capacitance introduced by NC8 and NC9, are applied to pins 5 and 6 of the 579 to set the free-running frequency. Capacitor NC9 is selected for precise frequency control. The frequency is approximately 12 MHz if NC9 is 3 picofarads; it is about 1.6 MHz if NC9 is 150 picofarads.



DELAY - UBD/UBE/UBF/UBH

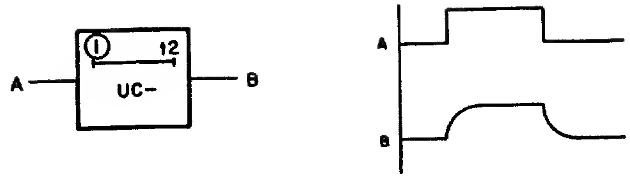
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

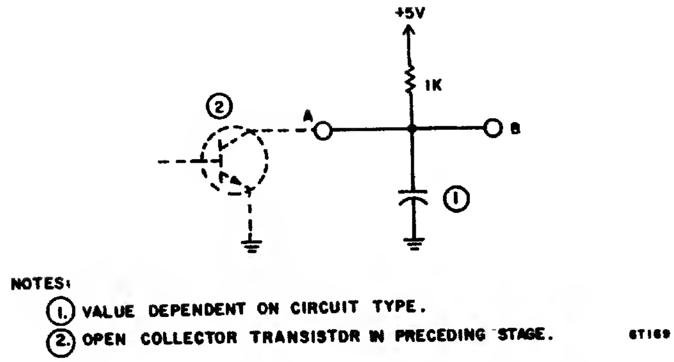
Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms
UBH	100 nsec





Delay - UC–

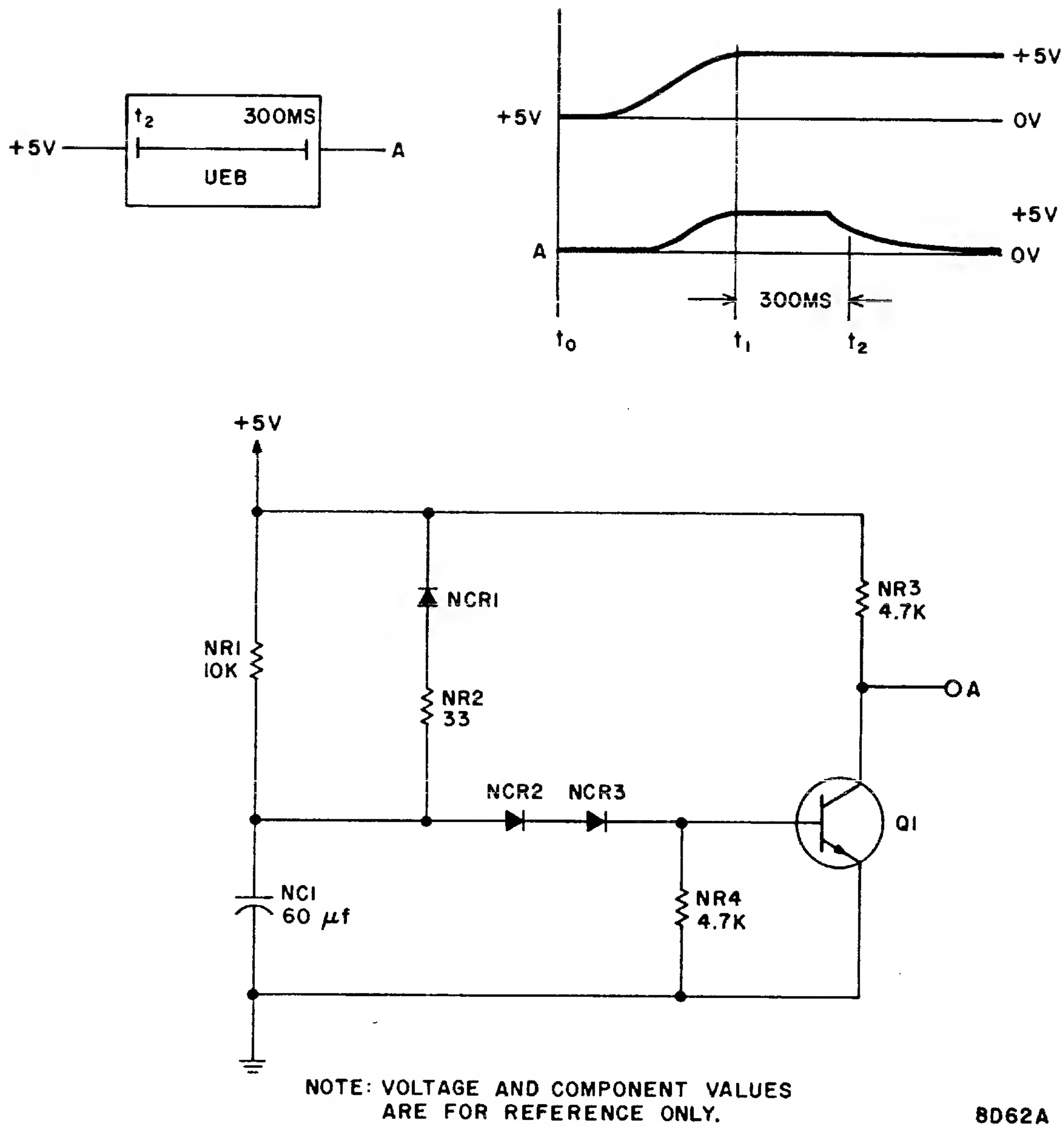
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5 volts and a capacitor connected to ground.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

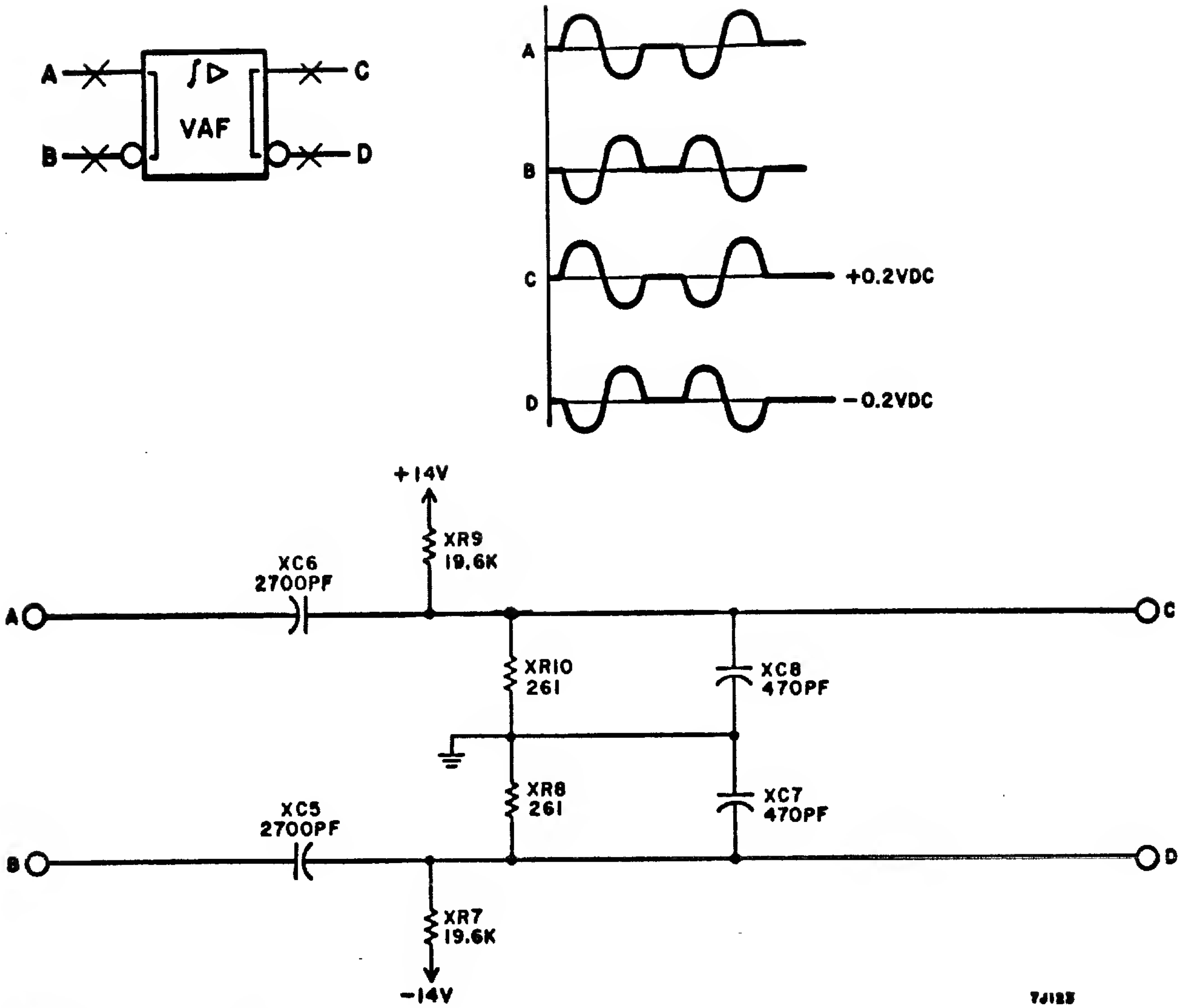
Circuit Type	Capacitance	Resistance	Delay
UCF	1500 PF	1K	350 nsec
UCH	390 PF	1K	100 nsec
UCJ	22 μF	2.7K	10 μsec
UCL	390 PF	2.2K	155 nsec
UCN	3300 PF	2.7K	1.5 μsec
UCT	2200 PF	2.7K	1.0 μsec



DELAY - UEB

The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor NC1 is discharged by NR4, NCR2 and NCR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and NC1 is charging. As the voltage across NC1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.



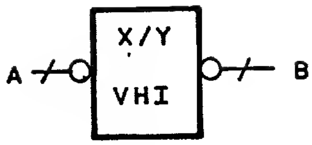
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

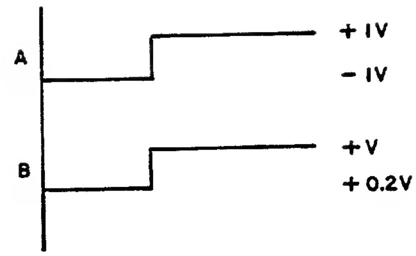
LEVEL SHIFTER – VAF

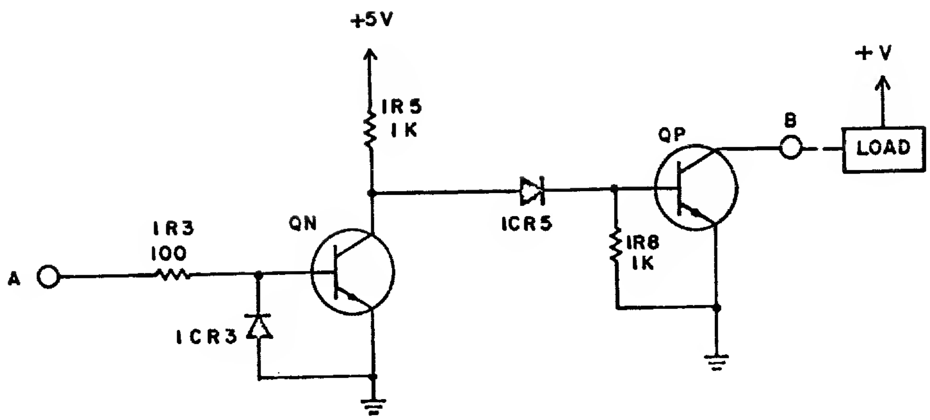
The VAF circuit receives the differentially amplified signal read by the servo head. It level-shifts the dc baseline of this signal to permit it to be analyzed by a differential voltage comparator.

Capacitors XC5 and XC6 block the dc level of the input while permitting the ac signal to pass. The resistors set the new dc baselines of the signal as shown in the illustration. Capacitors XC7 and XC8 shunt noise to ground.

The dc levels establish the switching point of the following comparator circuit. In its typical application, the next circuit switches state when output C is negative with respect to output D. The bias provided by the VAF circuit permits the comparator to switch state for about 50% of the time that input A is negative with respect to input B.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

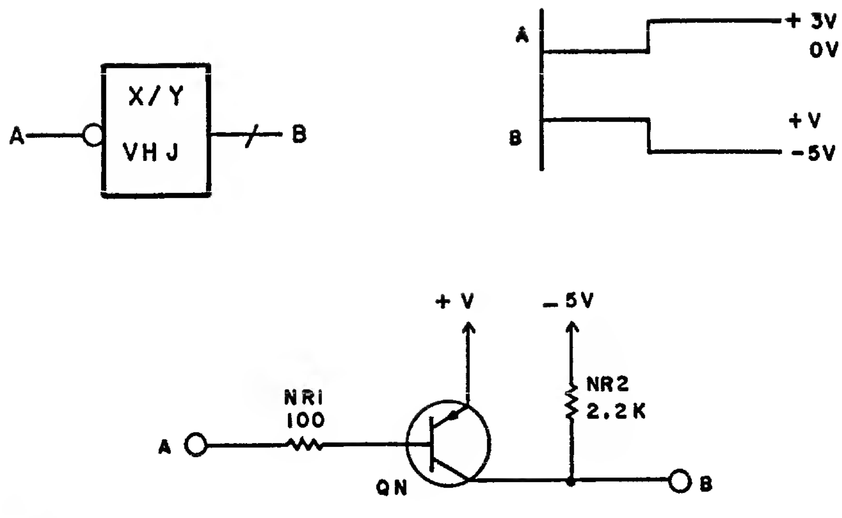
7J38

RELAY DRIVER - VHI

The VHI circuit drives a relay armature terminated at +V volts. Output B of the circuit functions to apply or remove ground so that the +V source may pull or drop the relay.

An input of +1 volt at A turns transistor QN on. The collector of QN goes low which turns transistor QP off. As a result, output B goes to +V and the relay is de-energized.

A -1 volt at input A turns off transistor QN. (Diode CR3 limits the reverse bias on QN to -0.7 volts.) The collector of QN now goes high which turns on transistor QP. This causes output B to go low, near 0 volts, energizing the load.



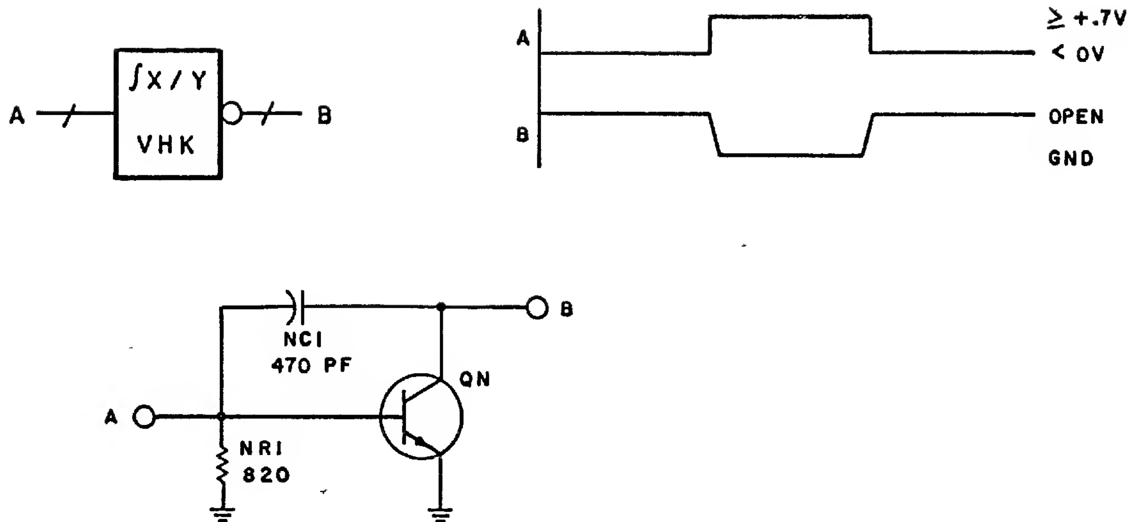
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J39

LEVEL TRANSLATOR - VHJ

The VHJ circuit converts TTL logic levels to +V and -5 volt levels where +V = 1.4 to 2.4 volts.

When a "0" (0v to +.4v) is applied to input A, QN turns on and applies +V (minus V_{ce} sat) to output B. When a "1" (+2.4v to +5v) is applied to A, QN turns off and output B switches to -5 volts.



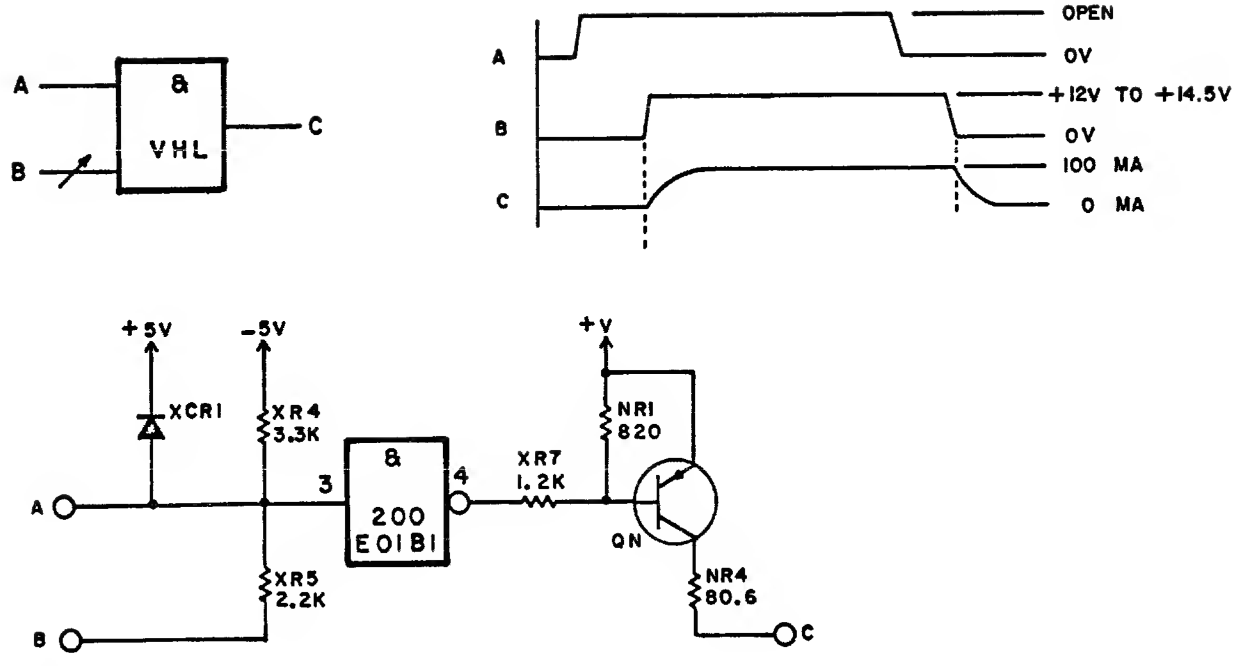
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J40

INTEGRATING LEVEL TRANSLATOR - VHK

The VHK circuit is a voltage level shifter that slows down and controls "turn on" and "turn off" transition times.

With an input to A of +.7 volts or greater (current limited to 20 ma), QN turns on with output B going to ground at a rate controlled by collector-base feedback capacitor NC1. With an input of 0 volts to -3 volts, QN turns off and output B is disconnected from ground.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

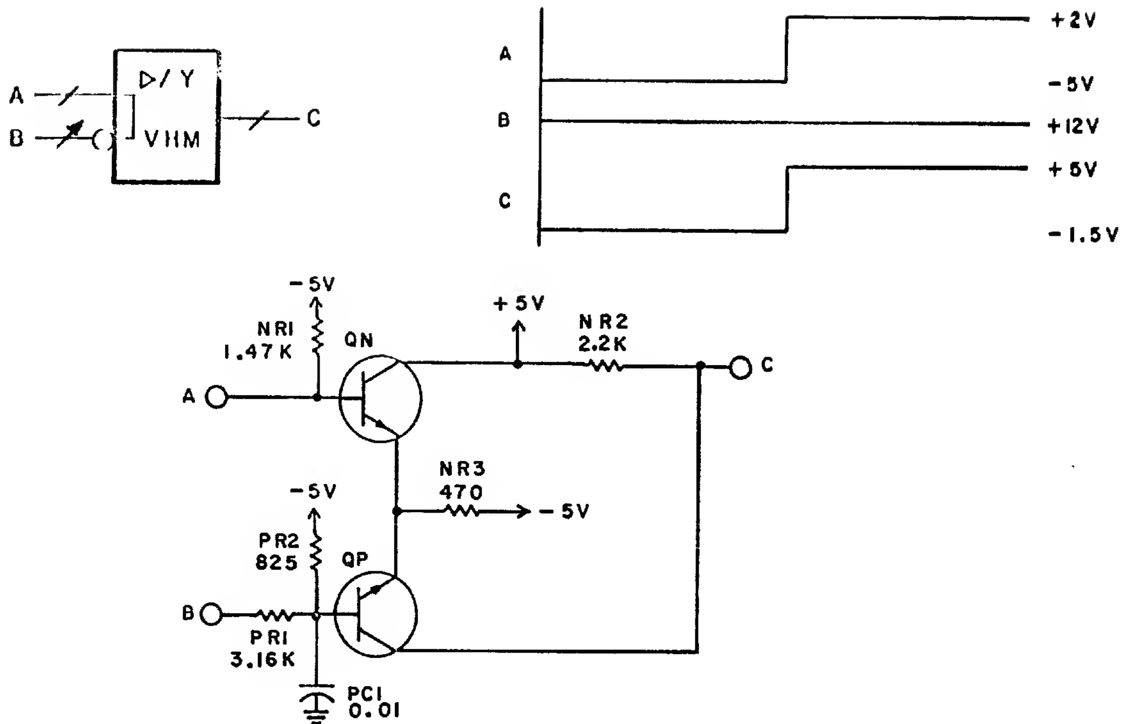
AND GATE - VHL

The VHL circuit is an erase current driver with a two AND function input.

Input A is normally connected to the output of a TTL open collector gate. Input B is normally connected to pin B of the FAG circuit which can vary from +12 volts to +15 volts. Output C gets connected to an erase head winding.

When input A is open ("1" output condition of open collector TTL gate) and input B is high (+12 v to +15 v), divider XR5 and XR4 insures a "1" condition at gate input pin 3. With inversion of the gate, pin 4 is a "0" (0 volts). This turns QN "on" and applies +V (approximately +12v) to the erase termination resistor NR4 which determines the amount of erase current to the head.

If either input A or B is held at a "0" condition, the output of gate 200 (pin 4) will go to +V (open collector output), QN will be turned "off" and no erase current will flow.



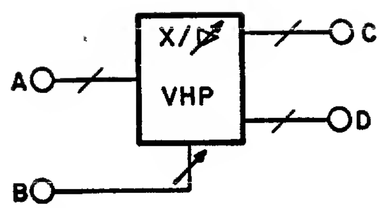
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

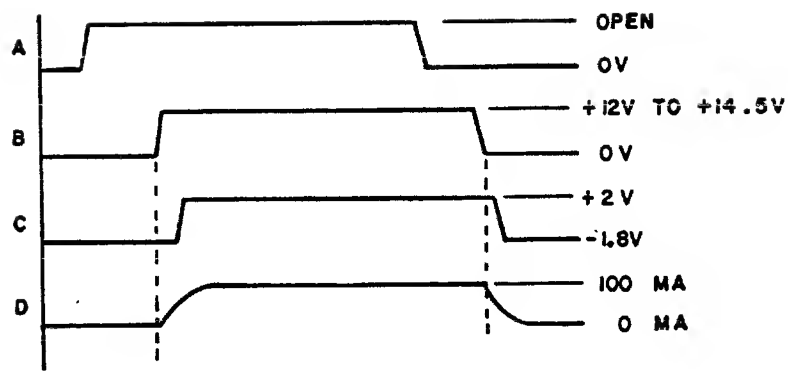
FAULT DETECTOR - VHM

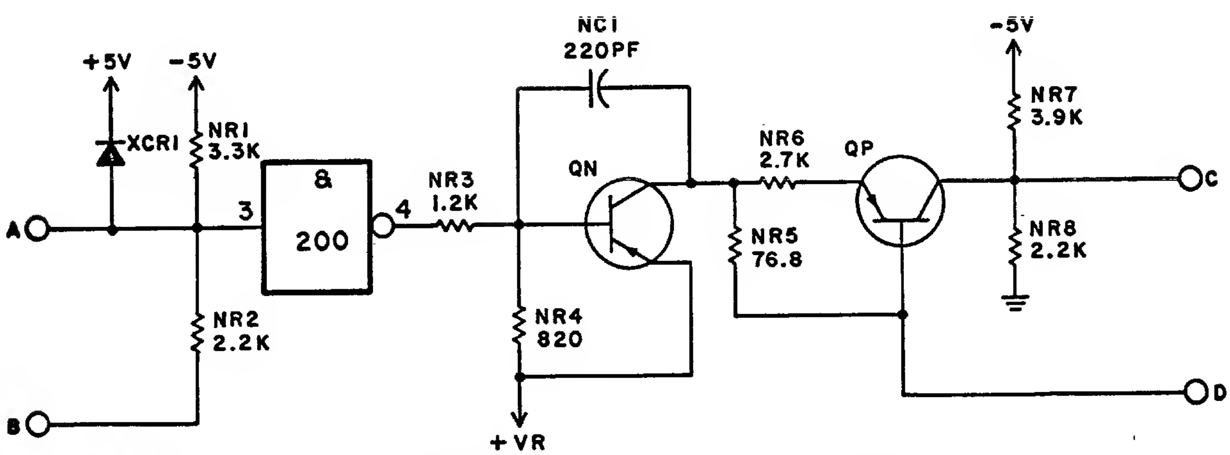
The VHM circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

Input A is typically connected to output G of a write driver (JAG) circuit. Input B is connected to a controlled current source (FAG) with an output between +12 to +15 volts, dependent upon the current drain at QP.

The voltage level at input A is determined by the current flow into A through NR1 to -5 volts. With no current into A (A low) the voltage at A is -5 volts which is less than the voltage at the base of QP. QN is off, QP is on, and output C gets clamped at the saturated level of about -1.5 volts or at -.7 volts if output C is connected to a TTL gate input that has a diode clamp. When current flow into A exceeds approximately 2.7 ma, the voltage at A becomes more positive than at the base of QP. QN turns on, QP turns off, and output C rises to +5 volts.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J96

ERASE CURRENT DRIVER - VHP

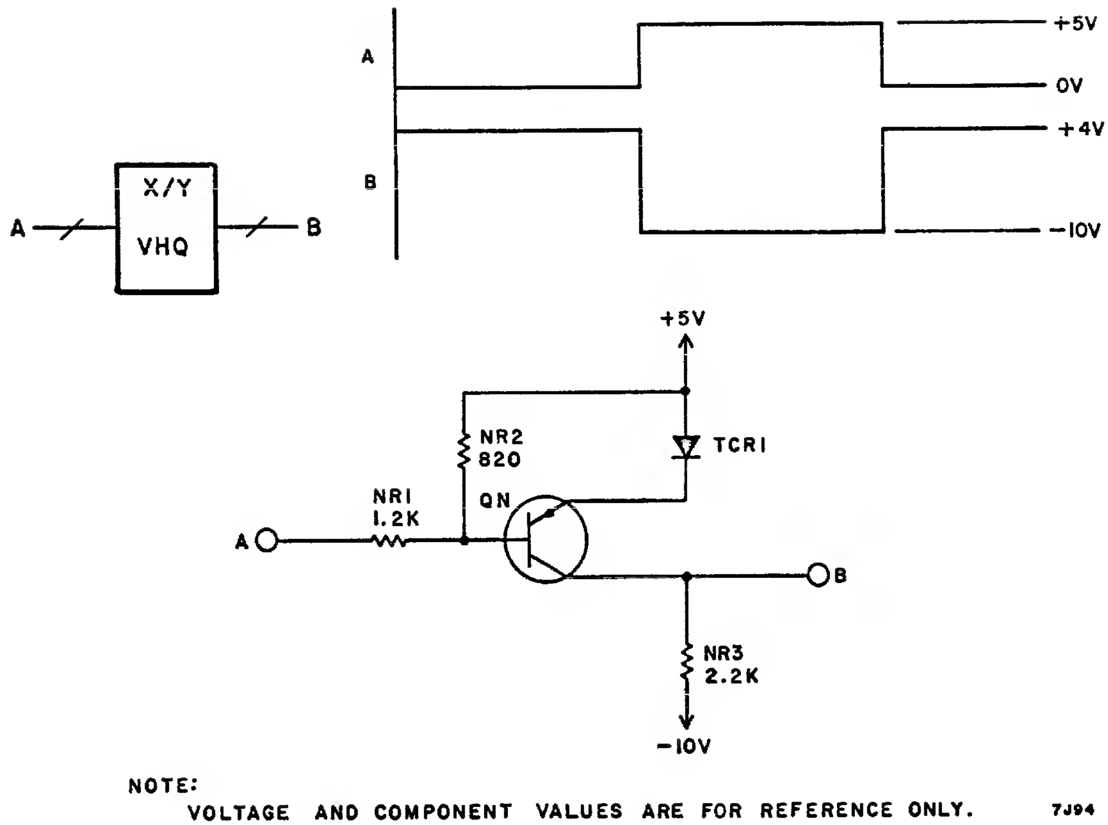
The VHP circuit provides approximately 100 ma of current (output D) for the erase coil of a read/write head. The circuit includes an output (C) bi-level signal to indicate whether the erase current is on or off.

Input A is connected to the output of an open collector IC TTL gate. Input B is connected to the write voltage (Vw) which can vary from 12 to 14.5 volts or it can be shut off (0 volts).

Both input A and B have to be "1's" to activate QN which provides erase current through NR5 to output D. A "1" at A is the "open" state of the open collector IC. A "1" at B is Vw = 12 to 14.5 volts. These input conditions cause a "0" at pin 4 of 200 element which will turn QN "on". When QN is on, Vr is applied to NR5 and NR6. Output D is connected to an erase coil winding so the current is controlled by the ratio of Vr to NR5. The voltage drop across NR5 is across NR6 and emitter-base of QP. This turns on QP which supplies a collector current of .028X (current at output D). This changes the voltage at output C from -1.8 volts to +2 volts.

A "0" (0 volts) at either input A or B will cause a "1" at pin 4 output of element 200. QN will turn off eliminating erase current at output D. No voltage drop across NR5 causes QP to turn off and output C goes back to -1.8 volts.

NQ1 slows down the rise and fall times of erase current transitions.



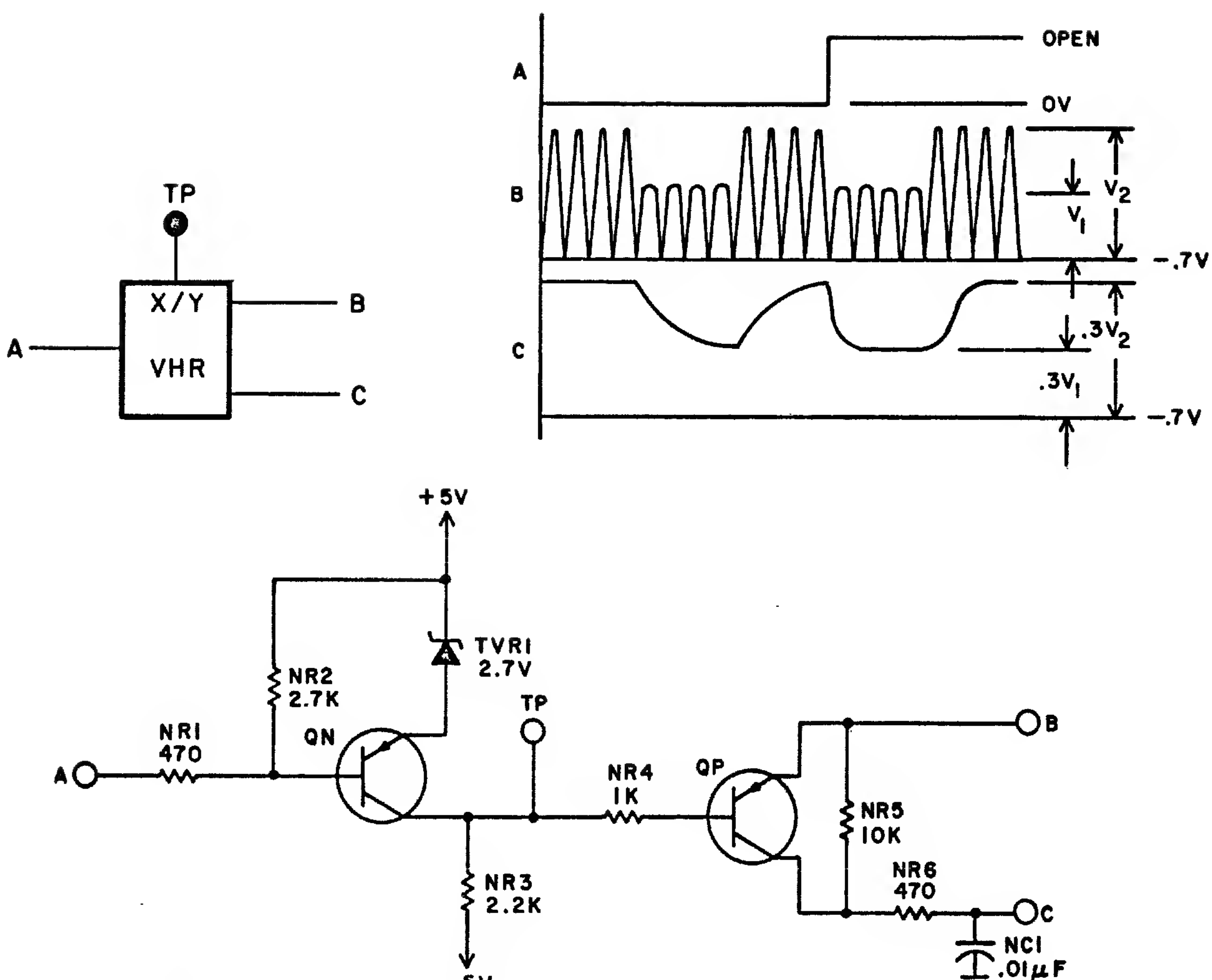
LEVEL TRANSLATOR – VHQ

The VHQ circuit translates digital signal levels of 0V and +5V to digital levels of +4V and -10V respectively.

A "0" (0V to +.5V) at input A causes QN to turn on and apply +5V minus V_{TCR1} or about +4 volts at output B.

A "1" (input open or +5 volts) at input A causes QN to turn off and output B goes to -10 volts through load resistor NR3.

An open collector IC or discrete transistor is used to provide the described input conditions at input A.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J99A

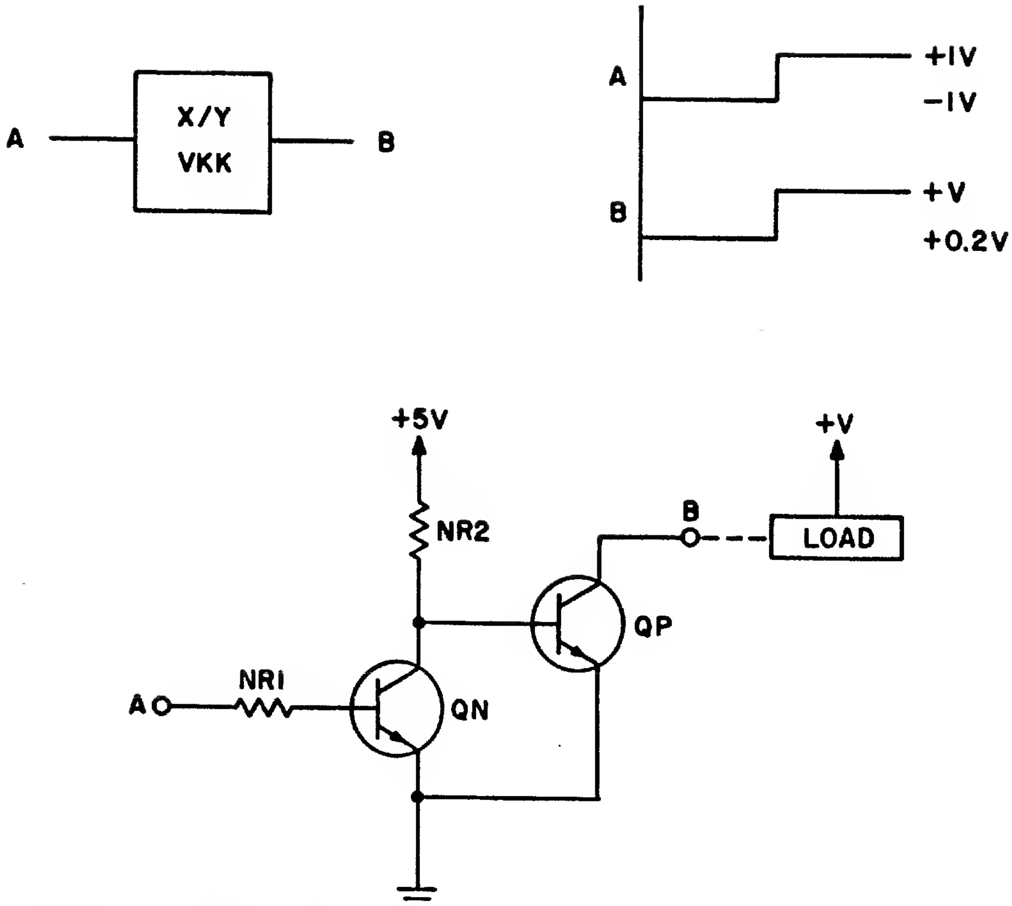
TIME CONSTANT SWITCH - VHR

The VHR circuit converts digital signals to integrator response times by switching a resistor in and out of an RC circuit. The integrator is made up of NR5, NR6, and NC1 with the input at B and output at C. The response time of this integrator can be changed by causing QP to switch NR5 in or out of the circuit.

Full wave rectification of read head signals is entered at B. The integrated output at C is a DC level which is an average value of the input signal waveform.

A "0" (0V to +.5V) at input A causes QN to turn on and apply +5V minus V_{TVR1} or about +2 volts at the base of QP. This causes QP to turn off which puts NR5 in series with NR6 and the time constant (response time) of the integrator becomes (NR5 + NR6) times (NC1).

A "1" (input open or +5 volts) at input A causes QN to turn off. QN collector goes toward -5 volts through NR3. This causes QP to turn on which "shorts out" NR5 leaving NR6 and NC1 to form the integrator. The time constant (response time) then becomes (NR6) times (NC1).



NOTE:
VOLTAGE AND COMPONENT VALUES
ARE FOR REFERENCE ONLY.

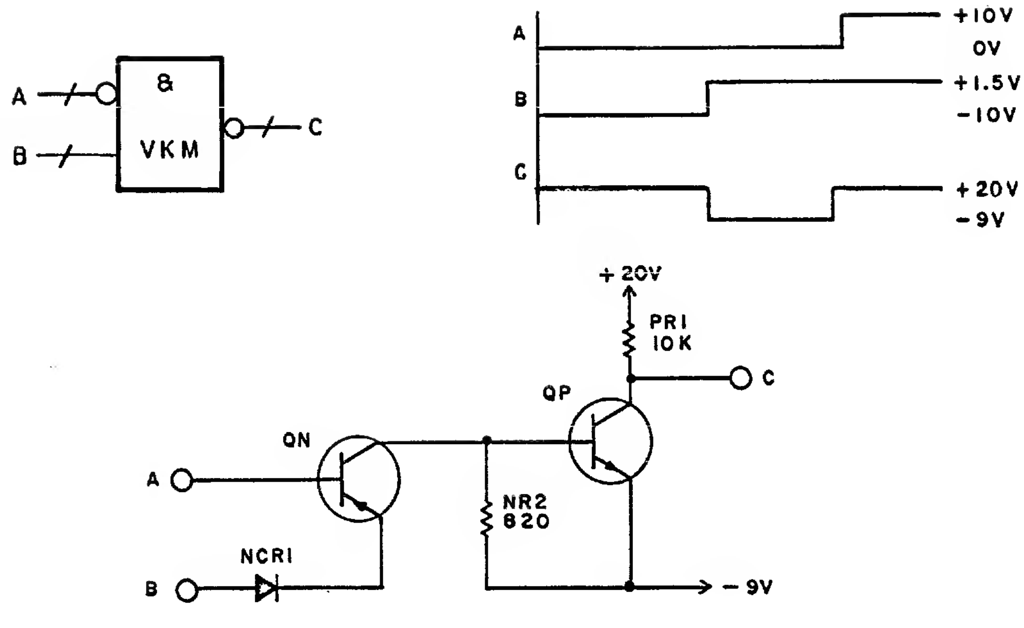
8D57

RELAY DRIVER - VKK

The VKK circuit drives a relay armature terminated at +V volts. Output B of the circuit functions to apply or remove ground so that the +V source may pull or drop the relay.

An input of about +1 volt at A turns QN on. The collector of QN goes low which turns QP off. As a result, output B goes to +V and the relay is de-energized.

A -1 volt turns QN off. The collector of QN goes high which turns QP on. This causes output B to go low, energizing the load.



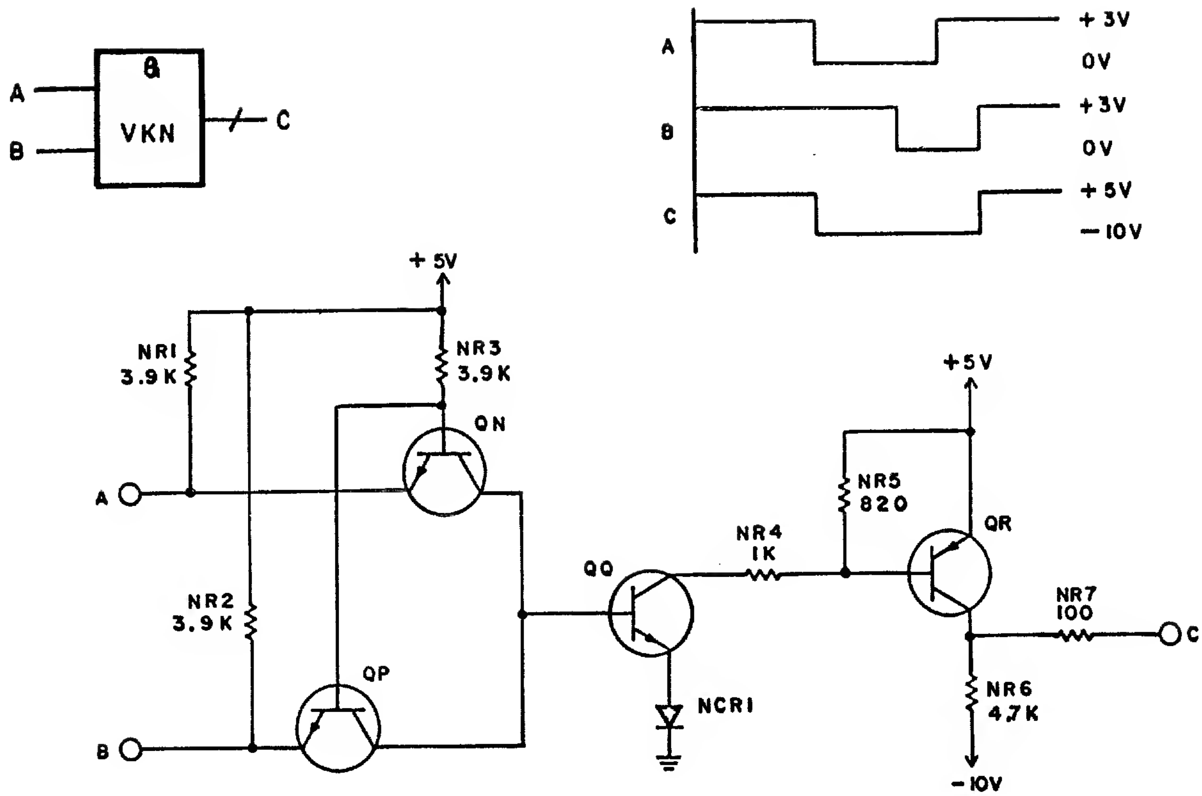
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J43

AND GATE - VKM

The VKM circuit is a two input gate with output levels of +20 volts and -9 volts.

Input A is typically connected to output B of VHK circuit and input B is connected to output C of VKN circuit through an 820 ohm current limiting resistor.

Diode NCR1 provides breakdown protection for the base emitter junction of QN when inputs A and B conditions cause reverse bias.



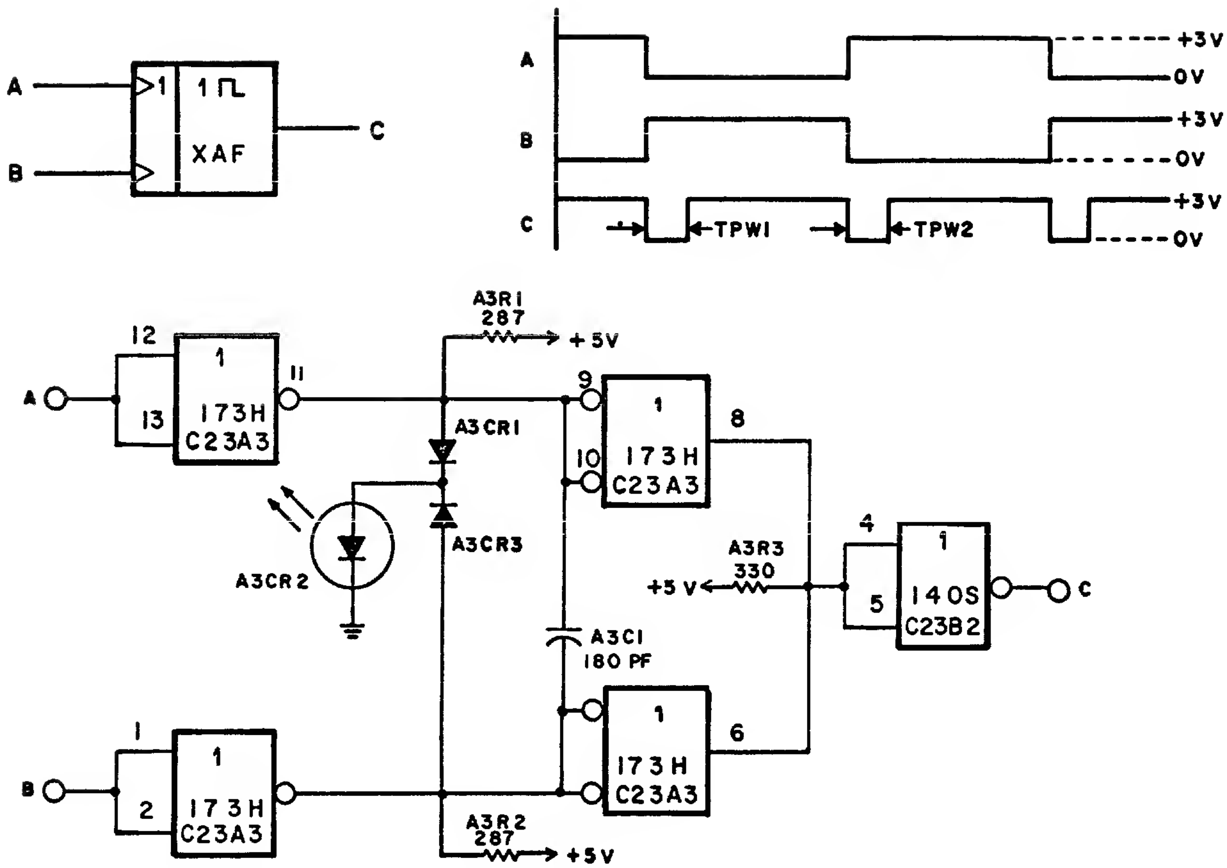
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J44

TWO INPUT AND GATE - VKN

The VKN circuit is a two input AND gate with input voltage levels matched to TTL threshold levels (approximately 1.4 volts) by NCR1.

Output voltages of +5 or -10 volts are current limited by resistors NR7 and NR6.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J53A

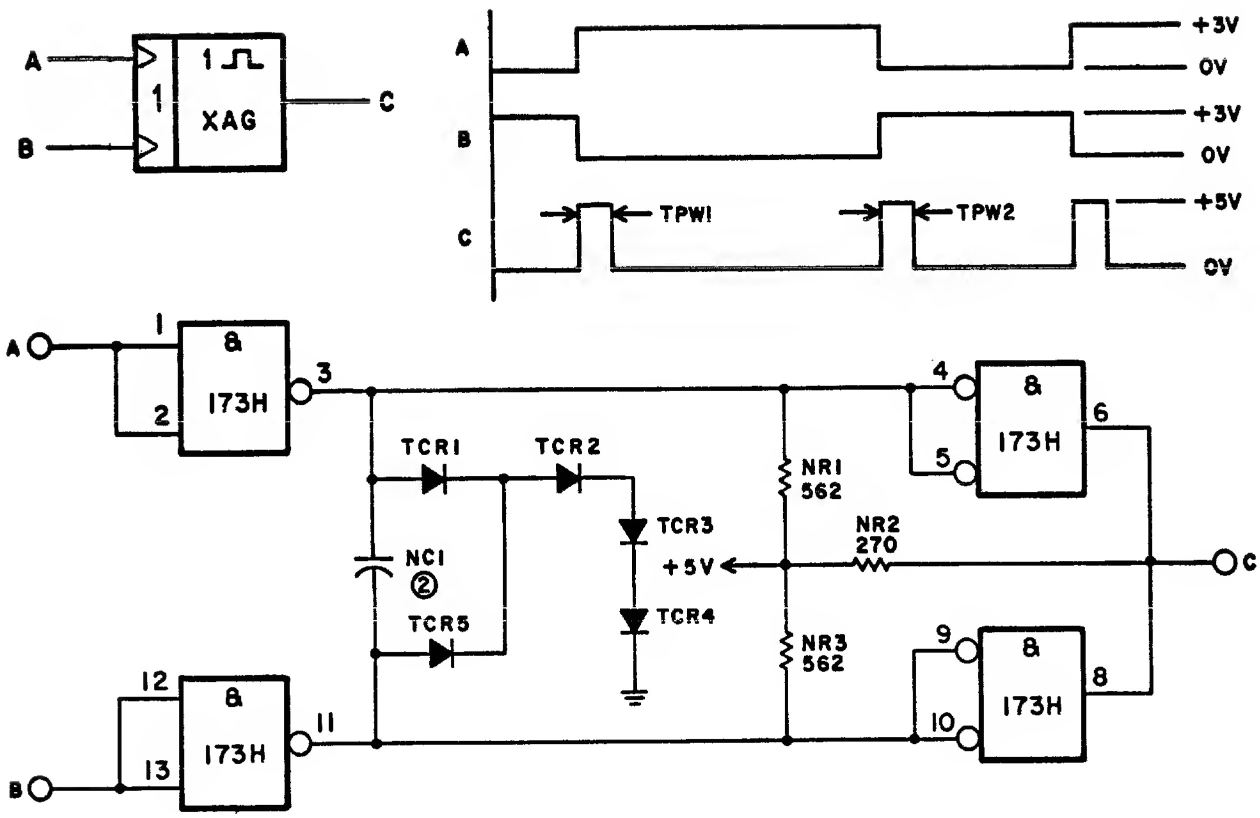
PULSE FORMER-XAF

The XAF circuit generates a negative pulse at output C for each positive going transition at either input A or B. Inputs and outputs are TTL compatible levels.

A negative going transition ("0") on input A and a positive going transition ("1") on input B cause a transition to ground at pin 3 of 173H (open collector IC) and a transition toward +5 volts at pin 11 through resistor A3R1. The "0" going transition is coupled through capacitor A3C1 and forces a negative spike on pin 11. This causes a delay in reaching the switching threshold of the output inverter, producing a negative pulse (TPW1) at output C for the duration of the delay (pulse width is determined by RC network A3C1 and A3R1).

The opposite condition on inputs A and B form the next pulse except using the RC network A3C1 and A3R2.

A3CR1, A3AR2 and A3CR3 clamp the positive excursion on pins 3 and 11 at approximately +2.2 volts to make the pulse width insensitive to repetition frequency variation up to 4 MHz and 50% duty cycle.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

② D2 = 150PF
   E2 = 100PF

7J92A

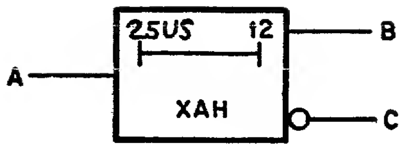
PULSE GENERATOR – XAG

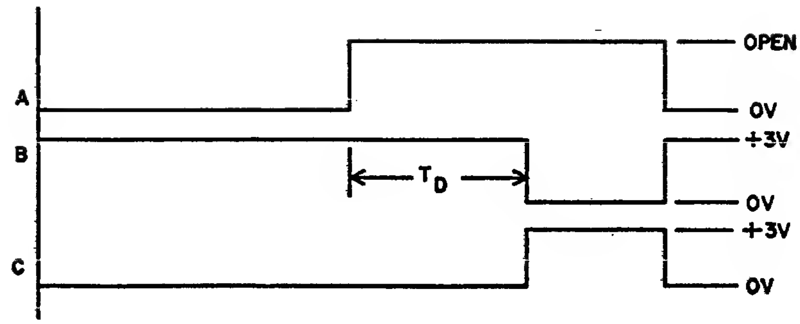
The XAG circuit generates a positive pulse output at C for each positive going transition at either input A or B. Inputs and outputs are TTL compatible levels.

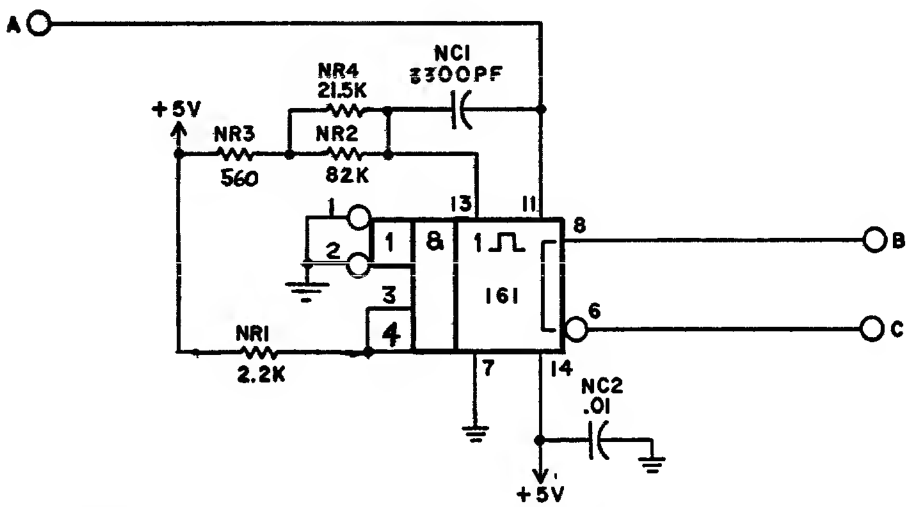
A positive going transition ("1") on input A and a negative going transition ("0") on input B cause a transition to ground at pin 3 of 173H (open collector IC) and a transition toward +5 volts at pin 11 of 173H through resistor NR3. The "0" going transition is coupled through capacitor NC1 and forces a negative spike on pin 11. Therefore, the voltage at pin 11 starts from a negative level and rises toward +5 volts at an RC time rate determined by NC1 and NR3. This causes a delay in reaching the switching threshhold of the following inverter and produces a positive pulse at "OR'ed" output C for the duration of this delay (TPW1).

The opposite conditions on inputs A and B form the positive pulse (TPW2) at "OR'ed" output C determined by the RC network of NC1 and NR1.

TCR1, TCR2, TCR3, TCR4, and TCR5 clamp the positive excursion on pins 3 and 11 at approximately +2.5 volts to make the pulse width insensitive to repetition frequency variation up to 4 MHz and 50% duty cycle.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J109

DELAY – XAH

The XAH circuit consists of a one shot integrated circuit (with external RC network) used in an application which results in delayed outputs rather than one shot pulse outputs.

A "0" (0V to +.5V) at input A (pin 11) causes outputs B and C to remain in an inactive state, "1" and "0" respectively.

When input A is released or open, the delay time out begins. At the end of the delay time, outputs B and C change state to a "0" and "1" respectively. The delay time is approximated by TD=.32 RC, where C=NC1 and R=NR3 + NR2//NR4. A return to a "0" at input A immediately resets outputs B and C to their original states of "1" and "0" respectively.

An open collector output integrated circuit such as a 173H or 200 is used to provide the described input conditions at A.

Resistor RN1 is an input gate pullup to insure a constant "1" condition on pins 3 and 4.

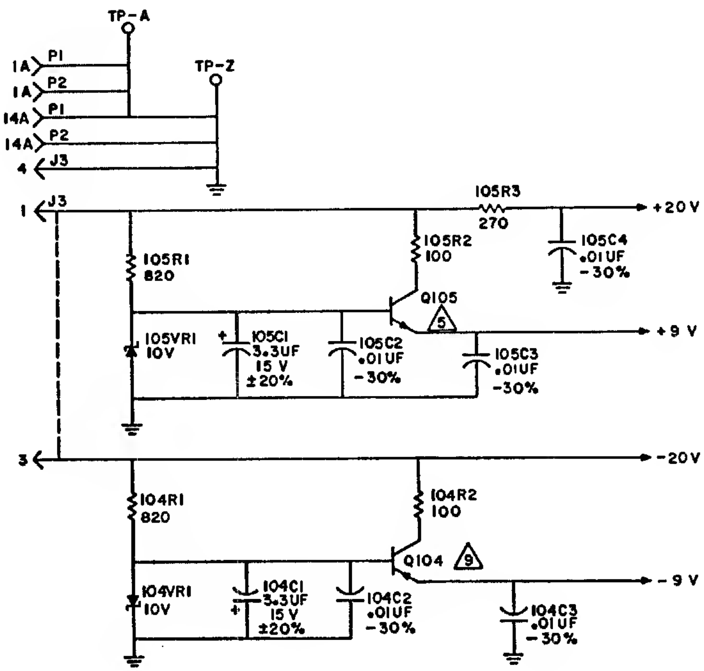
SECTION 4

CARD DIAGRAMS

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED		5-4-72		

REVISION RECORD



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL TRANSISTORS, SPNP, 2N4916, 50211610.
   ALL DIODES, SILICON, 24553500.
2. IC, TSTR ARRAY, CA3018, 50251100.
3. TSTR, DUAL SNPN , 24551000.
4. TSTR, SNPN, 2N3646, 50210310.
5. TSTR, SNPN, 2N3569, 50210811.
6. TSTR, SNPN, 50210104.
7. TSTR, SPNP, MATCHED PAIR, 50212201.
8. DIODE, SILICON, ZENER, 4.1V, 92115027.
9. TRANSISTOR, SPNP, 2N3638, 50210610.
10. TRANSISTOR, SPNP, 2N4258, 50211510.
11. SEE TABLE I FOR CHANNELS 0 THRU 18, TRANSISTOR, TEST POINT, RESISTOR, DIODE, AND CAPACITOR TRANSPOSITION.
12. BUS LINES TO CHANNELS 1 THRU 18.
13. PIN 10, U-103, IS CONNECTED TO -9V.

72829706

REFERENCE DRAWINGS
COMP ASSY: 72829606

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON 8R3A3

DWN	D. Macke	4-24-72
CHK	H. Hanson	
ENGR	B. Young	
MFG		
APPR		

TITLE

SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP

CODE IDENT		DRAWING NUMBER	CD
19333	C	72829706	0

SHEET 1 OF 3

1100

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

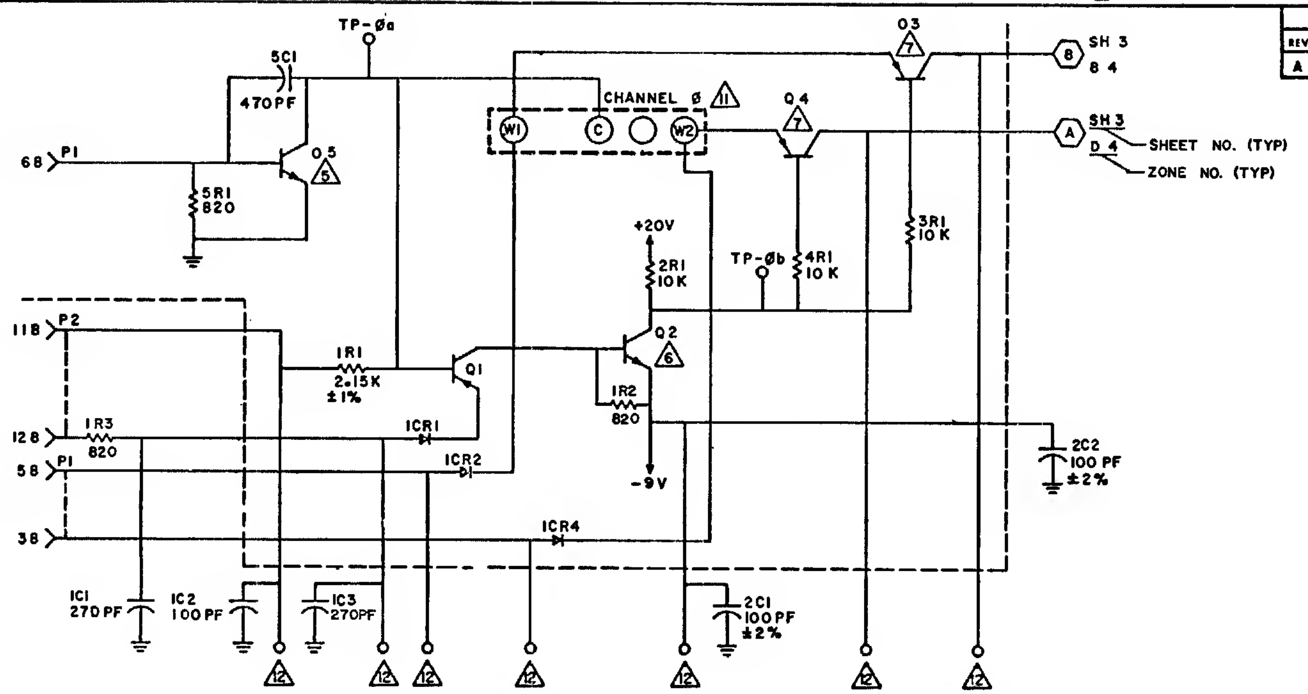


TABLE I 11

CHANNEL	I/P PIN	TSTR	TSTR 6	TSTR 7	TSTR 7	TSTR 5	TEST POINT	TEST POINT	RES	RES	RES	RES	RES	RES	DIODE	DIODE	CAP	DIODE
Ø	P1-68	Q1	Q2	Q3	Q4	Q5	Øa	Øb	1R1	2R1	4R1	3R1	5R1	1R2	1CR1	1CR2	5C1	1CR4
1	78	Q6	Q7	Q8	Q9	Q10	1a	1b	6R1	7R1	9R1	8R1	10R1	6R2	6CR1	6CR2	10C1.	6CR4
2	8A	Q11	Q12	Q13	Q14	Q15	2a	2b	11R1	12R1	14R1	13R1	15R1	11R2	11CR1	11CR2	15C1	11CR4
3	88	Q16	Q17	Q18	Q19	Q20	3a	3b	16R1	17R1	19R1	18R1	20R1	16R2	16CR1	16CR2	20C1	16CR4
4	10A	Q21	Q22	Q23	Q24	Q25	4a	4b	21R1	22R1	24R1	23R1	25R1	21R2	21CR1	21CR2	25C1	21CR4
5	118	Q26	Q27	Q28	Q29	Q30	5a	5b	26R1	27R1	29R1	28R1	30R1	26R2	26CR1	26CR2	30C1	26CR4
6	11A	Q31	Q32	Q33	Q34	Q35	6a	6b	31R1	32R1	34R1	33R1	35R1	31R2	31CR1	31CR2	35C1	31CR4
7	128	Q36	Q37	Q38	Q39	Q40	7a	7b	36R1	37R1	39R1	38R1	40R1	36R2	36CR1	36CR2	40C1	36CR4
8	12A	Q41	Q42	Q43	Q44	Q45	8a	8b	41R1	42R1	44R1	43R1	45R1	41R2	41CR1	41CR2	45C1	41CR4
9	P1-13A	Q46	Q47	Q48	Q49	Q50	9a	9b	46R1	47R1	49R1	48R1	50R1	46R2	46CR1	46CR2	50C1	46CR4
10	P2-2A	Q51	Q52	Q53	Q54	Q55	10a	10b	51R1	52R1	54R1	53R1	55R1	51R2	51CR1	51CR2	55C1	51CR4
11	3A	Q56	Q57	Q58	Q59	Q60	11a	11b	56R1	57R1	59R1	58R1	60R1	56R2	56CR1	56CR2	60C1	56CR4
12	38	Q61	Q62	Q63	Q64	Q65	12a	12b	61R1	62R1	64R1	63R1	65R1	61R2	61CR1	61CR2	65C1	61CR4
13	48	Q66	Q67	Q68	Q69	Q70	13a	13b	66R1	67R1	69R1	68R1	70R1	66R2	66CR1	66CR2	70C1	66CR4
14	68	Q71	Q72	Q73	Q74	Q75	14a	14b	71R1	72R1	74R1	73R1	75R1	71R2	71CR1	71CR2	75C1	71CR4
15	78	Q76	Q77	Q78	Q79	Q80	15a	15b	76R1	77R1	79R1	78R1	80R1	76R2	76CR1	76CR2	80C1	76CR4
16	88	Q81	Q82	Q83	Q84	Q85	16a	16b	81R1	82R1	84R1	83R1	85R1	81R2	81CR1	81CR2	85C1	81CR4
17	9A	Q86	Q87	Q88	Q89	Q90	17a	17b	86R1	87R1	89R1	89R1	90R1	86R2	86CR1	86CR2	90C1	86CR4
18	P2-108	Q91	Q92	Q93	Q94	Q95	18a	18b	91R1	92R1	94R1	93R1	95R1	91R2	91CR1	91CR2	95C1	91CR4

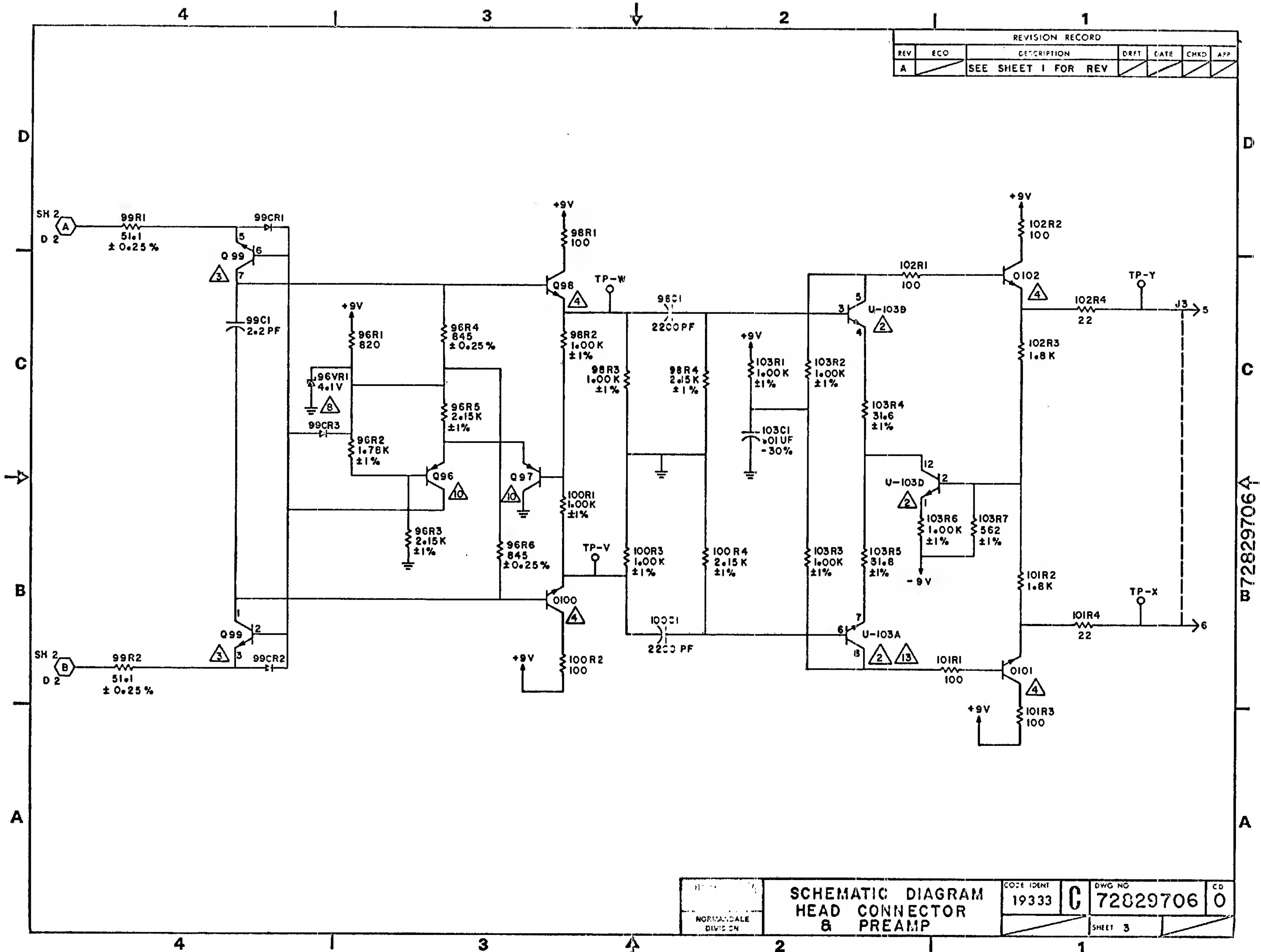
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
HEAD CONNECTOR
& PREAMP

CODE IDENT 19333 | C | DWG NO 72829706 | CD 0

SHEET 2

72829706



SCHEMATIC DIAGRAM
HEAD CONNECTOR
& PREAMP

NORMANDALE DIVISION

CODE IDENT 19333 | C | DWG NO 72829706 | CD 0

SHEET 3

B72829706

70629100 G

4-2.1/4-2.2

SHEET REVISION STATUS	REVISION RECORD						
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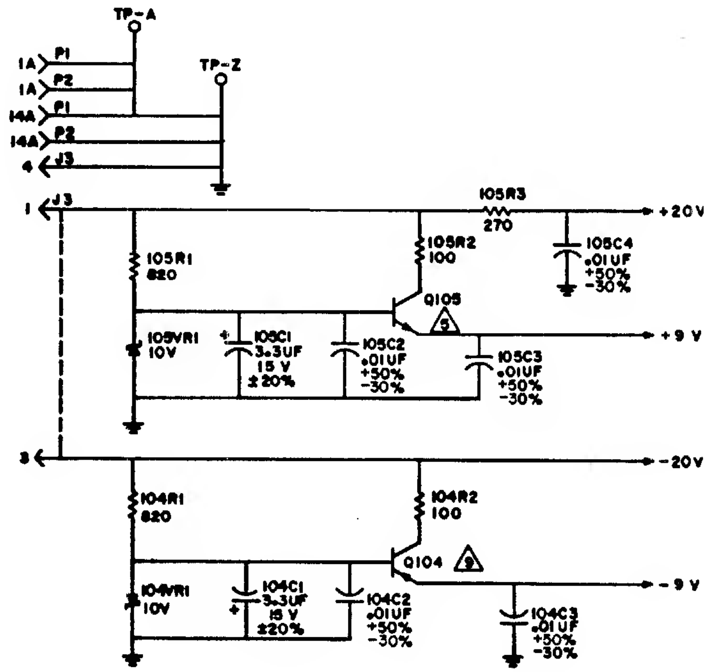
	A		RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL TRANSISTORS, SPNP, 2N4916, 50211610.
   ALL DIODES, SILICON, 24553500.
2. IC, TSTR ARRAY, CA3018, 50251100.
3. TSTR, DUAL SNPN , 24551000.
4. TSTR, SNPN, 2N3646, 50210310.
5. TSTR, SNPN, 2N3569, 50210811.
6. TSTR, SNPN, 50210104.
7. TSTR, SPNP, MATCHED PAIR, 50212201.
8. DIODE, SILICON, ZENER, 4.1V, 92115027.
9. TRANSISTOR, SPNP, 2N3638, 50210610.
10. TRANSISTOR, SPNP, 2N4256, 50211510.
11. SEE TABLE I FOR CHANNELS 0 THRU 15, TRANSISTOR, TEST POINT, RESISTOR, DIODE, AND CAPACITOR TRANSPOSITION.
12. BUS LINES TO CHANNELS 1 THRU 16.
13. PIN 10, U-103, IS CONNECTED TO -9 V.

REFERENCE DRAWINGS	
COMP A3	
COMPONENTS	
TOLERANCE	
RES	±5%	1/4 W
CAP	±10%	

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A3	
DWN		5-2-74
CHK		5-14-74
ENGR		5/16/74
MFG		
APPR		

TITLE: SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP TYPE DZPN

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	72829712	8

SHEET 1 OF 3

72829712

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

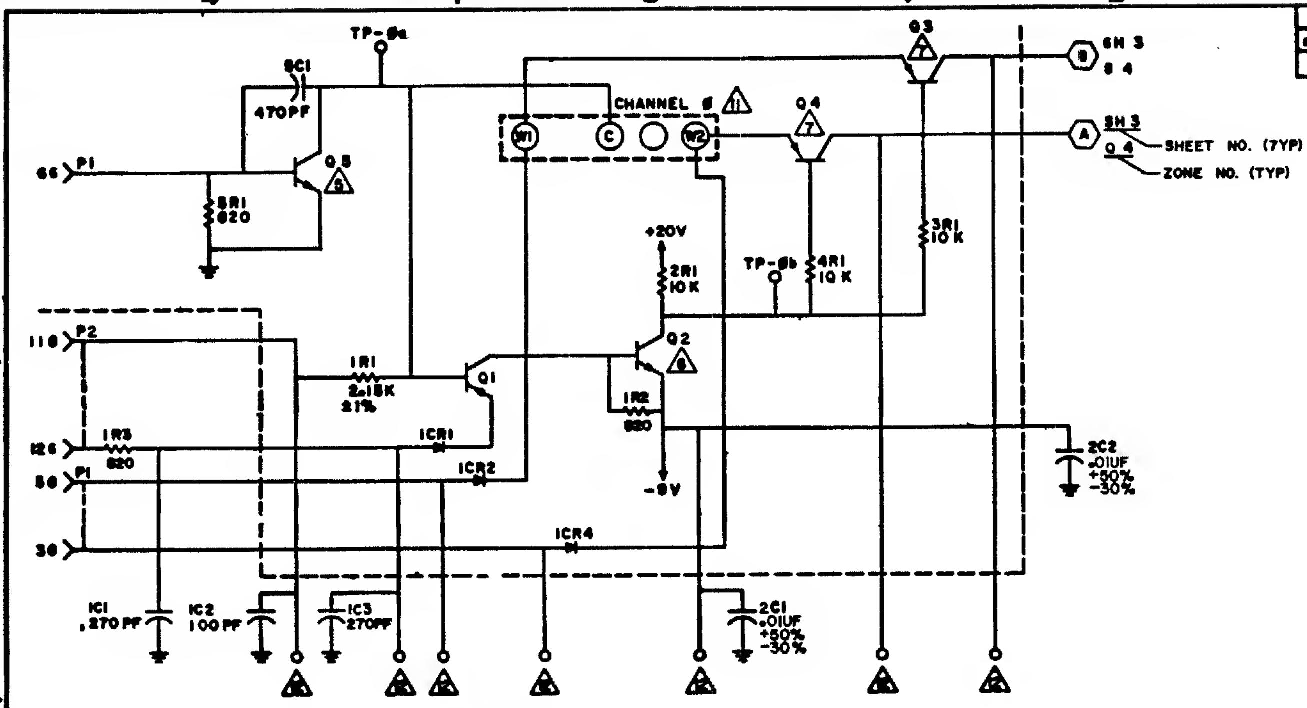


TABLE I

CHANNEL	I/P PIN	TSTR	TSTR	TSTR	TSTR	TSTR	TEST POINT	TEST POINT	RES	RES	RES	RES	RES	RES	DIODE	DIODE	CAP	DIODE
Ø	P1-66	Q1	Q2	Q3	Q4	Q5	Øa	Øb	1R1	2R1	4R1	3R1	5R1	1R2	1CR1	1CR2	5C1	1CR4
1	76	Q6	Q7	Q8	Q9	Q10	1a	1b	6R1	7R1	8R1	8R1	10R1	6R2	6CR1	6CR2	10C1	6CR4
2	6A	Q11	Q12	Q13	Q14	Q13	2a	2b	11R1	12R1	14R1	13R1	13R1	11R2	11CR1	11CR2	15C1	11CR4
3	66	Q16	Q17	Q16	Q18	Q20	3a	3b	16R1	17R1	19R1	18R1	20R1	16R2	16CR1	16CR2	20C1	16CR4
4	10A	Q21	Q22	Q23	Q24	Q25	4a	4b	21R1	22R1	24R1	23R1	25R1	21R2	21CR1	21CR2	25C1	21CR4
5	118	Q26	Q27	Q26	Q28	Q30	3a	5b	26R1	27R1	29R1	28R1	30R1	26R2	26CR1	26CR2	30C1	26CR4
6	11A	Q31	Q32	Q33	Q34	Q33	6a	6b	31R1	32R1	34R1	33R1	35R1	31R2	31CR1	31CR2	35C1	31CR4
7	128	Q36	Q37	Q38	Q39	Q40	7a	7b	36R1	37R1	39R1	38R1	40R1	36R2	38CR1	36CR2	40C1	36CR4
8	12A	Q41	Q42	Q43	Q44	Q45	8a	6b	41R1	42R1	44R1	43R1	45R1	41R2	41CR1	41CR2	45C1	41CR4
9	P1-13A	Q46	Q47	Q46	Q49	Q50	8a	9b	46R1	47R1	49R1	48R1	50R1	46R2	46CR1	48CR2	50C1	46CR4
10	P2-2A	Q51	Q52	Q53	Q54	Q55	10a	10b	51R1	52R1	54R1	53R1	55R1	51R2	51CR1	51CR2	55C1	51CR4
11	3A	Q56	Q57	Q58	Q59	Q60	11a	11b	56R1	57R1	59R1	58R1	60R1	56R2	56CR1	56CR2	60C1	36CR4
12	38	Q61	Q62	Q63	Q64	Q63	12a	12b	61R1	62R1	64R1	63R1	65R1	61R2	61CR1	61CR2	65C1	61CR4
13	48	Q66	Q67	Q68	Q68	Q70	13a	13b	66R1	67R1	69R1	68R1	70R1	66R2	66CR1	66CR2	70C1	66CR4
14	68	Q71	Q72	Q73	Q74	Q75	14a	14b	71R1	72R1	74R1	73R1	75R1	71R2	71CR1	71CR2	75C1	71CR4
15	78	Q76	Q77	Q76	Q79	Q80	15a	13b	76R1	77R1	79R1	78R1	60R1	76R2	76CR1	76CR2	60C1	76CR4
16	88	Q81	Q62	Q83	Q64	Q85	16a	16b	81R1	82R1	84R1	83R1	85R1	81R2	81CR1	61CR2	85C1	81CR4
17	9A	Q86	Q87	Q68	Q88	Q90	17a	17b	66R1	87R1	69R1	68R1	90R1	86R2	86CR1	66CR2	90C1	66CR4
18	P2-106	Q81	Q82	Q93	Q94	Q85	18a	18b	91R1	82R1	94R1	93R1	85R1	81R2	81CR1	91CR2	95C1	81CR4

NORMANDALE DIVISION

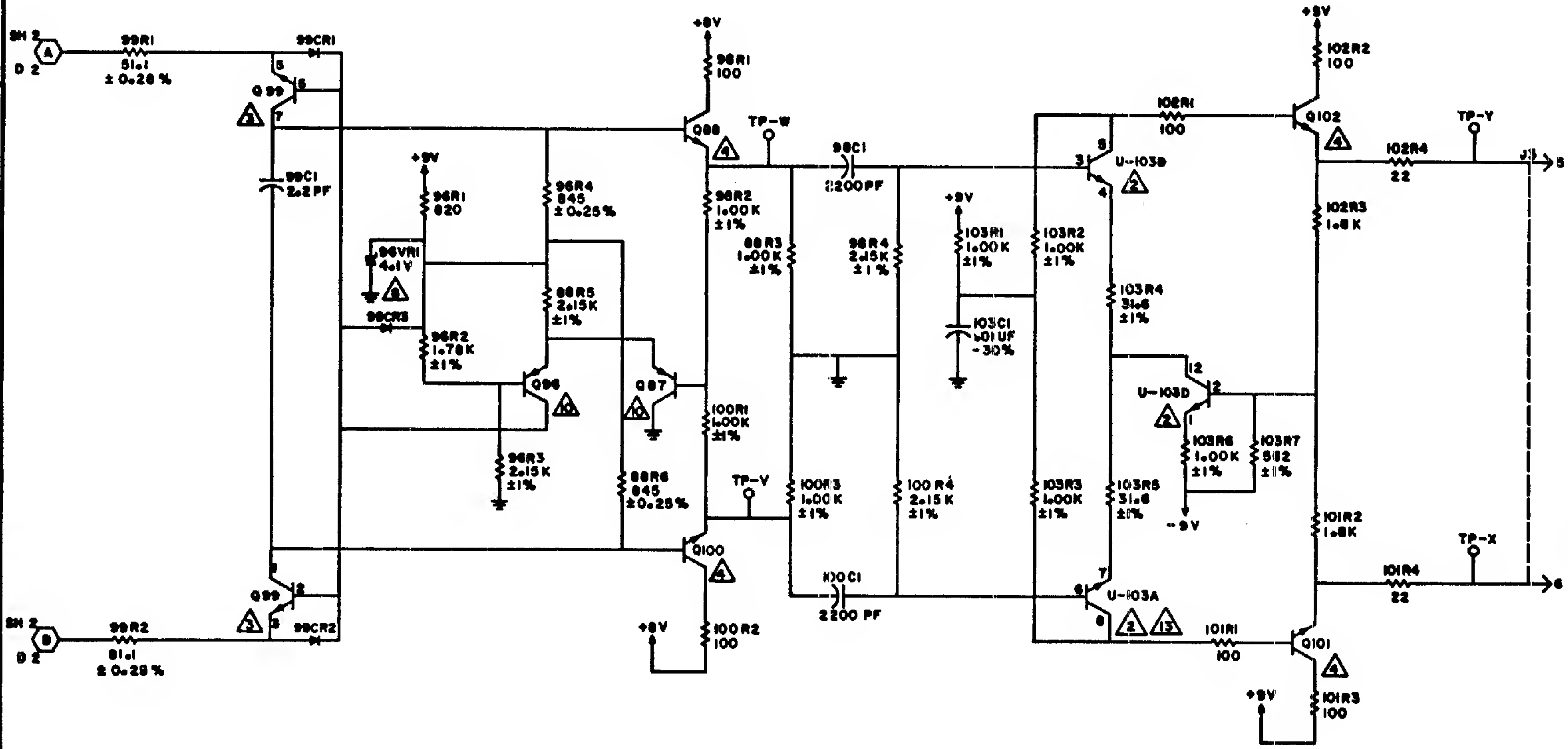
SCHEMATIC DIAGRAM
TYPE DZPN

CODE IDENT	SIZE	DWG NO	CD
19333	C	72829712	8
		SHEET 2	

72829712

70629100 G

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



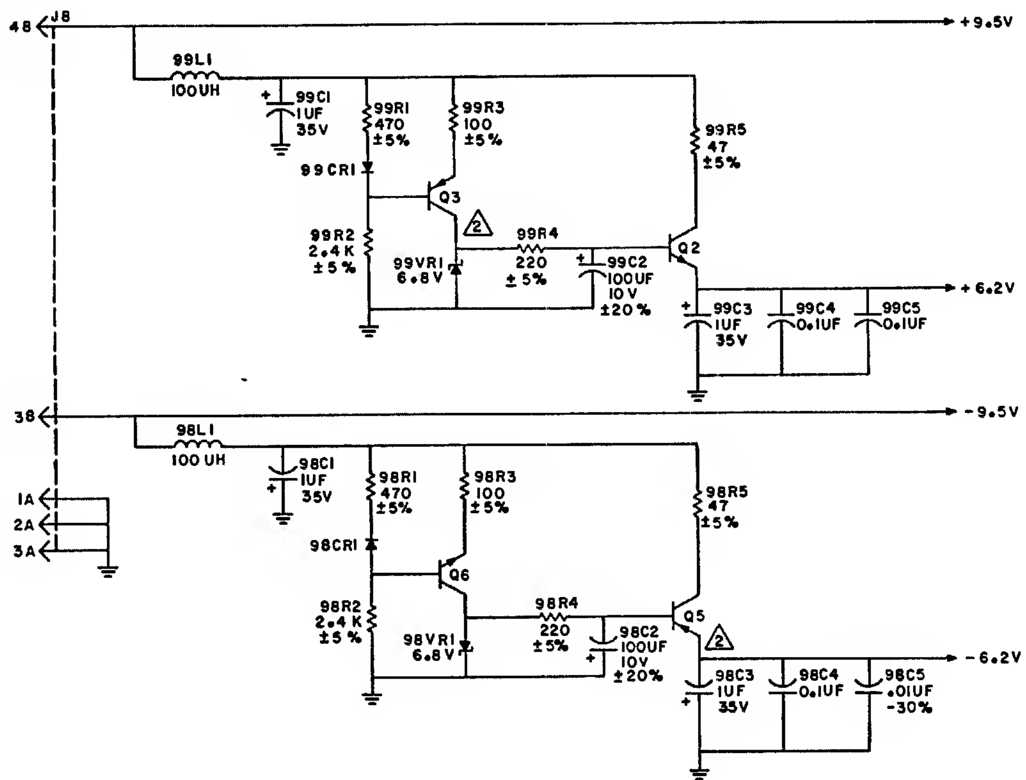
SCHEMATIC DIAGRAM TYPE DZPN	CODE IDENT 19333	C	DWG NO 72829712	CD 8
			SHEET 3	

B72829712

SHEET REVISION STATUS								

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	[illegible]	RELEASED		[illegible]		[illegible]
B	PE30380	INCREASE SERVO PREAMP GAIN	[illegible]		-	I-NR
C	PE30460	CHANGED REF DWG NO FROM 73485300 TO 73485301	[illegible]	[illegible]	-	[illegible]



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS SNPN, 2N2221, 50210102
   ALL DIODES, SILICON PLANAR, 24553500
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%.
2. TRANSISTOR, SPNP, 2N3250, 50211100.
3. IC, TYPE 309, HAS PINS 2 AND 10 CONNECTED TO GND; PIN 9 TO +6.2V; AND PINS 3 AND 4 TO -6.2V.
4. IC, TYPE 315, HAS PIN 1 CONNECTED TO GND; PIN 2 TO +6.2V; AND PINS 5 AND 11 TO -6.2V.
5. COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.

REFERENCE DRAWINGS

COMP ASSY: 73485301

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON: 8R3A1

DWN / CHK / ENGR / MFG / APPD

TITLE: SCHEMATIC DIAGRAM TRACK SERVO PREAMP

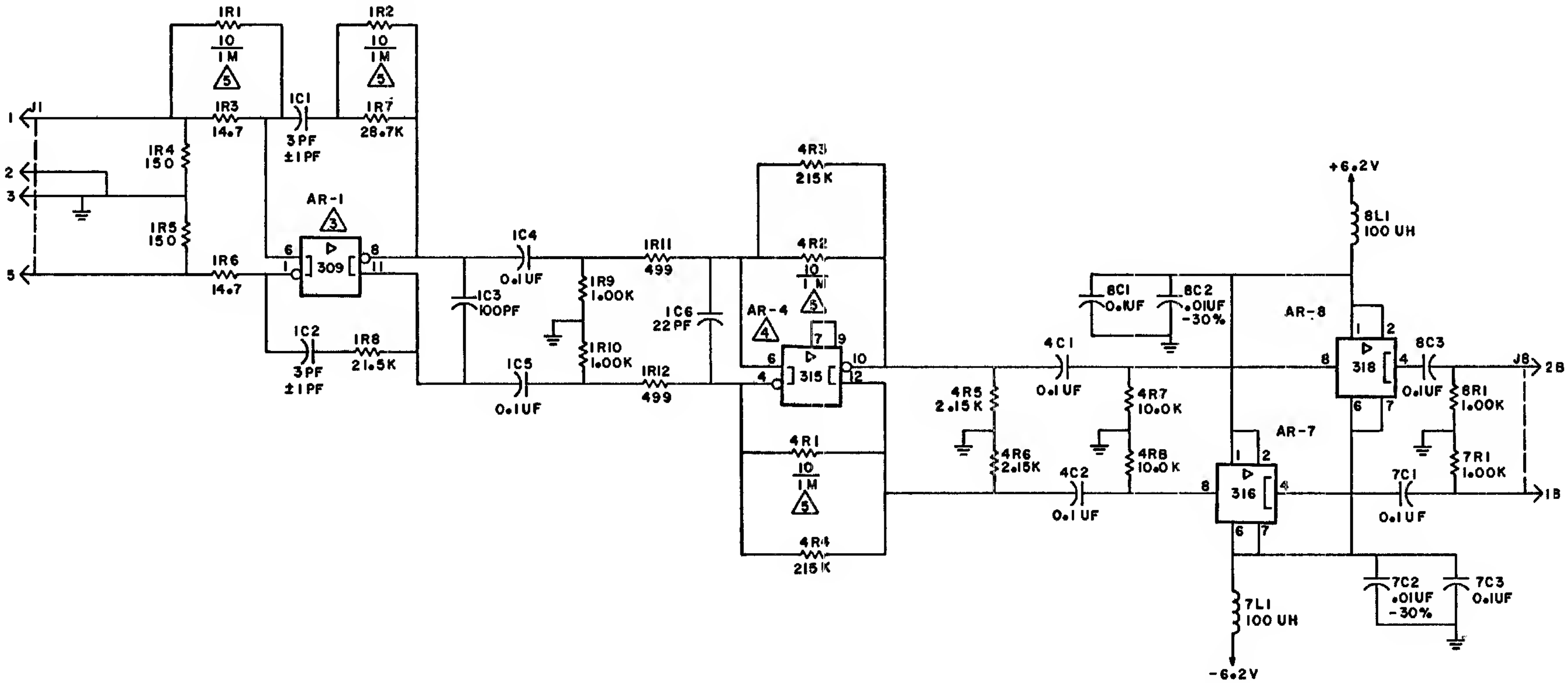
CODE IDENT 19333 | C | DRAWING NUMBER 73485400 | CD 3

SHEET 1 OF 2

HPD

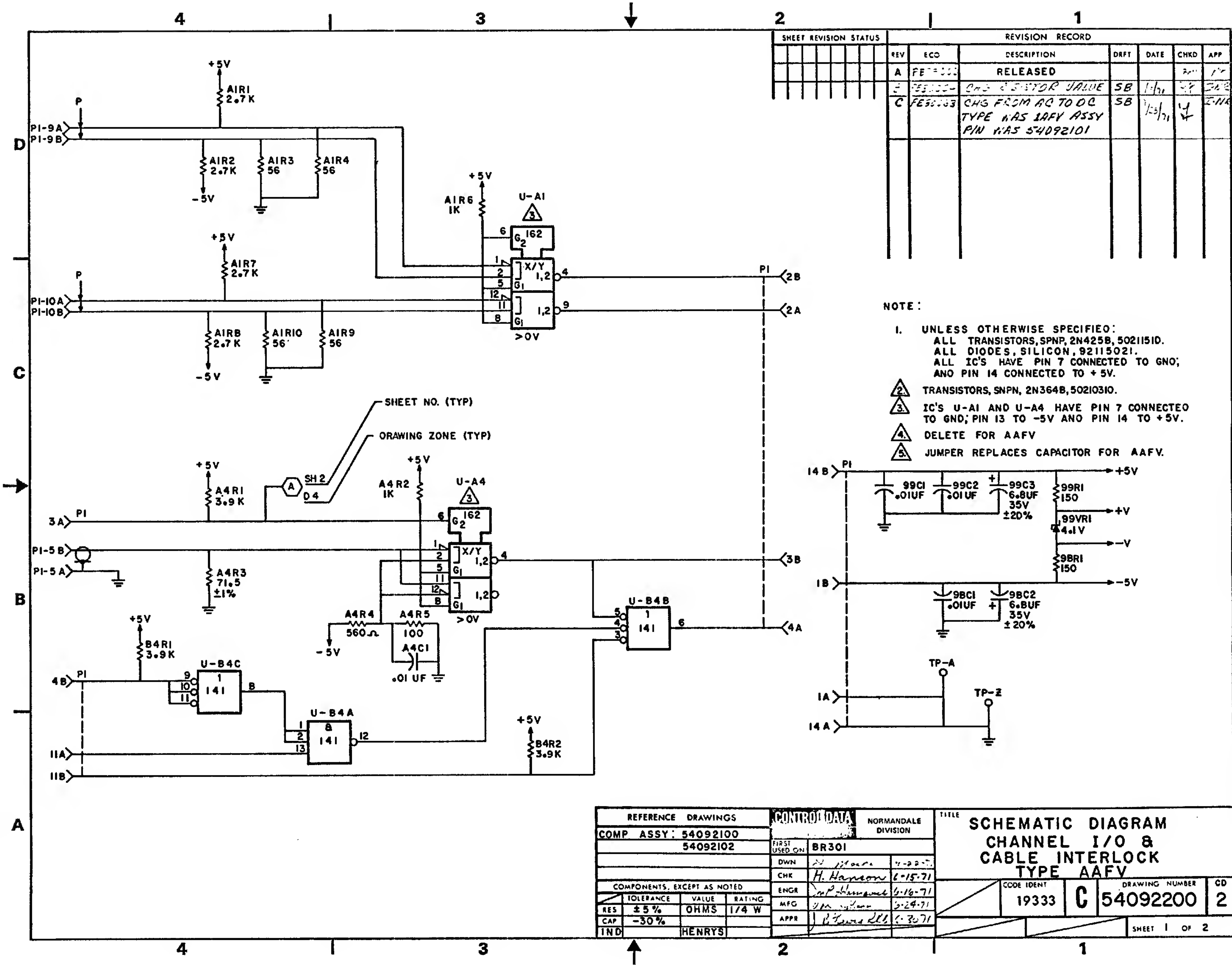
B73485400

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
C		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM TRACK SERVO PREAMP	CODE IDENT 19333	C	DWG NO 73485400	CD 3
				SHEET 2	

73485400



SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	FE	RELEASED				
B	FE	CHG RESISTOR VALUE	SB	71		
C	FE	CHG FROM AC TO DC TYPE WAS 1AFY ASSY P/N WAS 54092101	SB	71		

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N425B, 50211510.
   ALL DIODES, SILICON, 92115021.
   ALL IC'S HAVE PIN 7 CONNECTED TO GND; AND PIN 14 CONNECTED TO +5V.
2. TRANSISTORS, SNPN, 2N364B, 50210310.
3. IC'S U-A1 AND U-A4 HAVE PIN 7 CONNECTED TO GND; PIN 13 TO -5V AND PIN 14 TO +5V.
4. DELETE FOR AAFV
5. JUMPER REPLACES CAPACITOR FOR AAFV.

REFERENCE DRAWINGS			
COMP ASSY: 54092100			
54092102			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		
IND		HENRYS	

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON: BR301

DWN		7-22-71
CHK	H. Hanson	6-15-71
ENGR		6-16-71
MFG		6-24-71
APPR		6-30-71

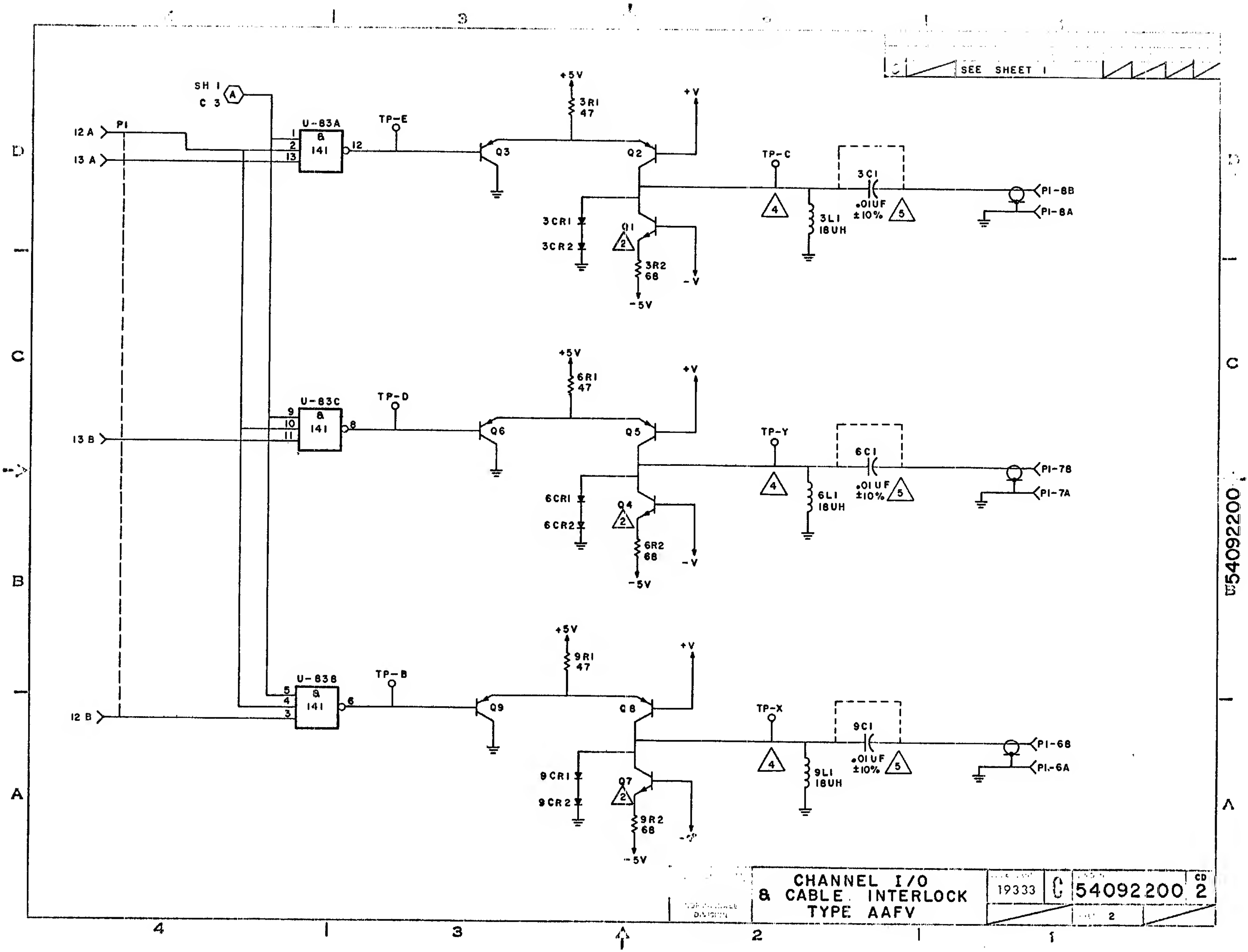
TITLE: SCHEMATIC DIAGRAM CHANNEL I/O & CABLE INTERLOCK TYPE AAFV

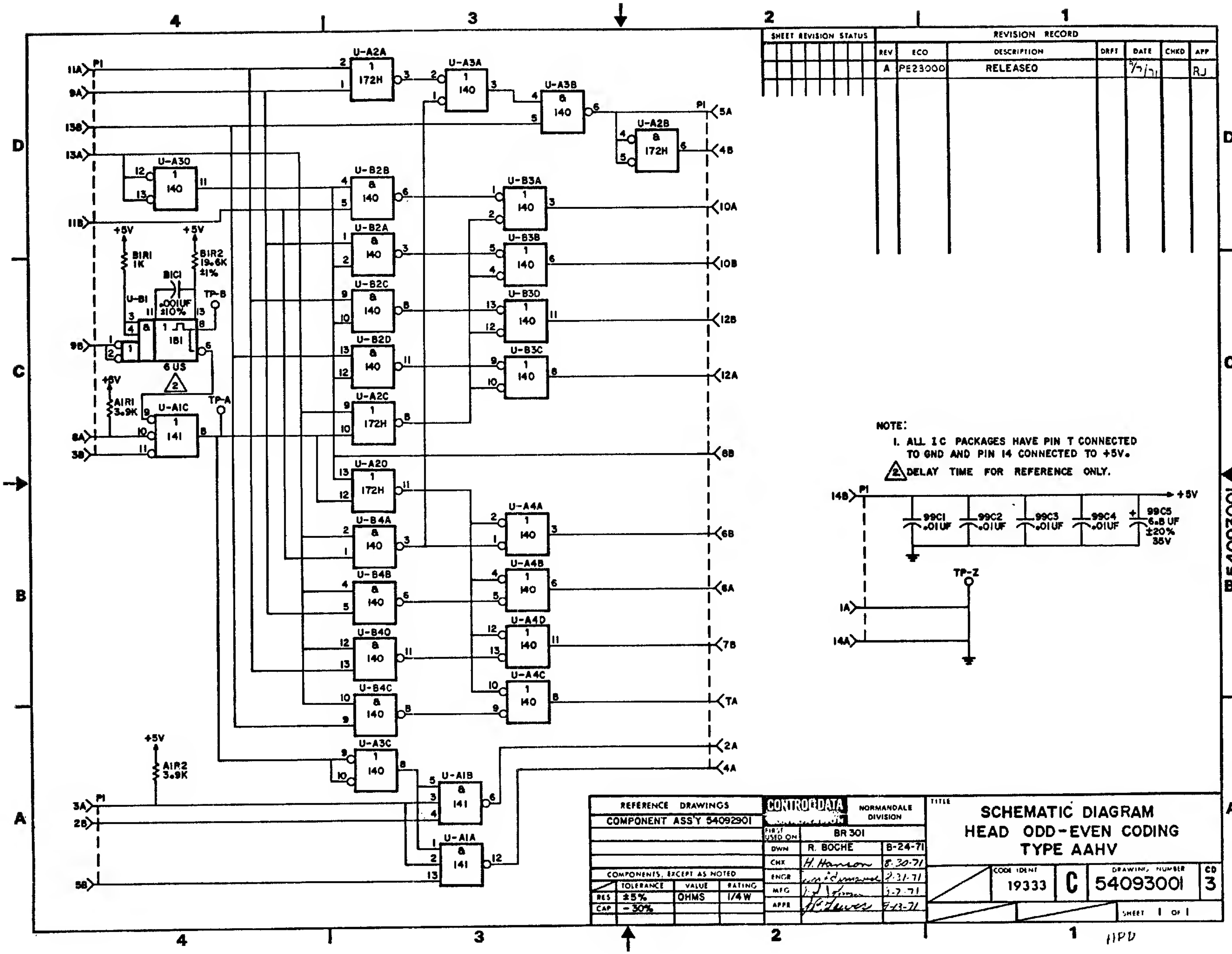
CODE IDENT 19333 | C | DRAWING NUMBER 54092200 | CD 2

SHEET 1 OF 2

54092200

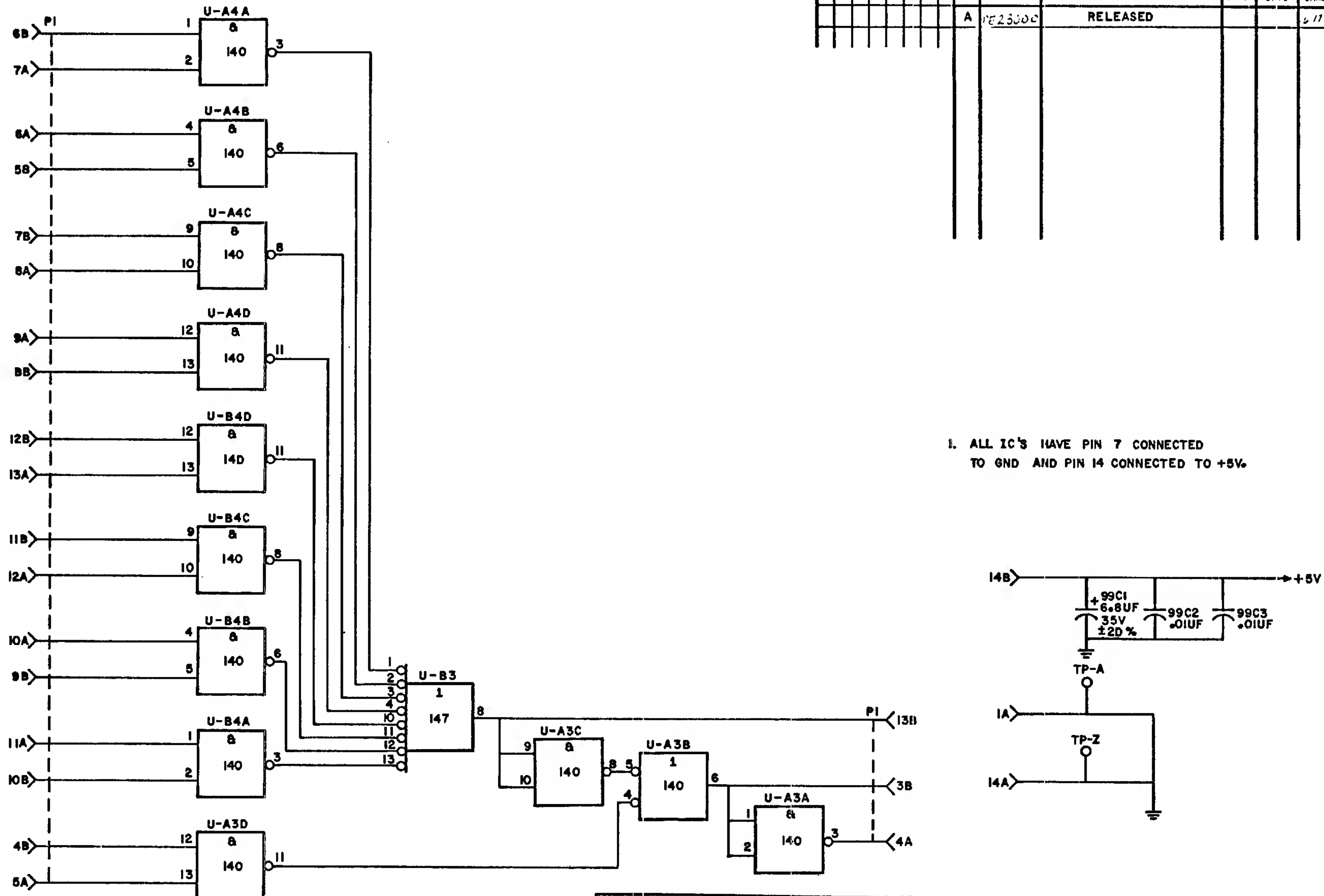
70629100 E


SH 1 C 3
A
12 A
13 A
13 B
12 B
P1
U-83A
U-83C
U-83B
141
TP-E
TP-D
TP-B
TP-C
TP-Y
TP-X
+5V
3R1 47
6R1 47
9R1 47
+V
-V
-5V
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
3CR1
3CR2
6CR1
6CR2
9CR1
9CR2
3R2 68
6R2 68
9R2 68
3L1 18UH
6L1 18UH
9L1 18UH
3C1
6C1
9C1
.01UF ±10%
P1-8B
P1-8A
P1-7B
P1-7A
P1-6B
P1-6A
SEE SHEET 1
CHANNEL I/O
& CABLE INTERLOCK
TYPE AAFV
19333
C
54092200
2



SCHEMATIC DIAGRAM
HEAD ODD-EVEN CODING
TYPE AAHV
NOTE:
1. ALL I C PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2 DELAY TIME FOR REFERENCE ONLY.
SHEET REVISION STATUS
REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A PE23000 RELEASED RJ
REFERENCE DRAWINGS
COMPONENT ASS'Y 54092901
COMPONENTS, EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHMS 1/4 W
CAP -30%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR 301
DWN R. BOCHE 8-24-71
CHK H. Hanson 8-30-71
CODE IDENT 19333
C
DRAWING NUMBER 54093001
CD 3
SHEET 1 OF 1
54093001

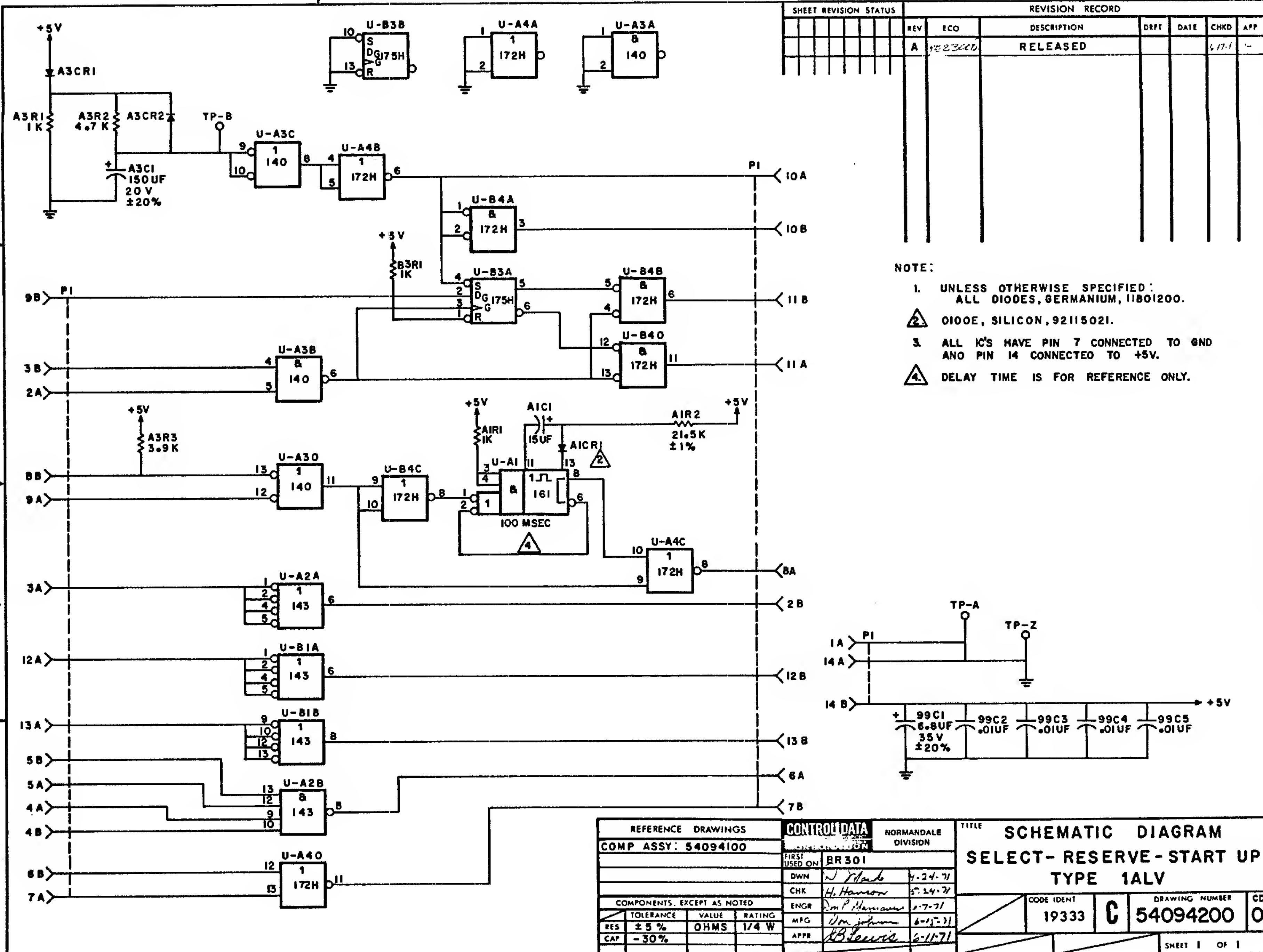
SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23500	RELEASED			6/11	9/1



1. ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

REFERENCE DRAWINGS	CONTROL DATA NORMANDALE DIVISION		TITLE
COMPONENT ASSY 54093300	FIRST USED ON	BR 301	SCHEMATIC DIAGRAM 9—BIT MULTIPLEXER TYPE 1AJV
	DWN	R. BOCHE 4-13-71	
	CHK	H. Hanson 5-27-71	
COMPONENTS, EXCEPT AS NOTED	ENGR	5-27-71	CODE IDENT 19333
TOLERANCE / VALUE / RATING	MFG	6-15-71	C
RES	APPR	6-11-71	DRAWING NUMBER 54093400
CAP -30%			C.D. 7
			SHEET 1 OF 1

54093400



SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	1823000	RELEASED			6-17-71	

NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL DIODES, GERMANIUM, 11801200.
2. DIODE, SILICON, 92115021.
3. ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
4. DELAY TIME IS FOR REFERENCE ONLY.

REFERENCE DRAWINGS

COMP ASSY: 54094100

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON: BR301

DWN	N. Mask	4-24-71
CHK	H. Hanson	5-24-71
ENGR	D. P. Hanson	6-7-71
MFG	Don Johnson	6-15-71
APPR	H.B. Lewis	6-11-71

TITLE: SCHEMATIC DIAGRAM SELECT-RESERVE-START UP TYPE 1ALV

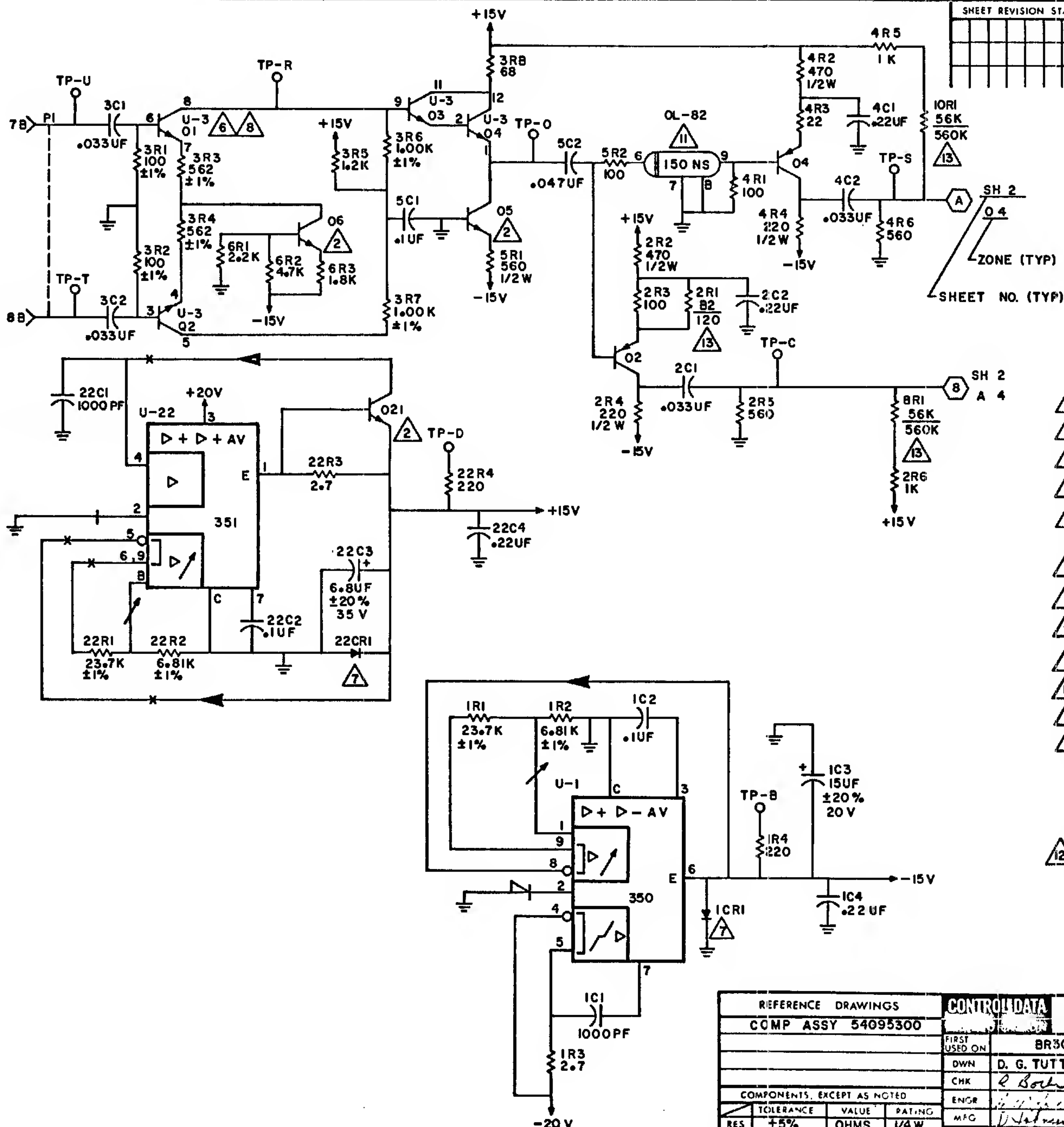
CODE IDENT 19333 — C — DRAWING NUMBER 54094200 — CD 0

SHEET 1 OF 1

54094200

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23300	RELEASED				



1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4916, 50211610.
   ALL DIODES, SILICON, 92115021

2. TRANSISTOR, SNPN, 2N3646, 50210310.

3. TRANSISTOR, SNPN, 2N3642, 50210510.

4. DIODES 9CR1, 7CR1, 15CR1, 13CR1 ARE SILICON MATCHED QUAD, 92115039.

5. DIODE, LIGHT EMITTING 94256300.

6. IC U-3, TRANSISTOR ARRAY, HAS PIN 10 CONNECTED TO BASE OF Q6.

7. DIODE, GERMANIUM, 11801200.

8. TRANSISTOR ARRAY, 50251100.

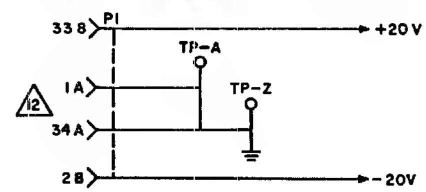
9. TRANSISTORS Q8, Q10 ARE SPNP, MATCHED PAIR, 50211612.

10. TRANSISTORS Q13, Q15 ARE SNPN, MATCHED PAIR, 50210311.

11. DELAY LINE, 94262304

12. ALL "A" ROW PINS GROUNDED.

13. RESISTORS 2R1, 8R1, 10R1 AND 11R1 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.



REFERENCE DRAWINGS	
COMP ASSY 54095300	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR301	
DWN	D. G. TUTTLE	5-25-71
CHK		7-26-71
ENGR		
MFG		
APPR		7-4-71

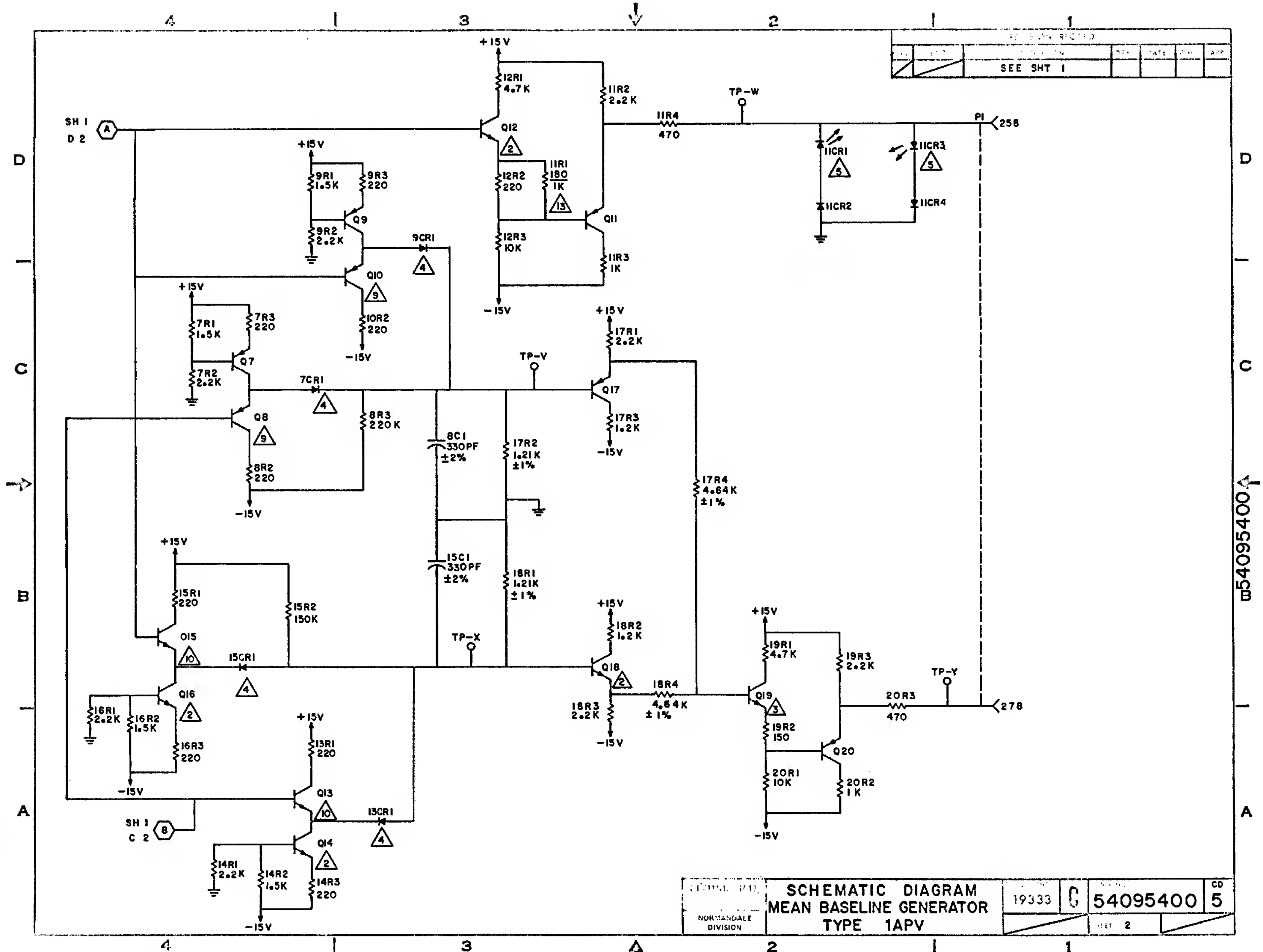
TITLE
SCHEMATIC DIAGRAM MEAN BASELINE GENERATOR TYPE 1APV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54095400	5

SHEET 1 OF 2

54095400

HPD


SEE SHT 1
SH 1 D 2
A
+15V
12R1 4.7K
11R2 2.2K
Q12
2
12R2 220
11R1 180 1K
13
Q11
12R3 10K
11R3 1K
-15V
11R4 470
TP-W
P1
258
11CR1
5
11CR2
11CR3
5
11CR4
9R1 1.5K
9R3 220
Q9
9R2 2.2K
9CR1
4
Q10
9
10R2 220
7R1 1.5K
7R3 220
Q7
7R2 2.2K
7CR1
4
Q8
9
8R3 220K
8R2 220
8C1 330PF ±2%
17R2 1.21K ±1%
TP-V
17R1 2.2K
Q17
17R3 1.2K
17R4 4.64K ±1%
15C1 330PF ±2%
18R1 1.21K ±1%
15R1 220
15R2 150K
Q15
10
15CR1
4
TP-X
18R2 1.2K
Q18
2
18R3 2.2K
18R4 4.64K ±1%
Q16
2
16R1 2.2K
16R2 1.5K
16R3 220
19R1 4.7K
19R3 2.2K
Q19
3
19R2 150
Q20
20R1 10K
20R2 1K
20R3 470
TP-Y
278
13R1 220
Q13
10
13CR1
4
SH 1 C 2
B
Q14
2
14R1 2.2K
14R2 1.5K
14R3 220
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
MEAN BASELINE GENERATOR
TYPE 1APV
19333
C
54095400
CD
5
SHT 2
54095400

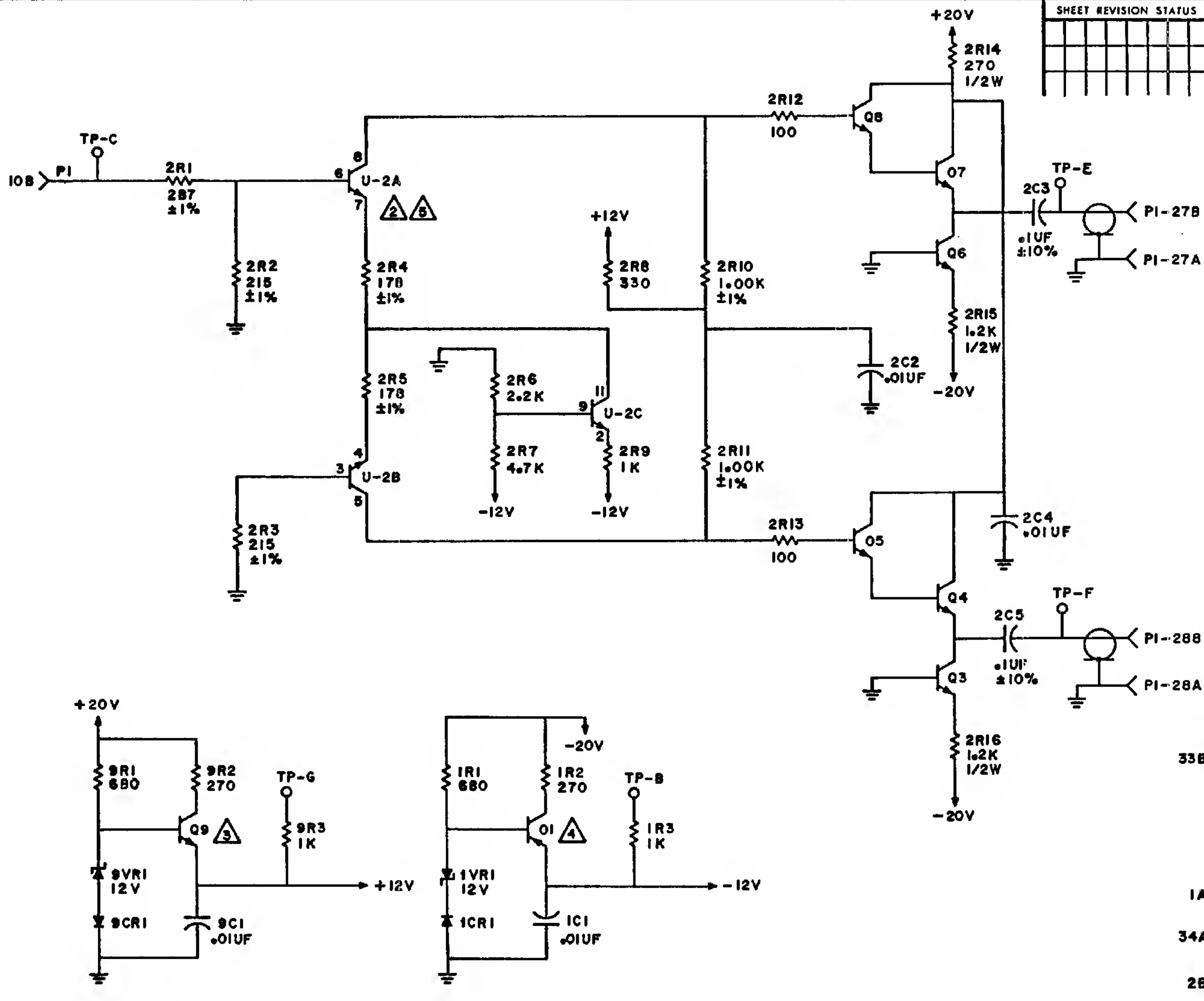
70629100 E

70629100 E

SHEET REVISION STATUS							

REVISION RECORD

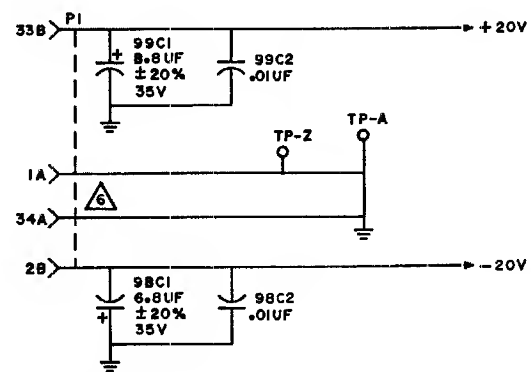
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		3-8-72		



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310.
   ALL DIODES SILICON, 92115023.
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%.

2. TRANSISTOR ARRAY, CA3018, 50251100.
3. TRANSISTOR, SNPN, 2N3569, 50210811.
4. TRANSISTOR, SPNP, 2N3638, 50210610.
5. PIN 10 OF U-2C IS CONNECTED TO PIN 9.
6. ALL ROW A PINS ON THE CONNECTOR ARE CONNECTED TO GND



REFERENCE DRAWINGS
COMPONENT ASSY 54095700

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	8R301	
DWN	R. KONECNY	1-11-72
CHK	[signature]	3-1-72
ENGR	D. Young	3-2-72
MFG	[signature]	3-6-72
APPR	[signature]	3-6-72

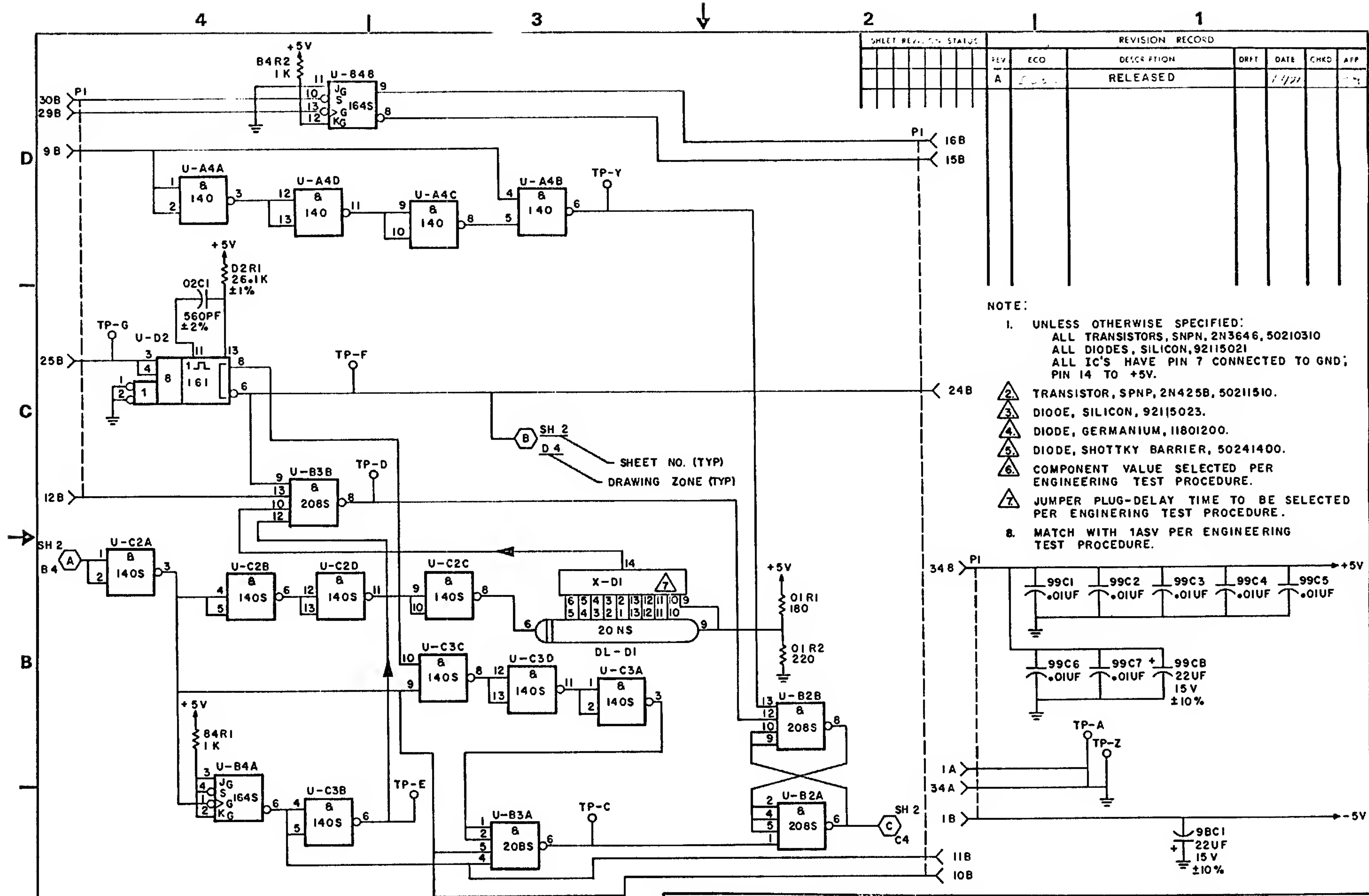
TITLE
SCHEMATIC DIAGRAM
AMPLIFIER BUFFER
TYPE 2AQV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54095800	6

SHEET 1 OF 1

HPD

54095800



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, 92115021
   ALL IC'S HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V.
2. TRANSISTOR, SPNP, 2N4258, 50211510.
3. DIODE, SILICON, 92115023.
4. DIODE, GERMANIUM, 11801200.
5. DIODE, SHOTTKY BARRIER, 50241400.
6. COMPONENT VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
7. JUMPER PLUG-DELAY TIME TO BE SELECTED PER ENGINERING TEST PROCEDURE.
8. MATCH WITH 1ASV PER ENGINEERING TEST PROCEDURE.

REFERENCE DRAWINGS
COMP ASSY: 54096100

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

BR301

DWN / CHK 9-10-71 / ENGR 9-13-71 / MFG / APPR

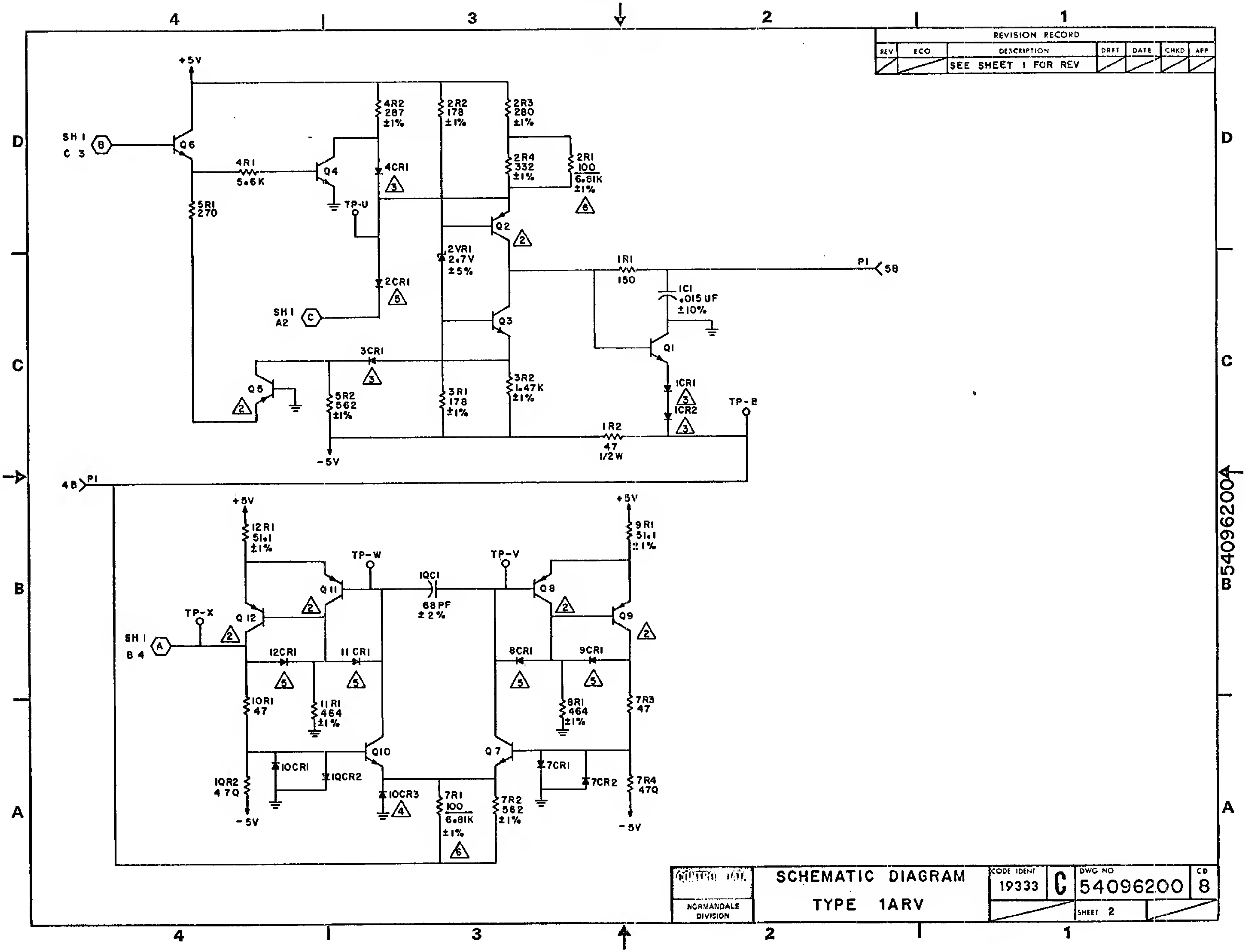
SCHEMATIC DIAGRAM
READ RECOVERY
PHASE LOCKED OSCILLATOR
TYPE 1ARV

CODE IDENT 19333 | C | DRAWING NUMBER 54096200 | CD 8

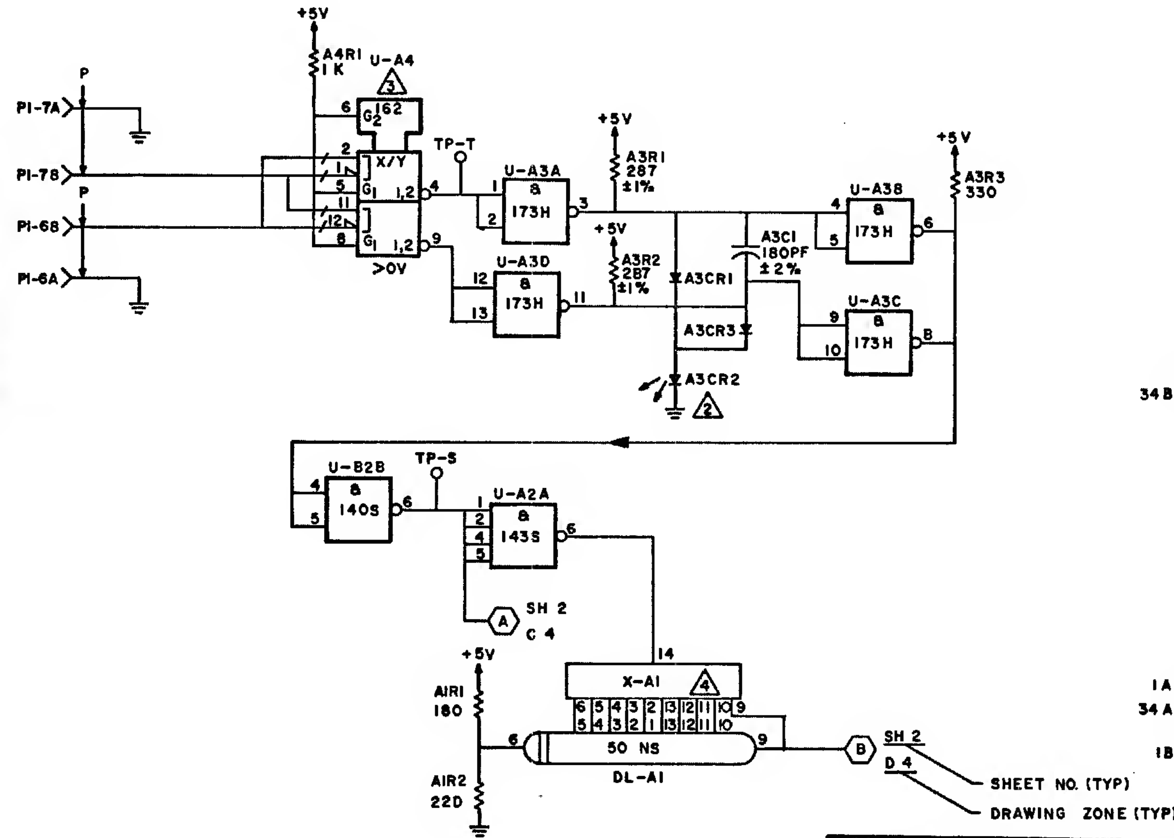
SHEET 1 OF 2

HPD

54096200

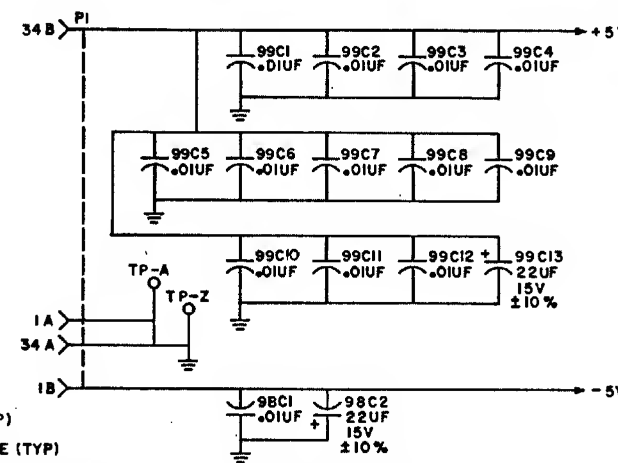

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
SEE SHEET 1 FOR REV
+5V
SH 1 C 3
B
Q6
4R1 5.6K
Q4
4R2 287 ±1%
2R2 178 ±1%
2R3 280 ±1%
2R4 332 ±1%
2R1 100 6.81K ±1%
4CR1
5R1 270
TP-U
Q2
2VR1 2.7V ±5%
2CR1
SH 1 A2
C
Q3
1R1 150
P1 5B
1C1 .015 UF ±10%
Q1
3CR1
Q5
5R2 562 ±1%
3R1 178 ±1%
3R2 1.47K ±1%
1CR1
1CR2
TP-B
1R2 47 1/2W
-5V
4B P1
12R1 51.1 ±1%
TP-W
TP-V
9R1 51.1 ±1%
Q11
1QC1 68PF ±2%
Q8
TP-X
Q12
Q9
SH 1 B 4
A
12CR1
11 CR1
8CR1
9CR1
10R1 47
11R1 464 ±1%
8R1 464 ±1%
7R3 47
Q10
Q7
10CR1
10CR2
7CR1
7CR2
1QR2 47Q
10CR3
7R1 100 6.81K ±1%
7R2 562 ±1%
7R4 47Q
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 1ARV
CODE IDENT 19333
C
DWG NO 54096200
CD 8
SHEET 2
54096200A

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	ES 23000	RELEASED		9/17/71		RH



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES, SILICON, 92115023.
   ALL IC'S HAVE PIN 7 CONNECTED TO GND, PIN 14 CONNECTED TO +5V.
2. DIODE, LIGHT EMITTING, 94256300.
3. IC U-A4 HAS PIN 13 CONNECTED TO -5V.
4. JUMPER PLUG - DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
5. MATCHED WITH 1ARV PER ENG. TEST PROCEDURE
6. DIODE, SHOTTKY BARRIER, 50241400.



REFERENCE DRAWINGS			
COMP ASSY: 54096500			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR301	
DWN		6-28-71
CHK	H. Larson	9-13-71
ENGR		9-16-71
MFG		9-16-71
APPR		9-16-71

TITLE SCHEMATIC DIAGRAM DATA SEPARATOR TYPE 1ASV

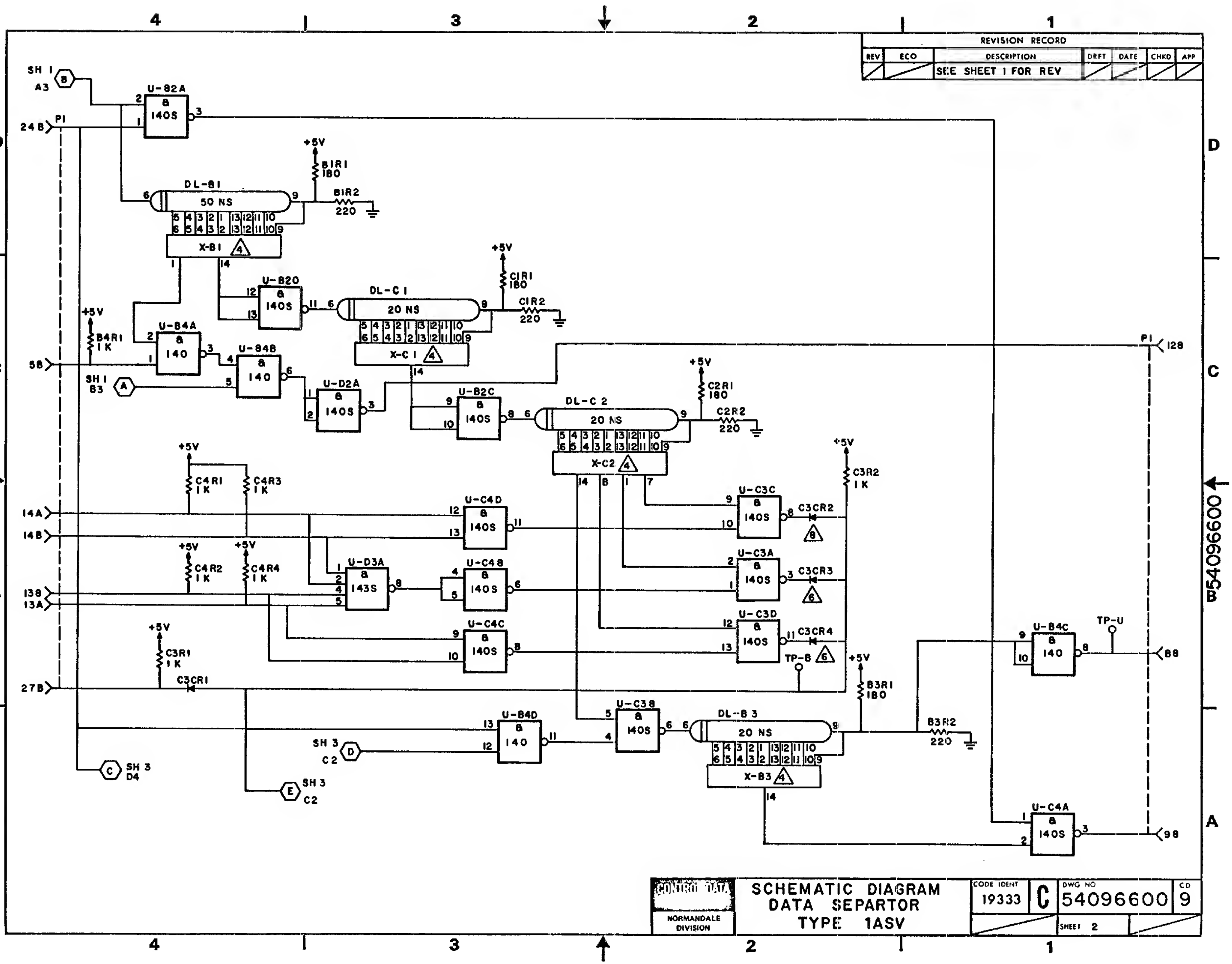
CODE IDENT 19333 — C — DRAWING NUMBER 54096600 — CD 9

SHEET 1 OF 3

HPD

54096600

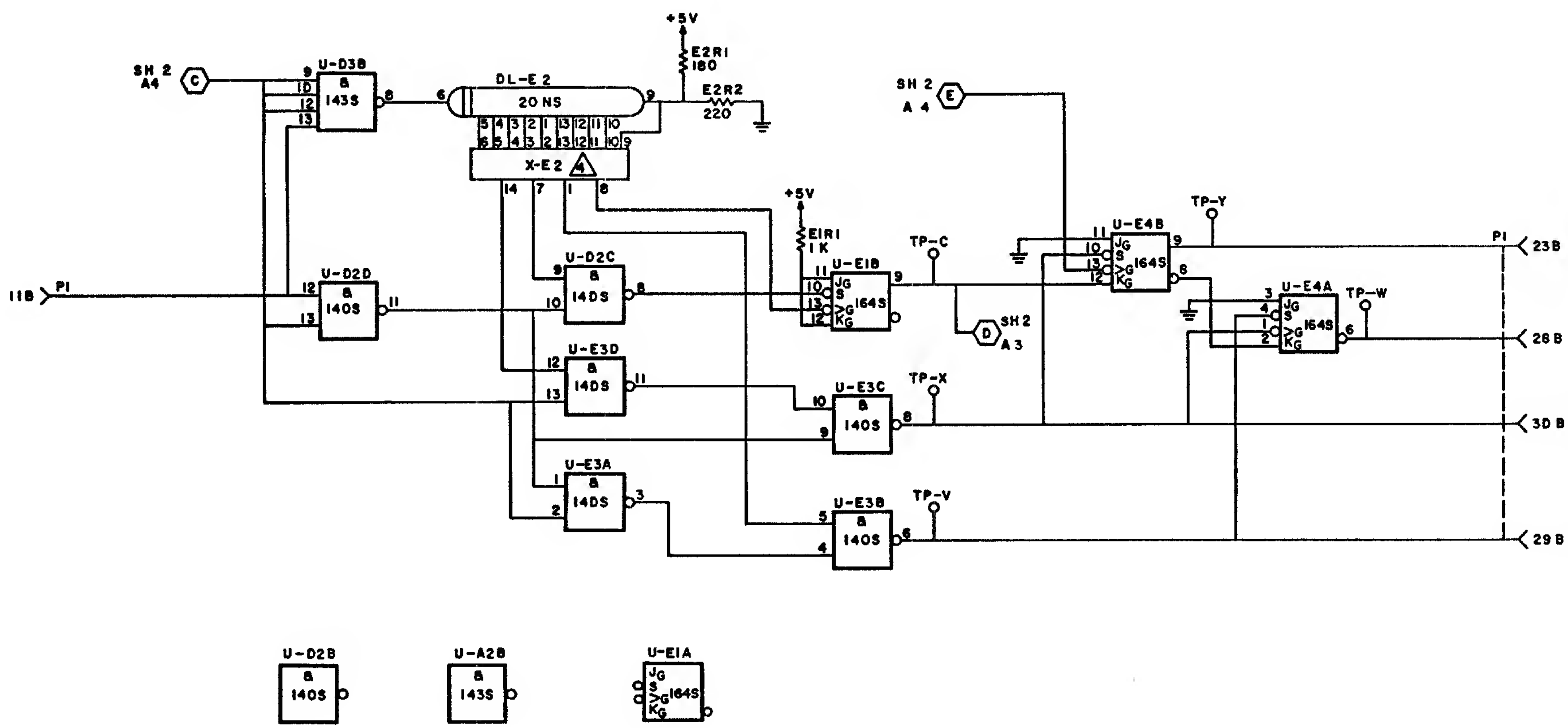
70629100 E



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
SEE SHEET 1 FOR REV
SH 1 A3 B
24B P1
U-B2A 8 140S
DL-B1 50 NS
+5V B1R1 180
B1R2 220
X-B1 4
U-B2D 8 140S
DL-C1 20 NS
+5V C1R1 180
C1R2 220
X-C1 4
+5V B4R1 1K
U-B4A 8 140
U-B4B 8 140
5B
SH 1 B3 A
U-D2A 8 140S
U-B2C 8 140S
DL-C2 20 NS
+5V C2R1 180
C2R2 220
X-C2 4
P1 12B
+5V C4R1 1K
C4R3 1K
14A
14B
U-C4D 8 140S
+5V C4R2 1K
+5V C4R4 1K
U-D3A 8 143S
U-C4B 8 140S
13B
13A
U-C4C 8 140S
U-C3C 8 140S
C3CR2 8
+5V C3R2 1K
U-C3A 8 140S
C3CR3 6
U-C3D 8 140S
C3CR4 6
TP-B
+5V C3R1 1K
C3CR1
27B
U-B4D 8 140
SH 3 C2 D
U-C3B 8 140S
DL-B3 20 NS
+5V B3R1 180
B3R2 220
X-B3 4
SH 3 D4 C
SH 3 C2 E
U-B4C 8 140
TP-U
8B
U-C4A 8 140S
9B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
DATA SEPARTOR
TYPE 1ASV
CODE IDENT 19333
C
DWG NO 54096600
CD 9
SHEET 2
54096600

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
DATA SEPARATOR
TYPE 1ASV

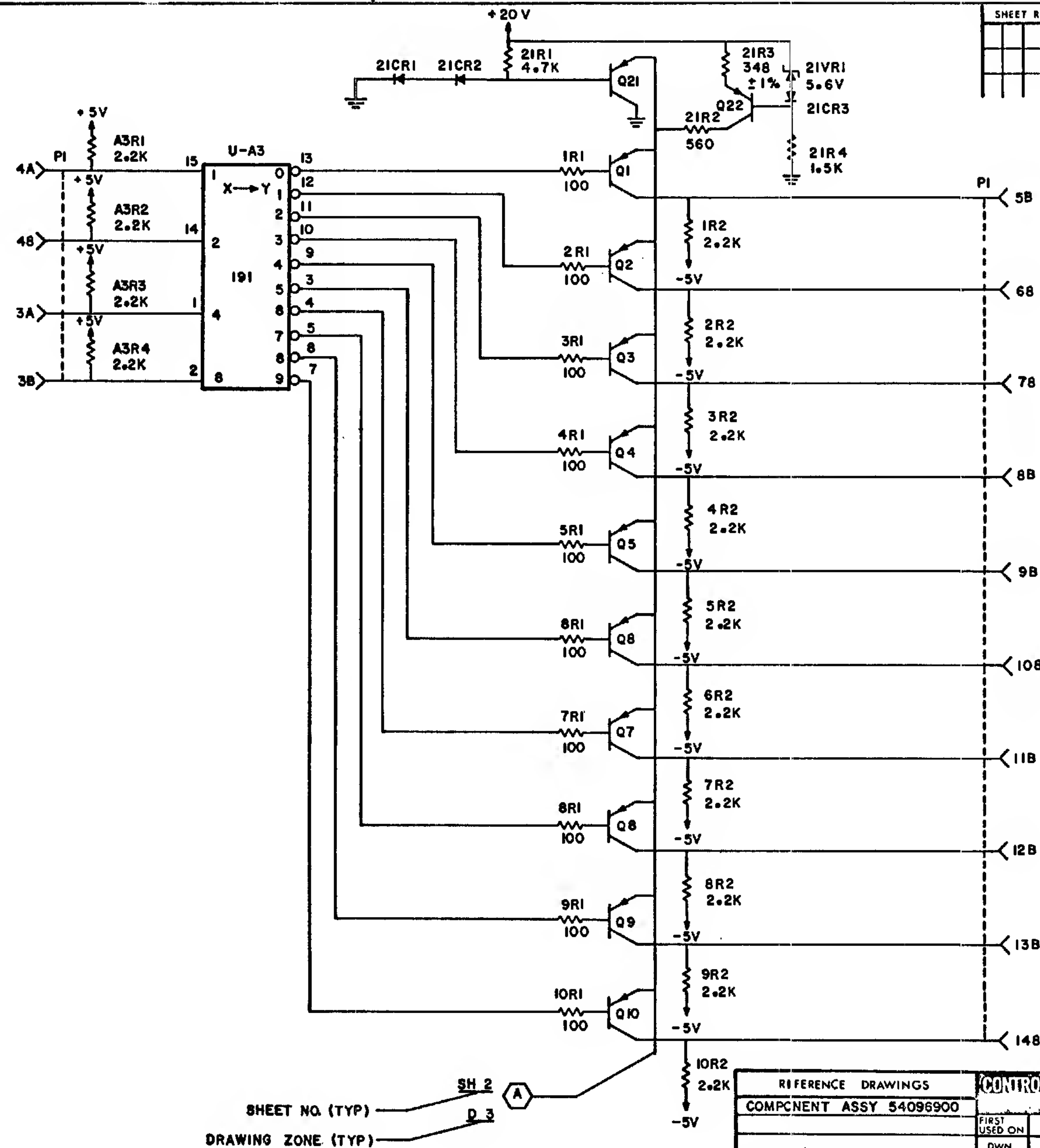
CODE IDENT 19333 | C | DWG NO 54096600 | CD 9

SHEET 3

54096600

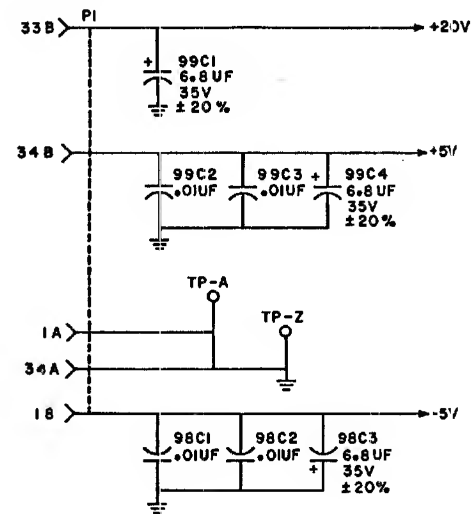
70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASE				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V
   ALL DIODES, SILICON, 92115021.
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.



REFERENCE DRAWINGS
COMPONENT ASSY 54096900

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR 301	
DWN	T. STREHLO	4-27-71
CHK		6-22-71
ENGR		7-12-71
MFG		7-22-71
APPR		7-20-71

TITLE

SCHEMATIC DIAGRAM HEAD & CHANNEL SELECTOR TYPE 1ATV

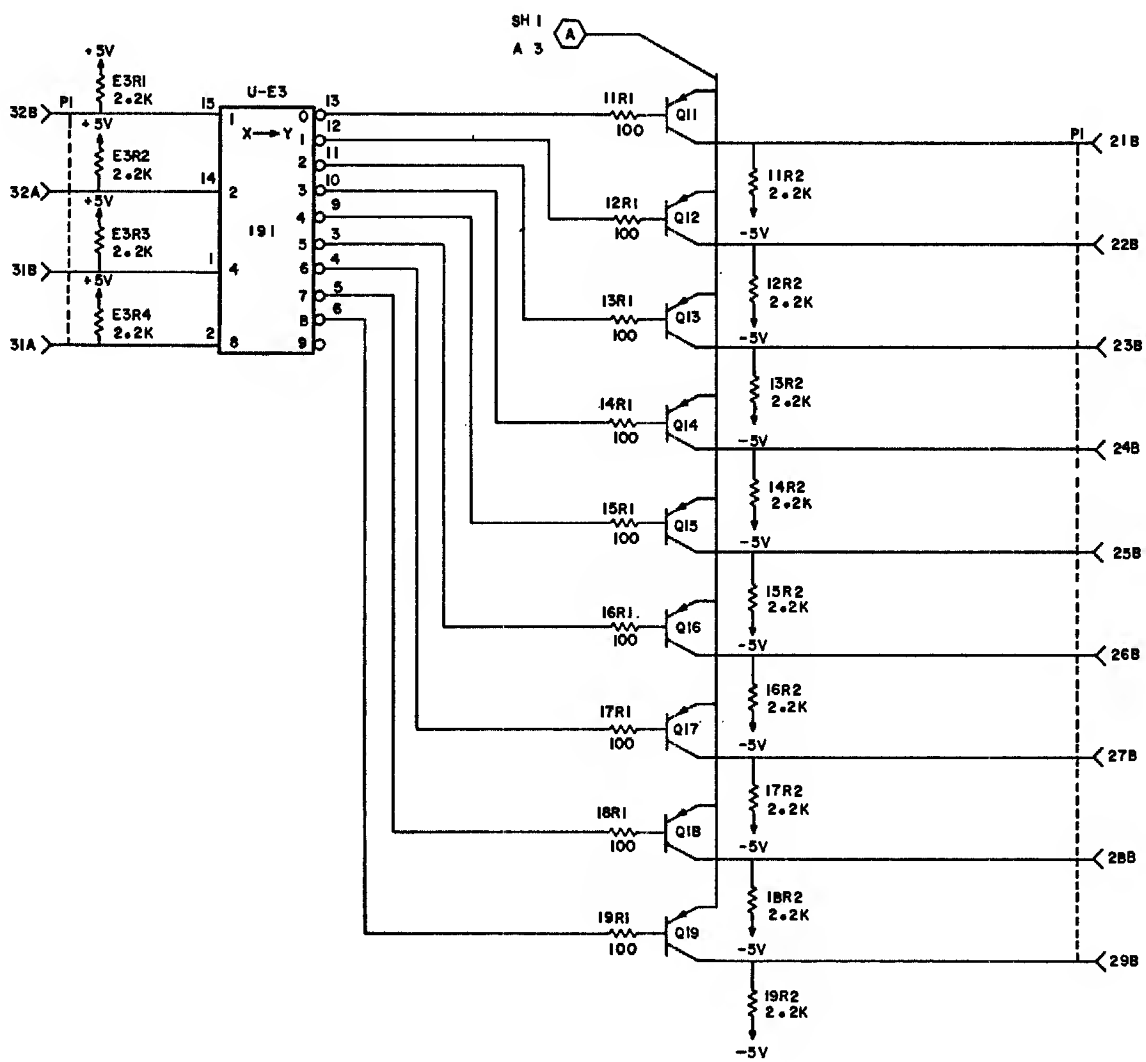
CODE IDENT		DRAWING NUMBER	CD
19333	C	54097000	1

SHEET 1 OF 2

HPD

54097000

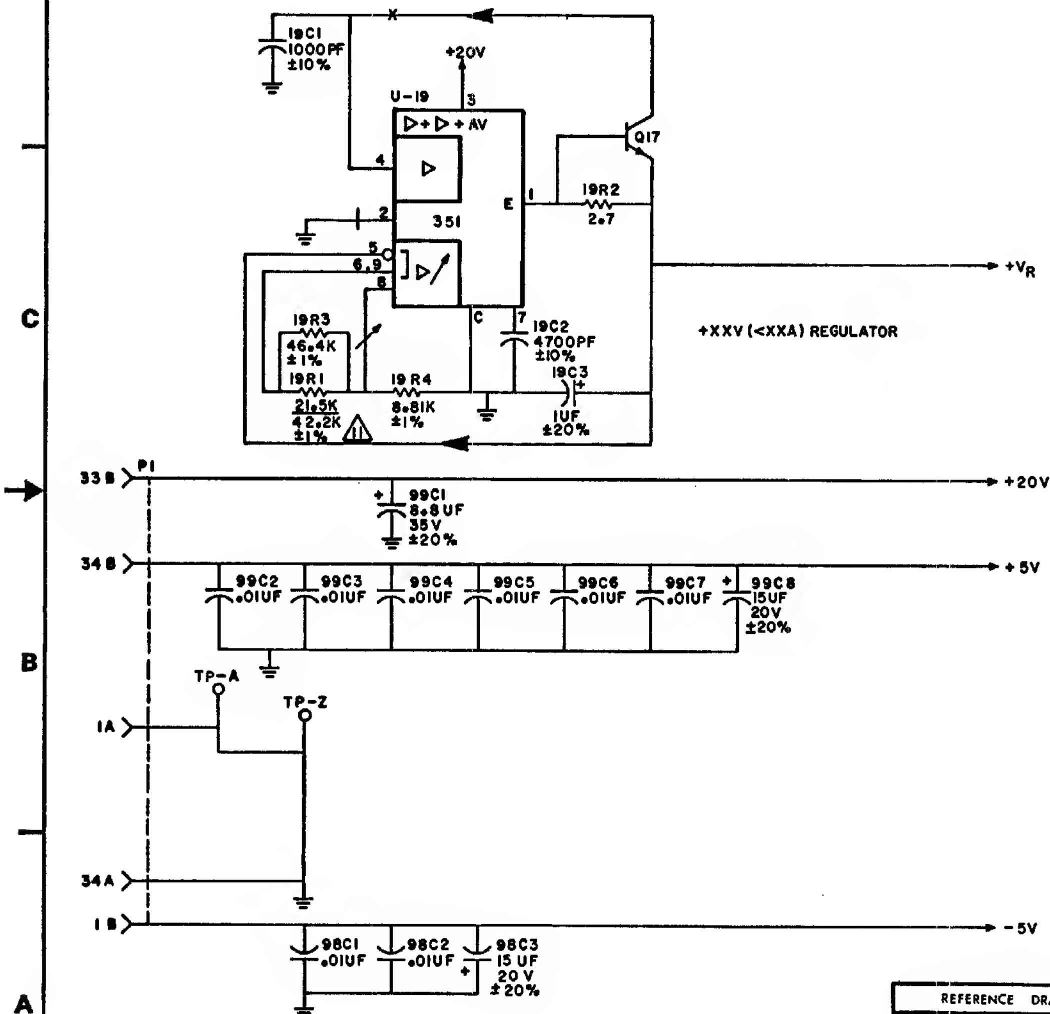
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET I FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD & CHANNEL SELECTOR TYPE 1ATV	CODE IDENT 19333	C	DWG NO 54097000	CD 1
				SHEET 2	

54097000

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, PLANAR, 24553500
   ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. TRANSISTOR, SPNP, 2N5456, 50212100
3. TRANSISTOR, SPNP, 2N4916, 50211610.
4. TRANSISTOR, SPNP, 2N4258, 50211510.
5. TRANSISTOR, SPNP, 2N3645, 50211210.
6. TRANSISTOR, SPNP, 2N3638, 50210610.
7. TRANSISTOR, SNPN, 2N4923, 50220902.
8. TRANSISTOR, SNPN, PLANAR, 24562100.
9. DIODE, SILICON, 50241400.
10. DIODE, GERMANIUM, 11801200.
11. RESISTOR SELECTED PER ENGINEERING TEST PROCEDURE.
12. IC'S U-B4 AND U-D3 HAVE PIN 7 CONNECTED TO GND, PIN 13 CONNECTED TO -5V AND PIN 14 CONNECTED TO +5V

REFERENCE DRAWINGS			
COMP ASSY: 54097301			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%	—	—

CONTROL DATA — NORMANDALE DIVISION

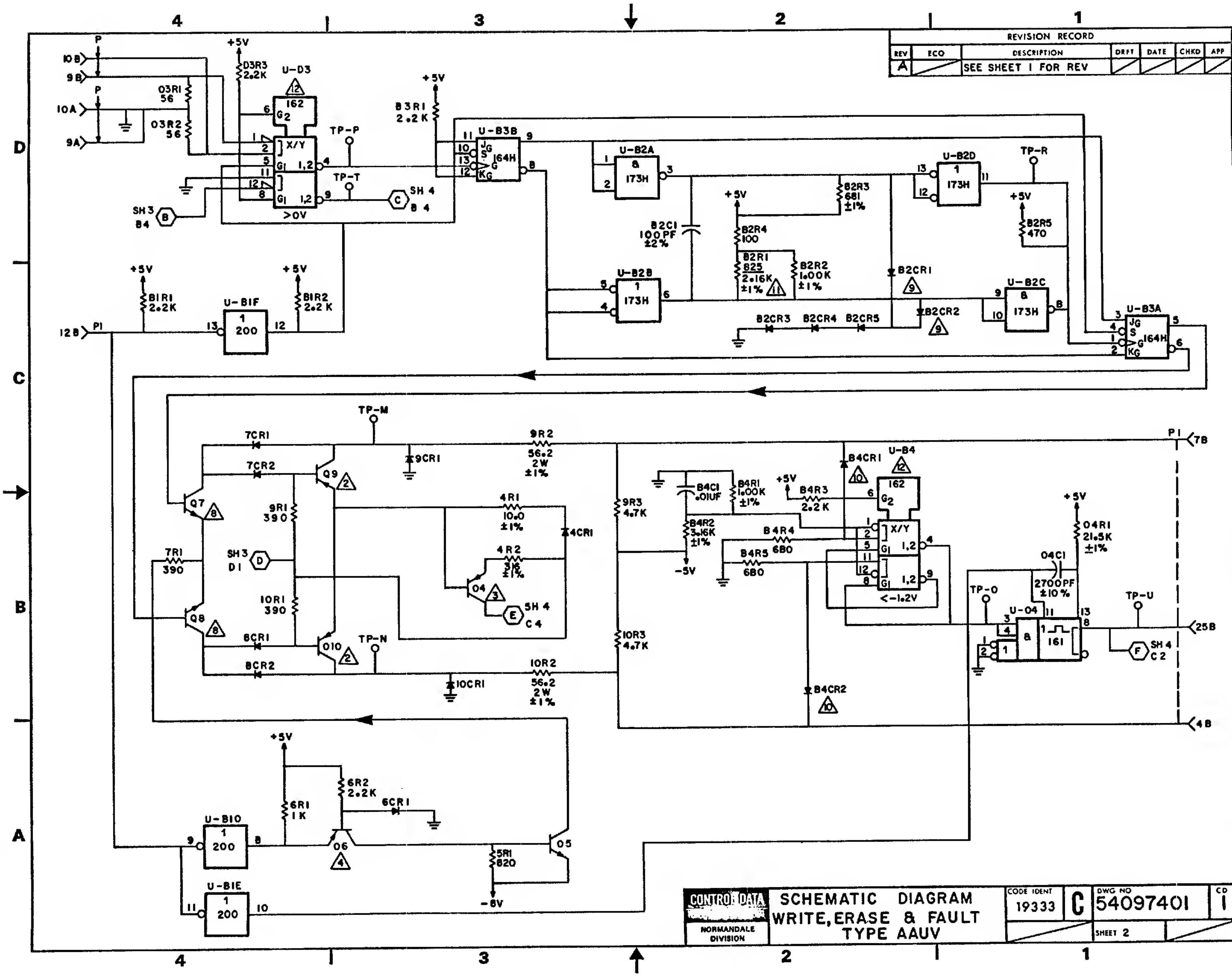
FIRST USED ON: BR301

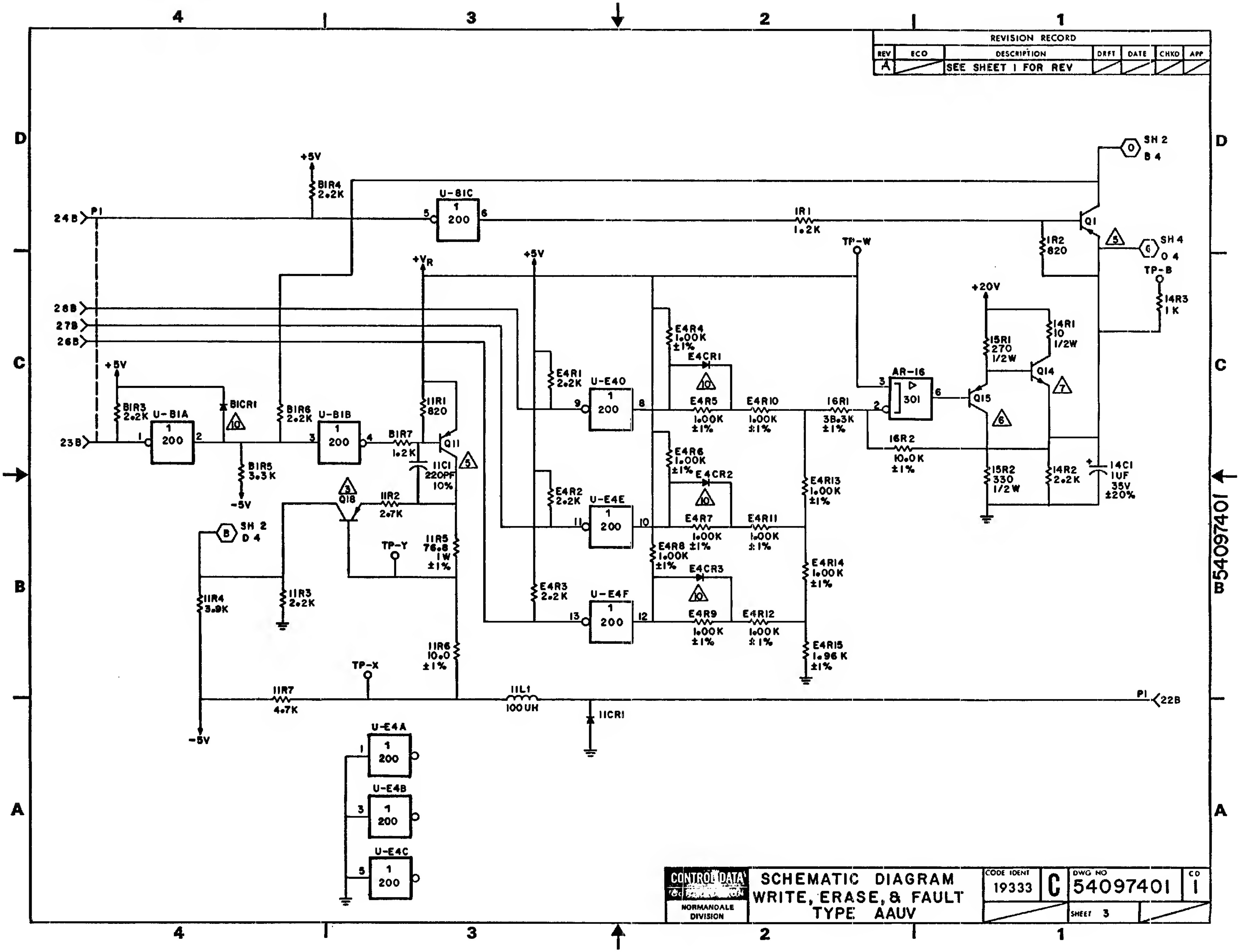
TITLE: SCHEMATIC DIAGRAM WRITE, ERASE & FAULT TYPE AAUV

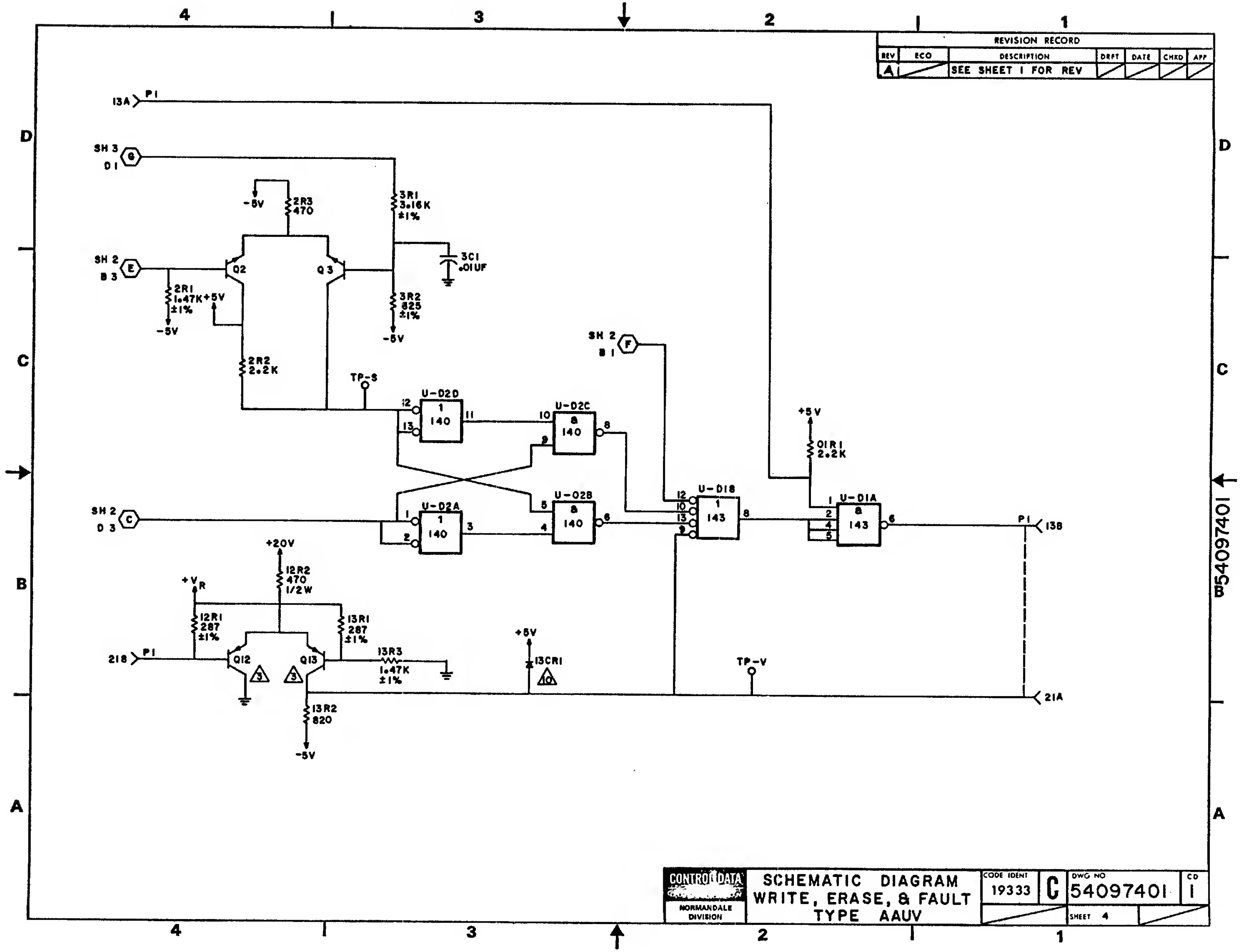
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54097401	1

SHEET 1 OF 4

54097401 B

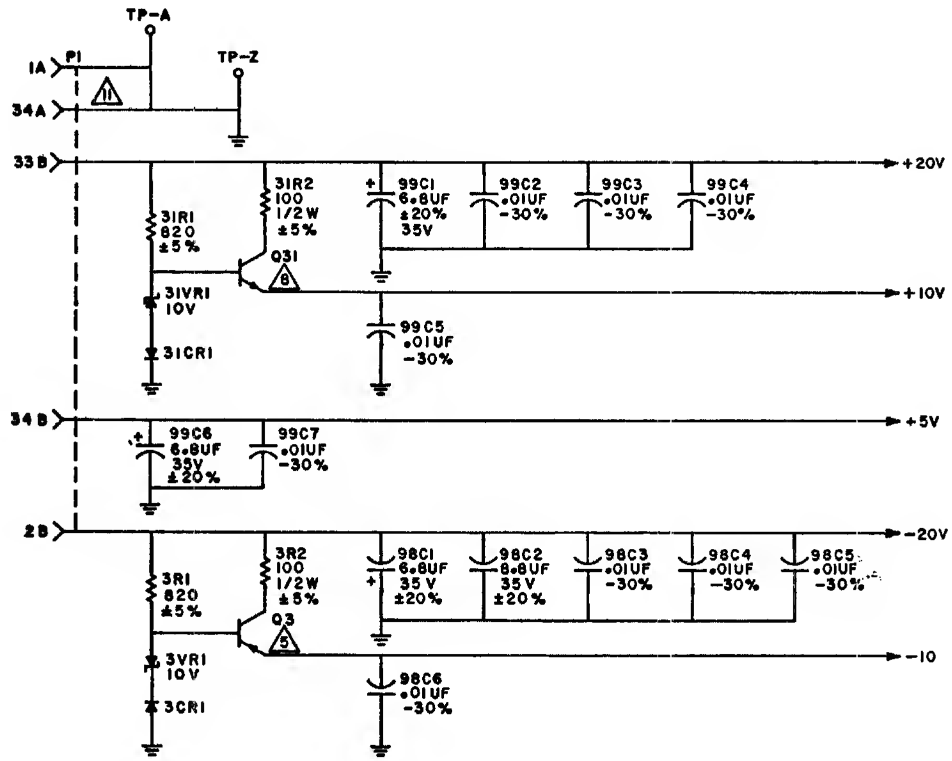

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
U-D3
162
X/Y
>0V
TP-P
TP-T
SH 4 B 4
SH 3 B4
D3R3 2.2K
D3R1 56
D3R2 56
B3R1 2.2 K
U-B3B
164H
U-B2A
173H
U-B2B
U-B2D
U-B2C
U-B3A
TP-R
B2R3 681 ±1%
B2R4 100
B2R1 825 2.16K ±1%
B2R2 1.00K ±1%
B2R5 470
B2C1 100 PF ±2%
B2CR1
B2CR2
B2CR3
B2CR4
B2CR5
B1R1 2.2K
B1R2 2.2 K
U-B1F
200
TP-M
7CR1
7CR2
9CR1
9R2 56.2 2W ±1%
Q9
Q7
9R1 390
4R1 10.0 ±1%
4CR1
4R2 316 ±1%
Q4
SH 4 C 4
7R1 390
SH3 D1
10R1 390
Q8
8CR1
8CR2
Q10
TP-N
10CR1
10R2 56.2 2W ±1%
9R3 4.7K
10R3 4.7K
B4C1 .01UF
B4R1 1.00K ±1%
B4R2 3.16K ±1%
B4R3 2.2 K
B4R4 680
B4R5 680
B4CR1
B4CR2
U-B4
<-1.2V
04R1 21.5K ±1%
04C1 2700PF ±10%
TP-O
TP-U
U-04
161
SH 4 C 2
P1
7B
25B
4B
12B
10B
9B
10A
9A
+5V
-5V
U-B10
U-B1E
6R1 1K
6R2 2.2K
6CR1
Q6
Q5
5R1 820
-6V
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
WRITE, ERASE & FAULT
TYPE AAUV
CODE IDENT 19333
C
DWG NO 54097401
SHEET 2
54097401


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
WRITE, ERASE, & FAULT
TYPE AAUV
CONTROL DATA
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54097401
CO 1
SHEET 3
54097401
U-B1A
U-B1B
U-B1C
U-E4A
U-E4B
U-E4C
U-E4D
U-E4E
U-E4F
AR-16
301
200
Q1
Q11
Q14
Q15
Q18
+5V
-5V
+20V
$+V_R$
TP-W
TP-B
TP-Y
TP-X
P1
24B
28B
27B
26B
23B
22B
SH 2 B 4
SH 4 D 4
SH 2 D 4
B1R4 2.2K
B1R3 2.2K
B1CR1
B1R5 3.3K
B1R6 2.2K
B1R7 1.2K
11R1 820
11C1 220PF 10%
11R2 2.7K
11R3 2.2K
11R4 3.9K
11R5 76.8 1W ±1%
11R6 10.0 ±1%
11R7 4.7K
11L1 100UH
11CR1
1R1 1.2K
1R2 820
E4R1 2.2K
E4R2 2.2K
E4R3 2.2K
E4R4 1.00K ±1%
E4CR1
E4R5 1.00K ±1%
E4R6 1.00K ±1%
E4CR2
E4R7 1.00K ±1%
E4R8 1.00K ±1%
E4CR3
E4R9 1.00K ±1%
E4R10 1.00K ±1%
E4R11 1.00K ±1%
E4R12 1.00K ±1%
E4R13 1.00K ±1%
E4R14 1.00K ±1%
E4R15 1.96 K ±1%
16R1 38.3K ±1%
16R2 10.0K ±1%
15R1 270 1/2W
15R2 330 1/2 W
14R1 10 1/2W
14R2 2.2K
14R3 1 K
14C1 1UF 35V ±20%


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
13A P1
SH 3 G D1
-5V
2R3 470
3R1 3.16K ±1%
3C1 .01UF
SH 2 E B3
Q2
Q3
2R1 1.47K ±1%
+5V
-5V
3R2 825 ±1%
2R2 2.2K
TP-S
U-D2D 1 140
U-D2C 8 140
SH 2 F B1
+5V
01R1 2.2K
U-D1B 1 143
U-D1A 8 143
SH 2 C D3
U-D2A 1 140
U-D2B 8 140
P1 13B
+20V
12R2 470 1/2W
+VR
12R1 287 ±1%
13R1 287 ±1%
21B P1
Q12
Q13
13R3 1.47K ±1%
+5V
13CR1
TP-V
21A
13R2 820
-5V
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
WRITE, ERASE, & FAULT
TYPE AAUV
CODE IDENT 19333
C
DWG NO 54097401
CD 1
SHEET 4
54097401

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED			7/30/71	



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL ZENER VOLTAGE TOLERANCES ±5%.
   ALL TRANSISTORS, SNPN, 2N3646, 50210310.
   ALL DIODES, SILICON, 92115023.
2. TSTR, CA3018, 50251100.
3. TSTR, SNPN, 2N2221, 50210102.
4. TSTR, SPNP, 2N4258, 50211510.
5. TSTR, SPNP, 2N3645, 50211210.
6. TSTR, SPNP, 2N4916, 50211610.
7. TSTR, SPNP, 2N4916, MATCHED PAIR, 50211612.
8. TSTR, SNPN, 2N3569, 50210811.
9. DIODE, SILICON, 92115021.
10. DIODE, HOT CARRIER, 50241400.
11. PINS 1A THRU 34A ARE CONNECTED TO GND.

REFERENCE DRAWINGS	
COMP ASSY: 54097700	

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: BR301

DWN	Moche	5-4-71
CHK	Hanson	7-21-71
ENGR	Uruna	7-23-71
MFG		7/23/71
APPR		7-23-71

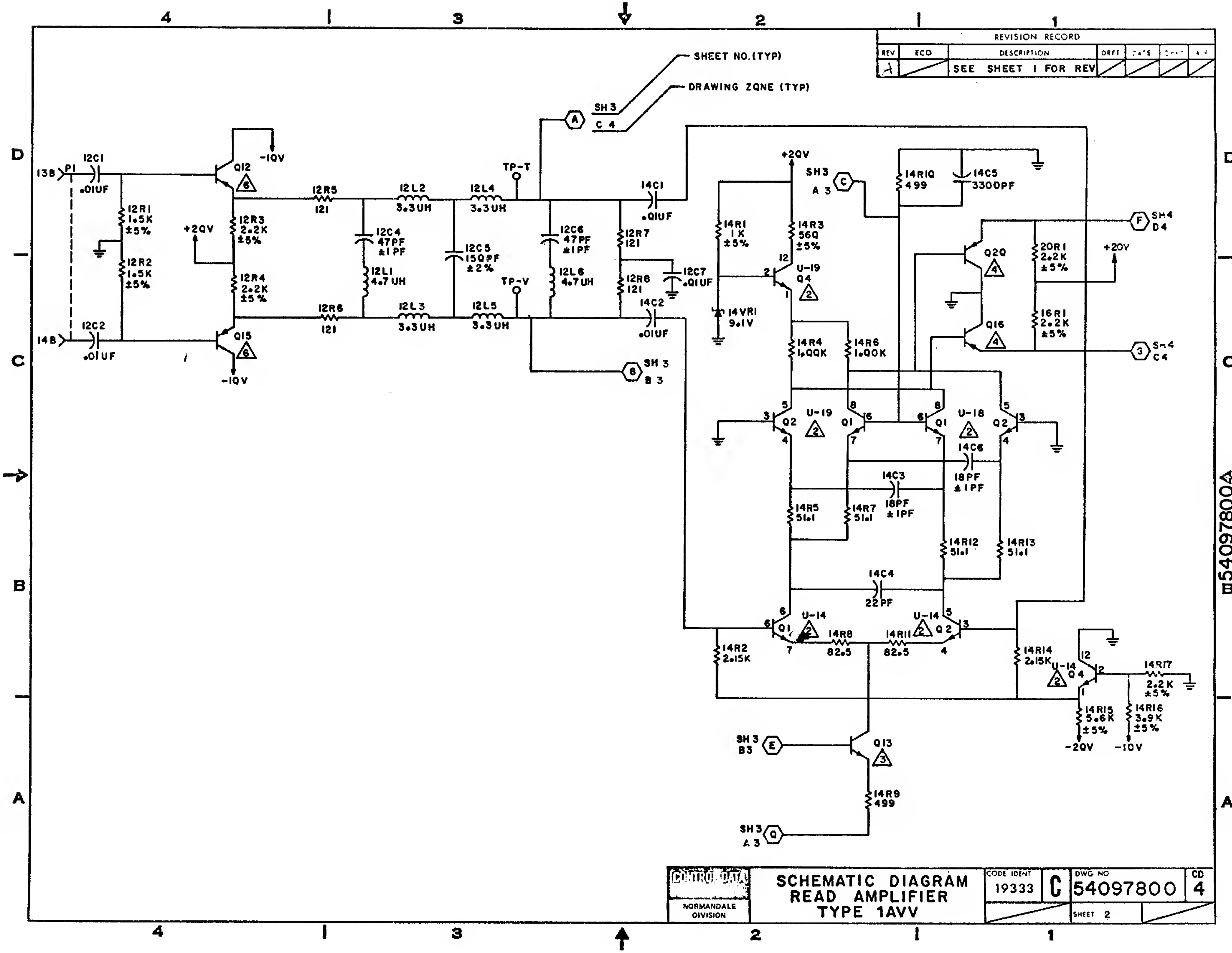
TITLE: SCHEMATIC DIAGRAM READ AMPLIFIER TYPE 1AVV

CODE IDENT 19333 — C — DRAWING NUMBER 54097800 — CD 4

SHEET 1 OF 4

4PD

54097800



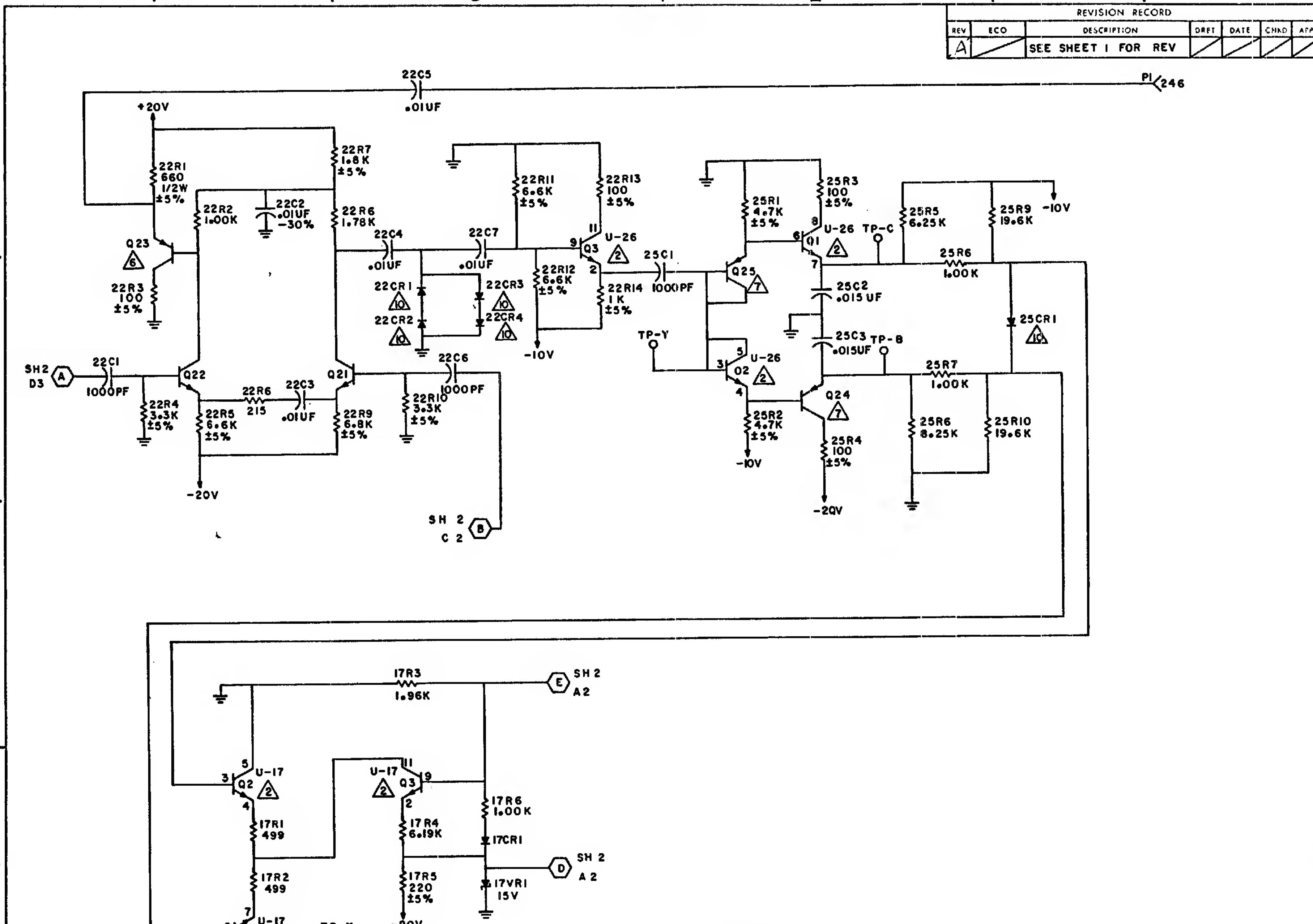
CONTROL DATA

NORMANDALE DIVISION

SCHEMATIC DIAGRAM
READ AMPLIFIER
TYPE 1AVV

CODE IDENT		DWG NO	CD
19333	C	54097800	4
		SHEET 2	

B54097800A



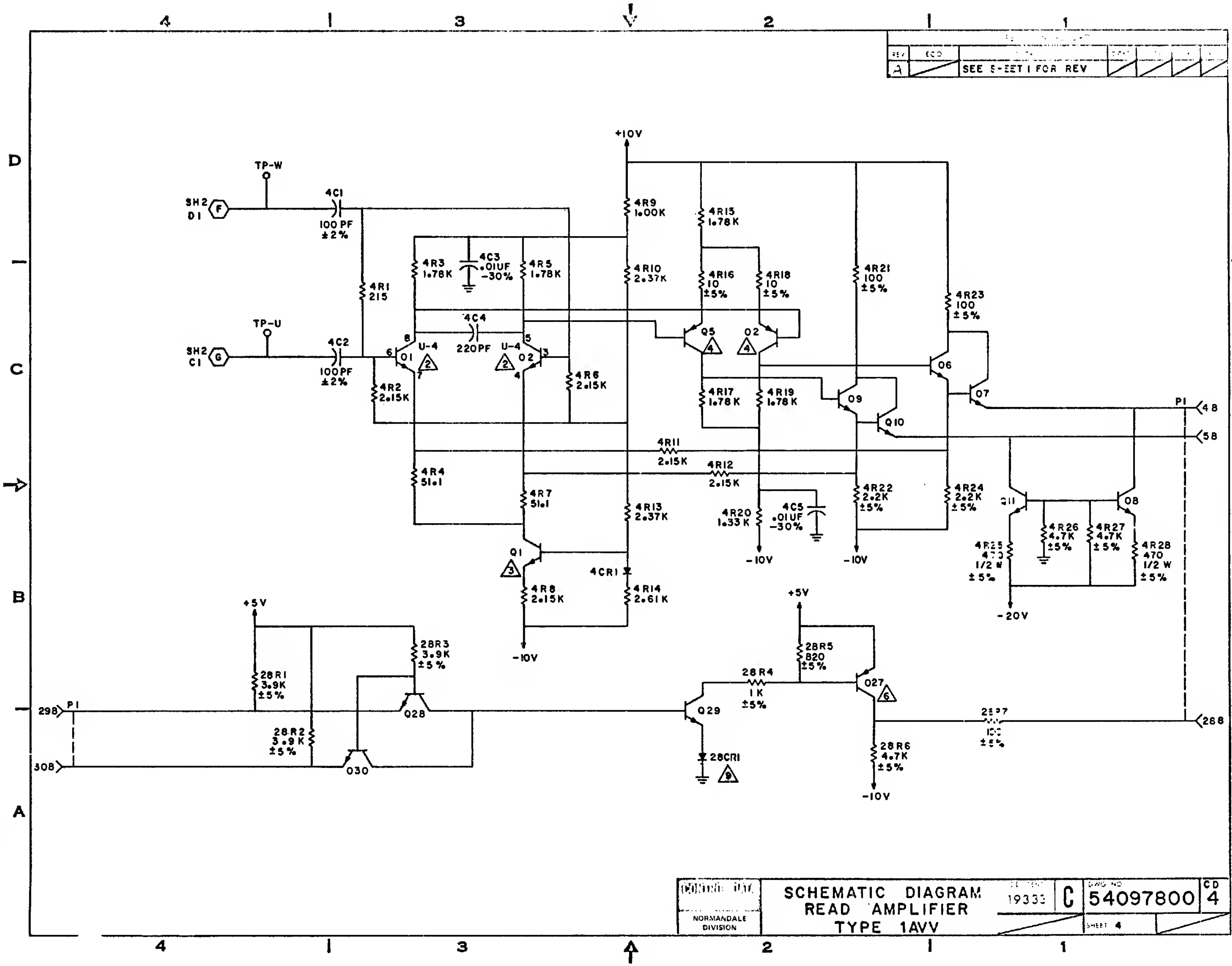
CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
READ AMPLIFIER
TYPE 1AVV

CODE IDENT	SIZE	DWG NO	
19333	C	54097800	4

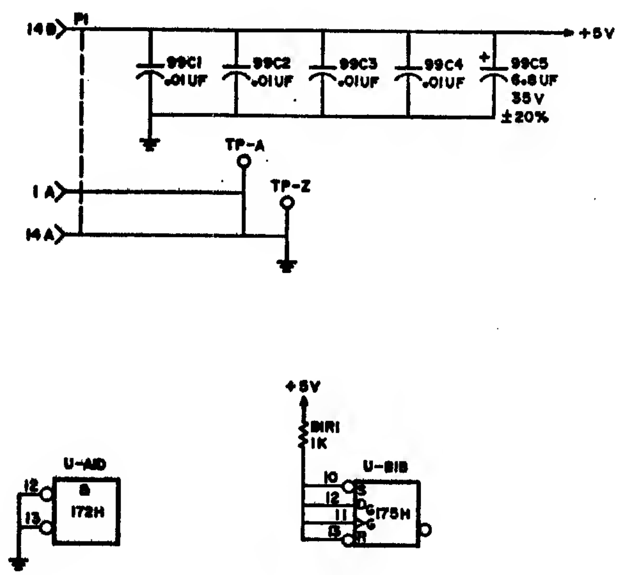
SHEET 3

B54097800 A


SEE SHEET I FOR REV
+10V
TP-W
SH2 D1
4C1 100 PF ±2%
4R1 215
4R3 1.78K
4C3 .01UF -30%
4R5 1.78K
4R9 1.00K
4R10 2.37K
4R15 1.78K
4R16 10 ±5%
4R18 10 ±5%
4R21 100 ±5%
4R23 100 ±5%
TP-U
SH2 C1
4C2 100PF ±2%
4C4 220PF
U-4
Q1
Q2
4R2 2.15K
4R6 2.15K
Q5
Q2
Q6
Q7
Q9
Q10
4R17 1.78K
4R19 1.78K
P1 48
58
4R11 2.15K
4R12 2.15K
4R4 51.1
4R7 51.1
4R13 2.37K
4R20 1.33K
4C5 .01UF -30%
4R22 2.2K ±5%
4R24 2.2K ±5%
Q11
Q8
4R26 4.7K ±5%
4R27 4.7K ±5%
4R25 470 1/2 W ±5%
4R28 470 1/2 W ±5%
-10V
-20V
Q1
4CR1
4R8 2.15K
4R14 2.61K
+5V
28R3 3.9K ±5%
28R1 3.9K ±5%
28R2 3.9K ±5%
298 P1
308
Q28
Q30
+5V
28R5 820 ±5%
28R4 1K ±5%
Q27
Q29
28CR1
28R6 4.7K ±5%
28R7 100 ±5%
288
SCHEMATIC DIAGRAM
READ AMPLIFIER
TYPE 1AVV
NORMANDALE DIVISION
19333
C
54097800
4
SHEET 4

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED		0-3-72		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
3. DELAY FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASSY 54100500

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A8B	
DWN	O. G. TUTTLE	9-5-72
CHK		9-17-72
ENGR		9/19/72
MFG		9-26-72
APPR		

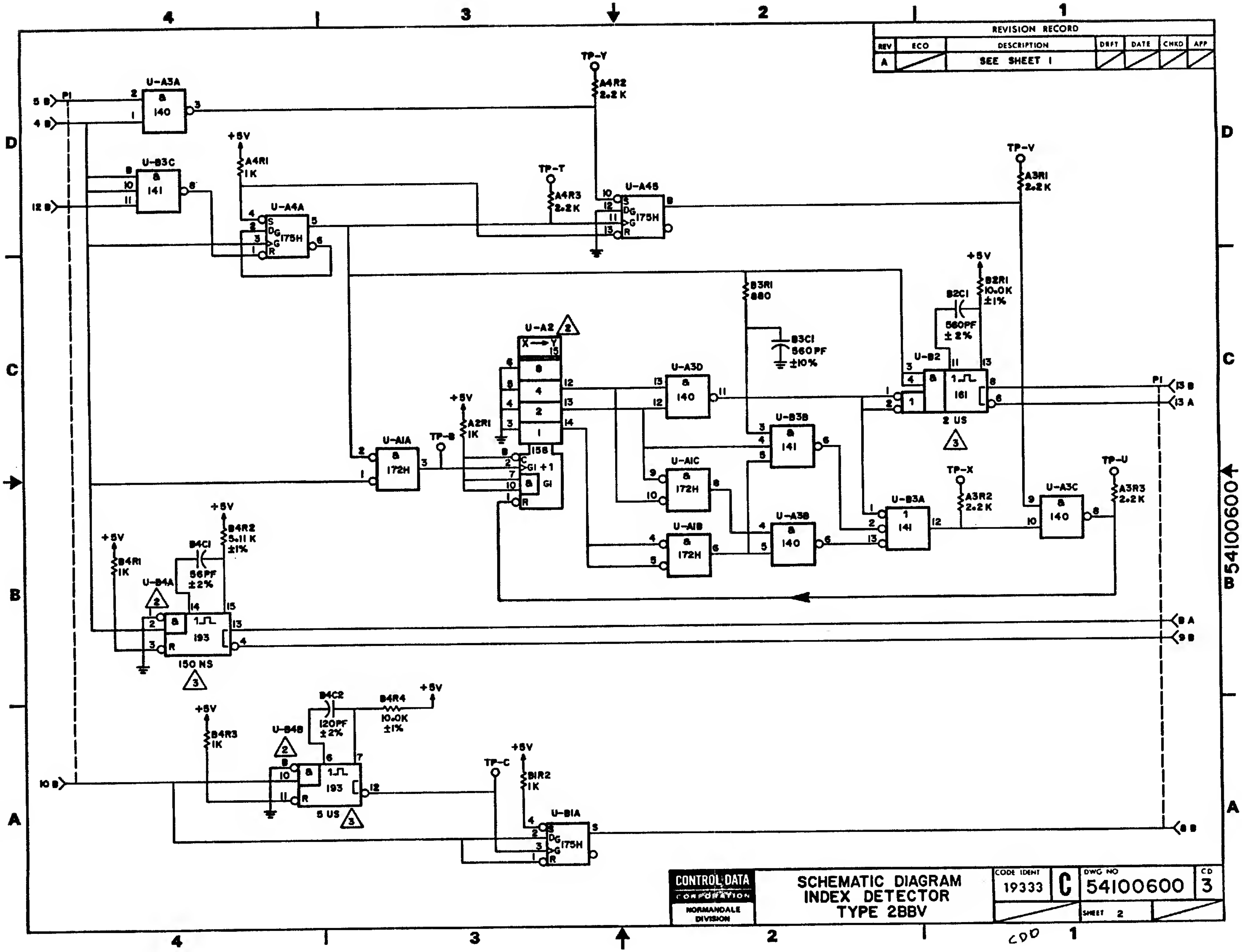
TITLE

SCHEMATIC DIAGRAM INDEX DETECTOR TYPE 2BBV

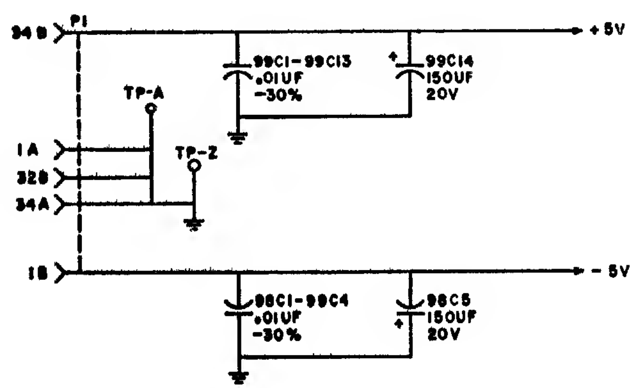
CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54100600	3

SHEET 1 OF 2

54100600


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1
U-A3A
U-B3C
U-A4A
U-A4B
U-A2
U-A3D
U-B2
U-A1A
U-B3B
U-A1C
U-A1B
U-A3B
U-B3A
U-A3C
U-B4A
U-B4B
U-B1A
2 US
150 NS
5 US
CONTROL DATA CORPORATION
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
INDEX DETECTOR
TYPE 2BBV
CODE IDENT 19333
C
DWG NO 54100600
CD 3
SHEET 2
54100600

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   ALL DIODES, SCHOTTKY BARRIER, 50241400.
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
2. TRANSISTOR, SNPN, 2N3646, 50210310.
3. DIODE, SILICON, 92115021.
4. DIODE, SILICON, 92115023.
5. DIODE, GERMANIUM, 11801200.
6. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
7. DELAY TIME TO BE SELECTED IN PRODUCTION PER RECOMMENDED TEST PROCEDURE.

B54105401

REFERENCE DRAWINGS	
COMP ASSY : 54105301	

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA — NORMANDALE DIVISION

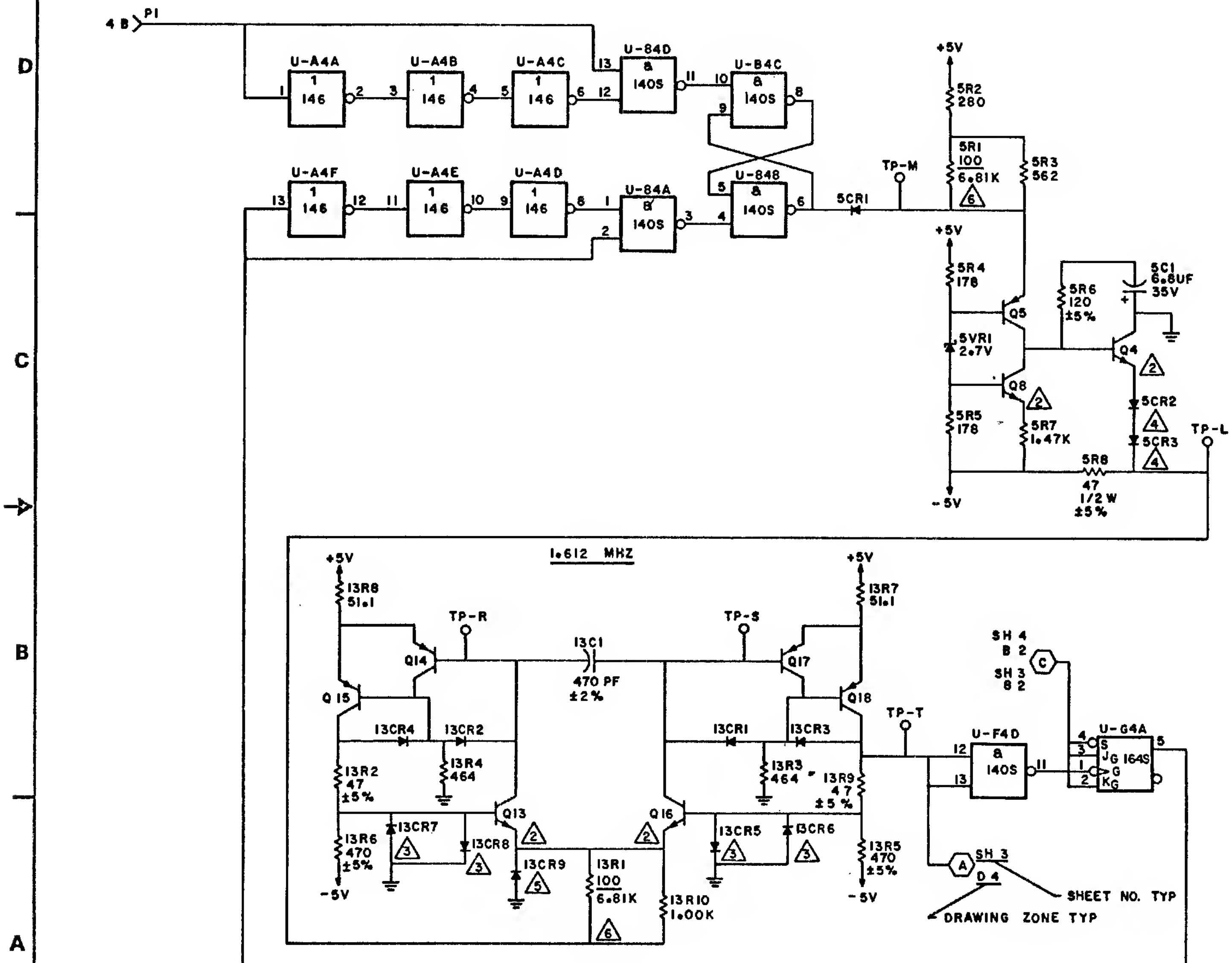
FIRST USED ON	BR3A3	
DWN	RKR	11-27-72
CHK		
ENGR		
MFG		
APPR		

TITLE: SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV

CODE IDENT 19333 | C | DRAWING NUMBER 54105401 | CD 1

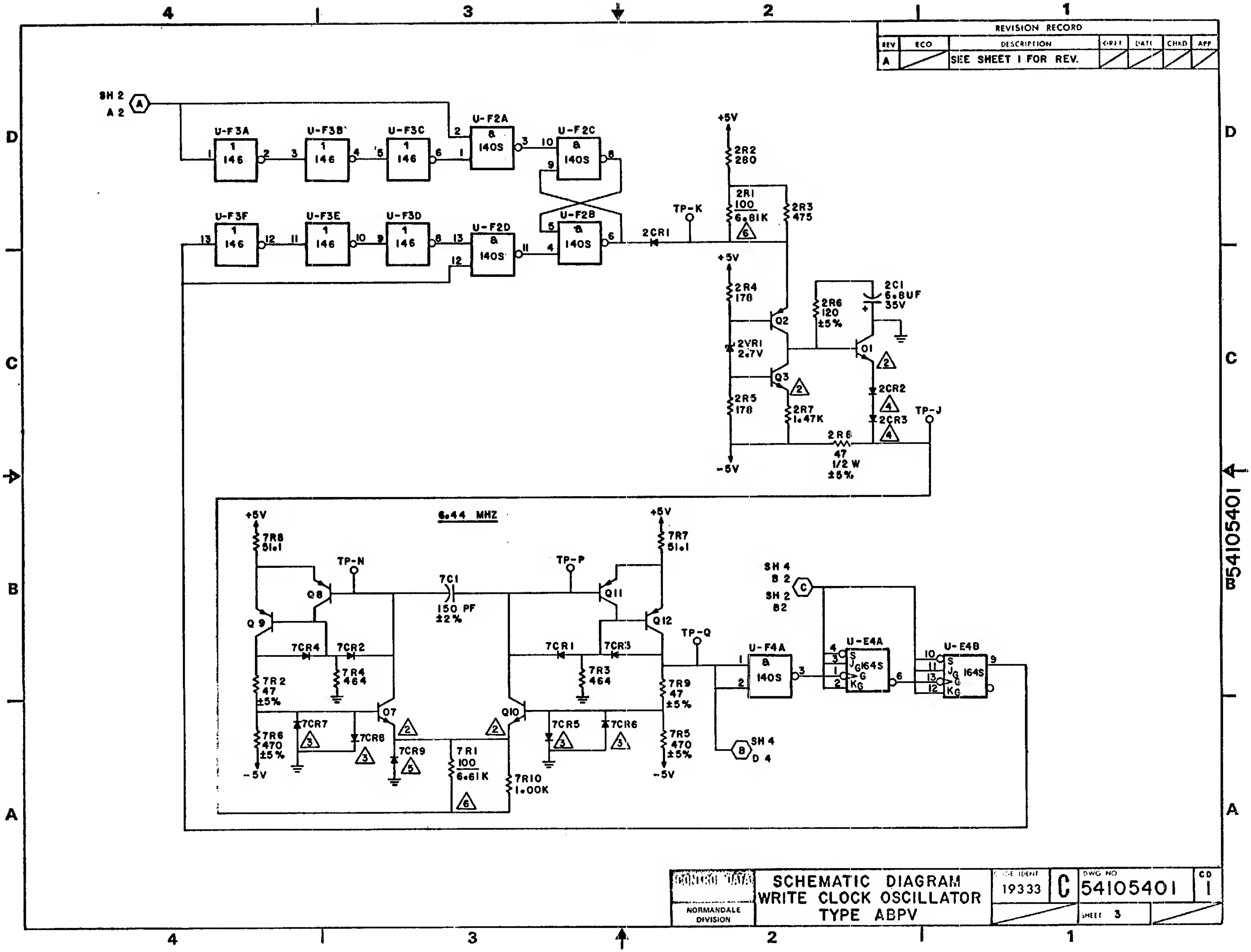
SHEET 1 OF 4

REVISION RECORD						
REV	ECO	DESCRIPTION	CRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV.				



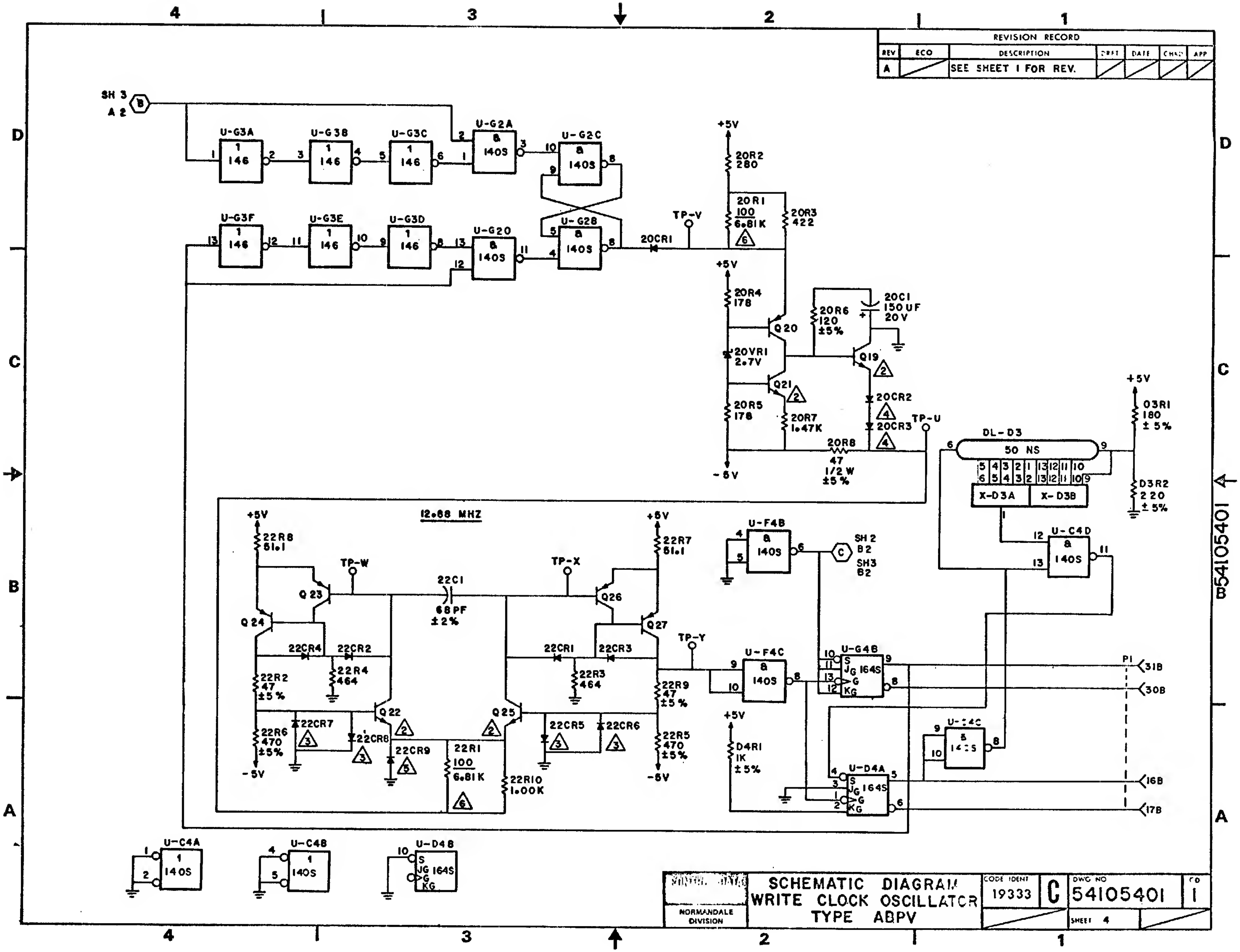
CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV	CODE IDENT 19333	C	DWG NO 54105401	CD 1
				SHEET 2	

54105401



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV	CODE IDENT 19333	C	DWG NO 54105401	CD 1
				SHEET 3	

54105401



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV.				

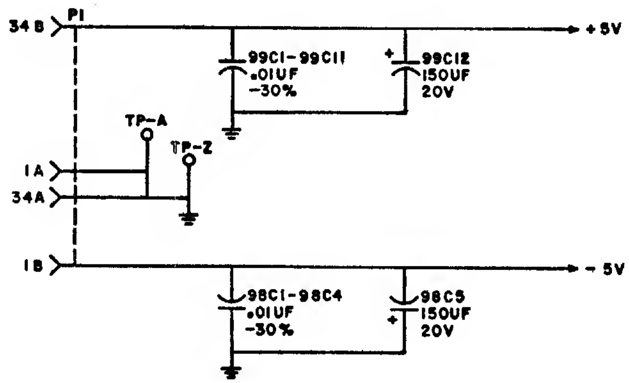
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
WRITE CLOCK OSCILLATOR
TYPE ABPV

CODE IDENT 19333 C DWG NO 54105401 SHEET 4

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED		3-7-72		RIR



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   ALL DIODES, SCHOTTKY BARRIER, 50241400.
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.

2. TRANSISTOR, SNPN, 2N3646, 50210310.
3. DIODE, SILICON, 92115021.
4. DIODE, SILICON, 92115023.
5. DIODE, GERMANIUM, 11801200.
6. COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.

54105400

REFERENCE DRAWINGS			
COMP ASSY : 54105300			
COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: BR3A3

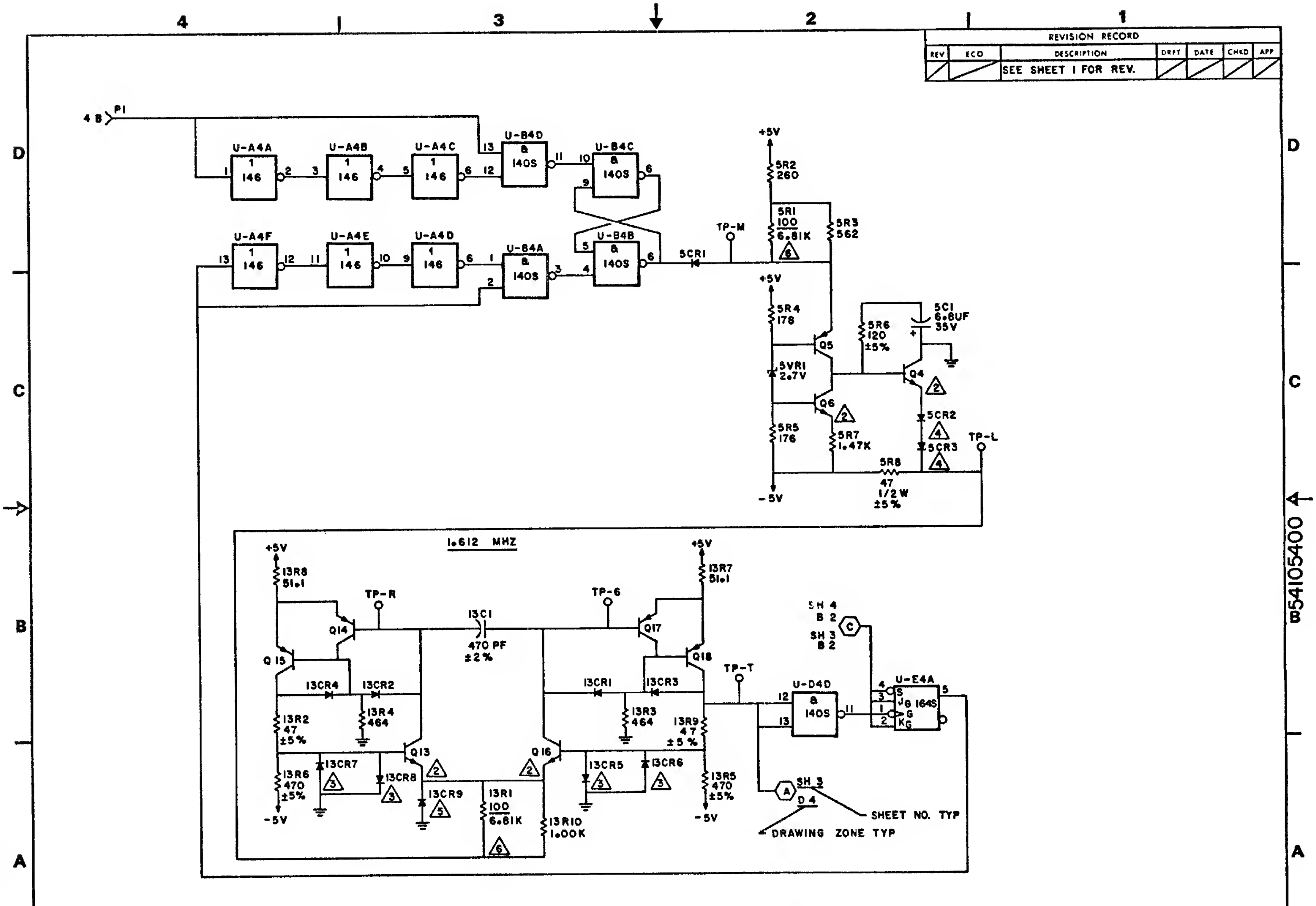
DWN / CHK / ENGR / MFG / APPR

TITLE: SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE 2BPV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54105400	3

SHEET 1 OF 4

HPD



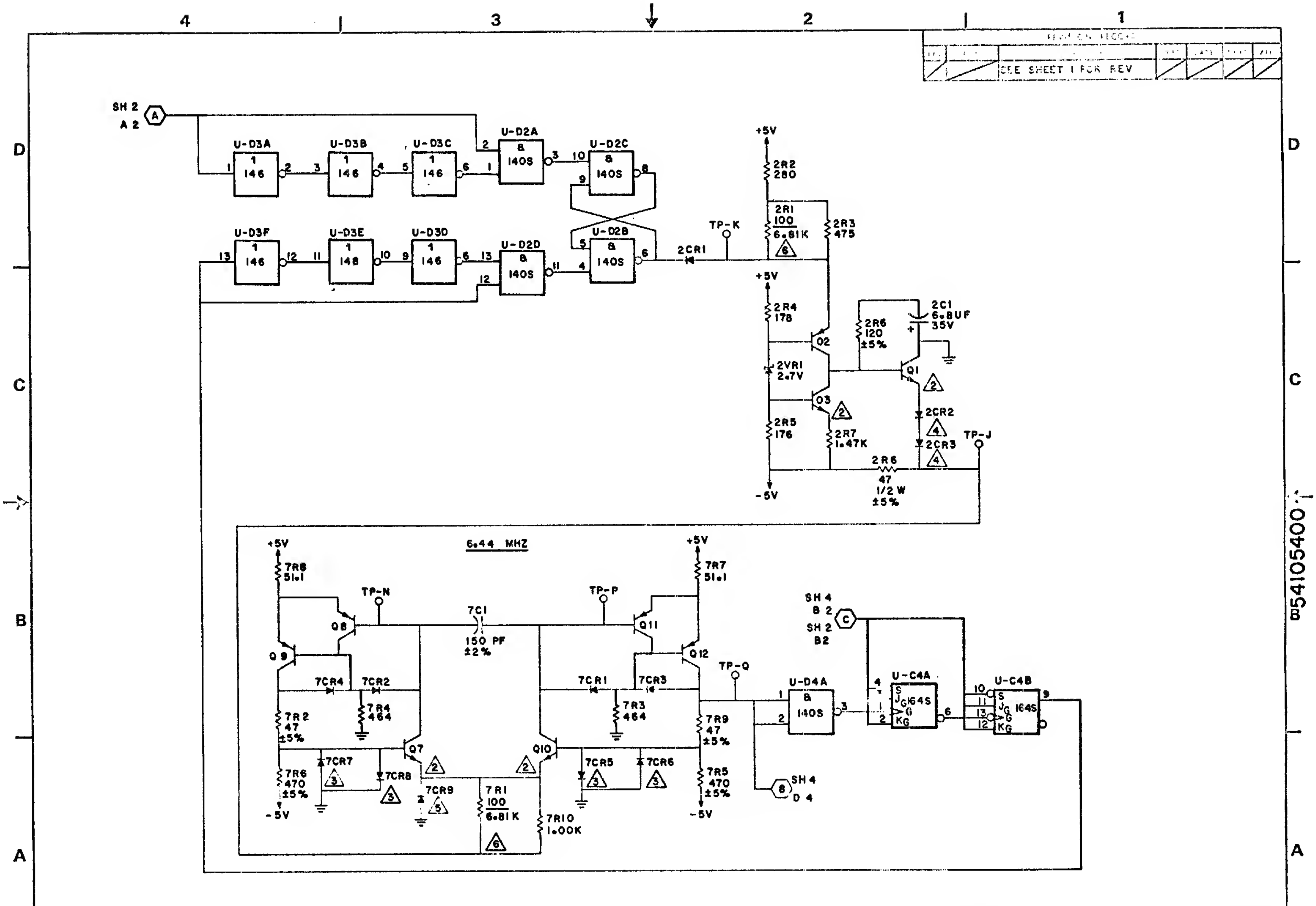
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
WRITE CLOCK OSCILLATOR
TYPE 2BPV

CODE IDENT	SIZE	DWG NO	CD
19333	C	54105400	3
		SHEET 2	

54105400

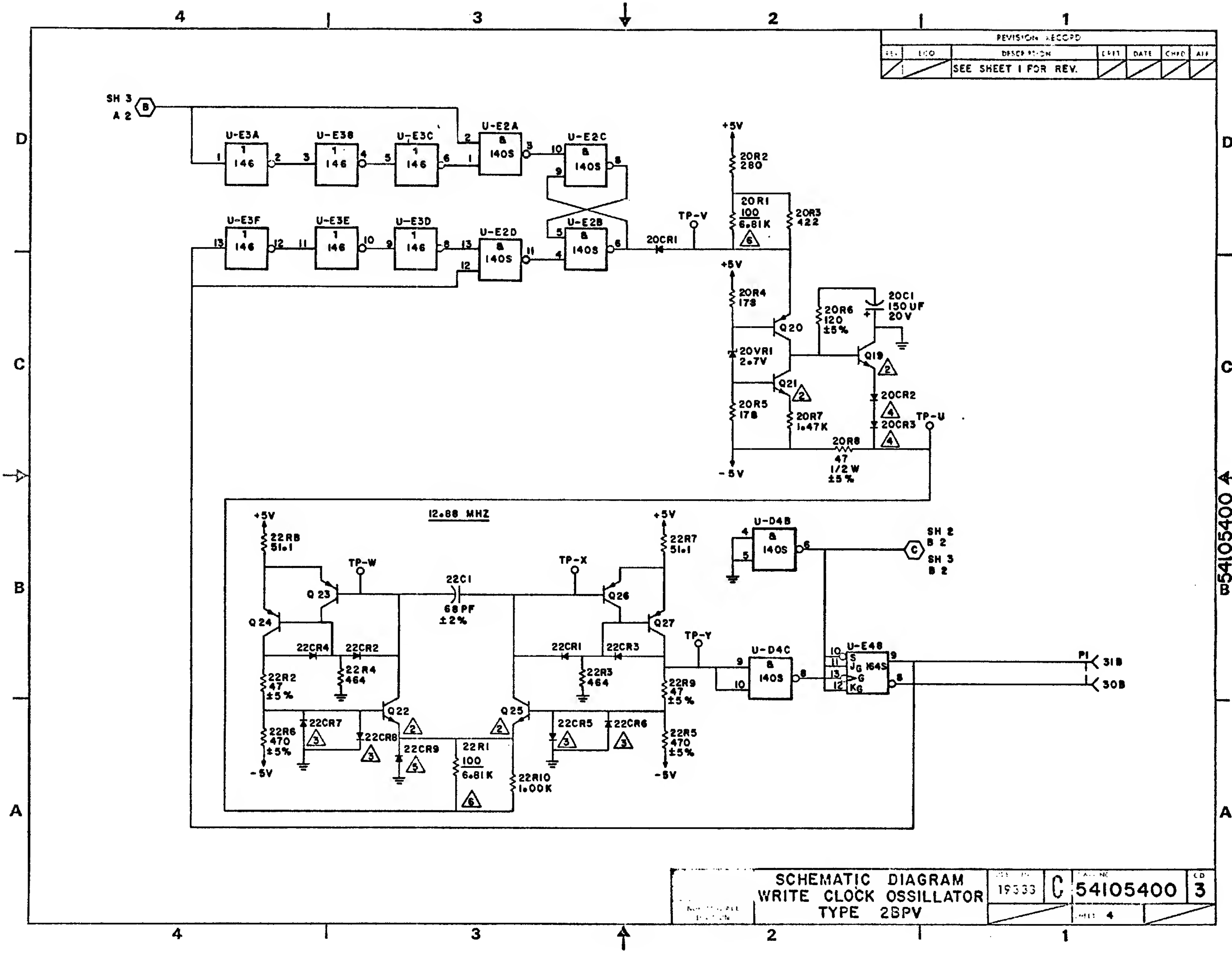
70629100 E



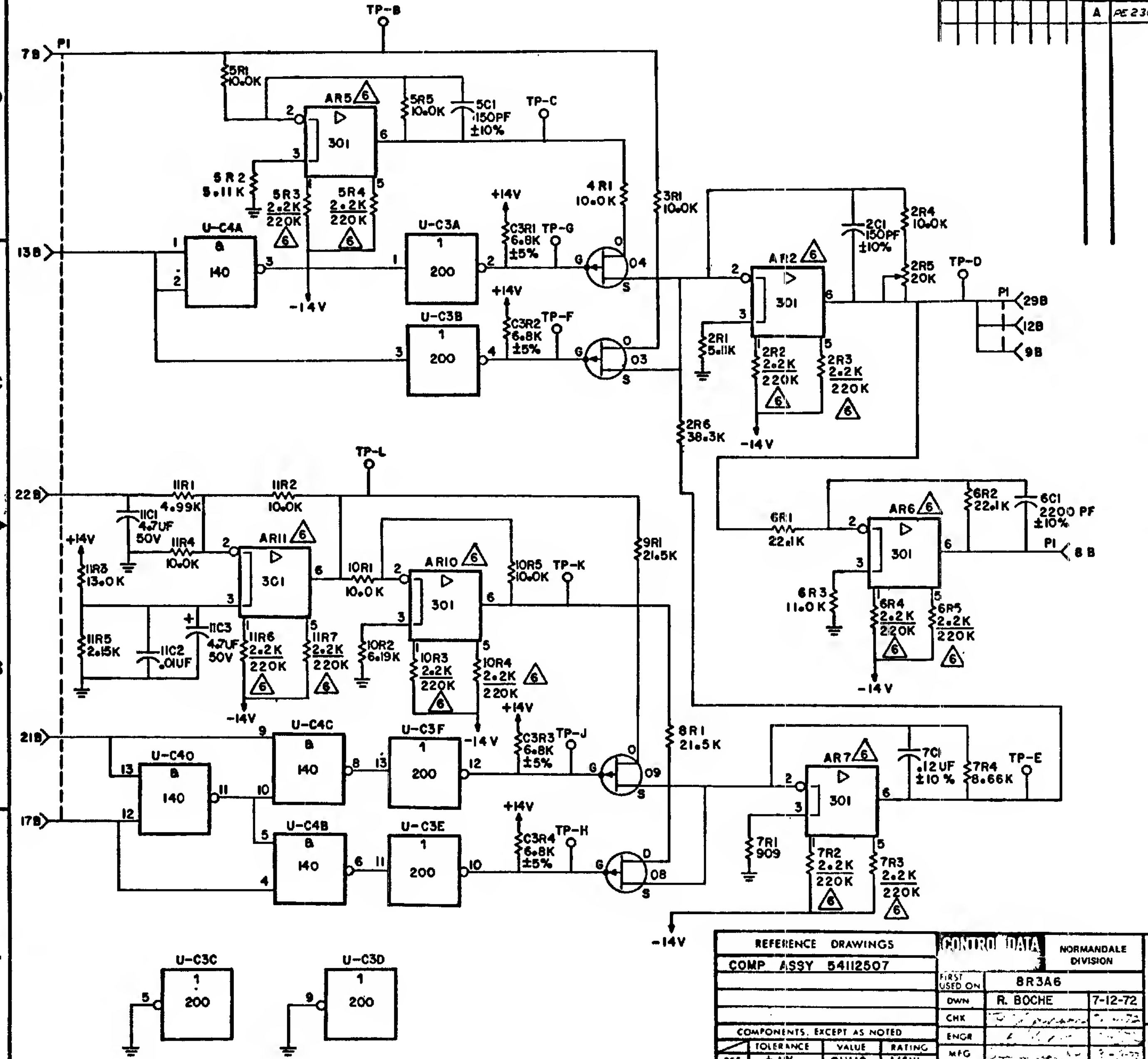
SCHEMATIC DIAGRAM
WRITE CLOCK OSCILLATOR
TYPE 2DPV

54105400 | 3

54105400


REVISION RECORD
SEE SHEET 1 FOR REV.
SH 3
A 2
U-E3A
U-E3B
U-E3C
U-E2A
U-E2C
U-E3F
U-E3E
U-E3D
U-E2D
U-E2B
146
140S
+5V
20R2
280
20R1
100
6.81K
20R3
422
TP-V
20CR1
20R4
178
Q20
20VR1
2.7V
Q21
20R5
178
20R7
1.47K
20R6
120
±5%
20C1
150 UF
20V
Q19
20CR2
20CR3
TP-U
20R8
47
1/2 W
±5%
-5V
12.88 MHZ
22R8
51.1
TP-W
Q 23
Q 24
22C1
68 PF
±2%
TP-X
Q26
22R7
51.1
Q27
22CR4
22CR2
22R4
464
22R2
47
±5%
22CR1
22CR3
22R3
464
22R9
47
±5%
Q22
Q25
22R6
470
±5%
22CR7
22CR8
22CR9
22R1
100
6.81K
22R10
1.00K
22CR5
22CR6
22R5
470
±5%
TP-Y
U-D4B
U-D4C
U-E4B
164S
SH 2
B 2
SH 3
B 2
P1
31B
30B
SCHEMATIC DIAGRAM
WRITE CLOCK OSSILLATOR
TYPE 2BPV
19333
C
54105400
3
4
54105400

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, FET'S 50218200
   ALL DIODES, GERMANIUM, 11801200
2. SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
5. IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
6. MATCHED COMPONENTS. SEE 70740800.

REFERENCE DRAWINGS
COMP ASSY 54112607

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	8R3A6	
DWN	R. BOCHE	7-12-72
CHK		
ENGR		
MFG		
APPD		

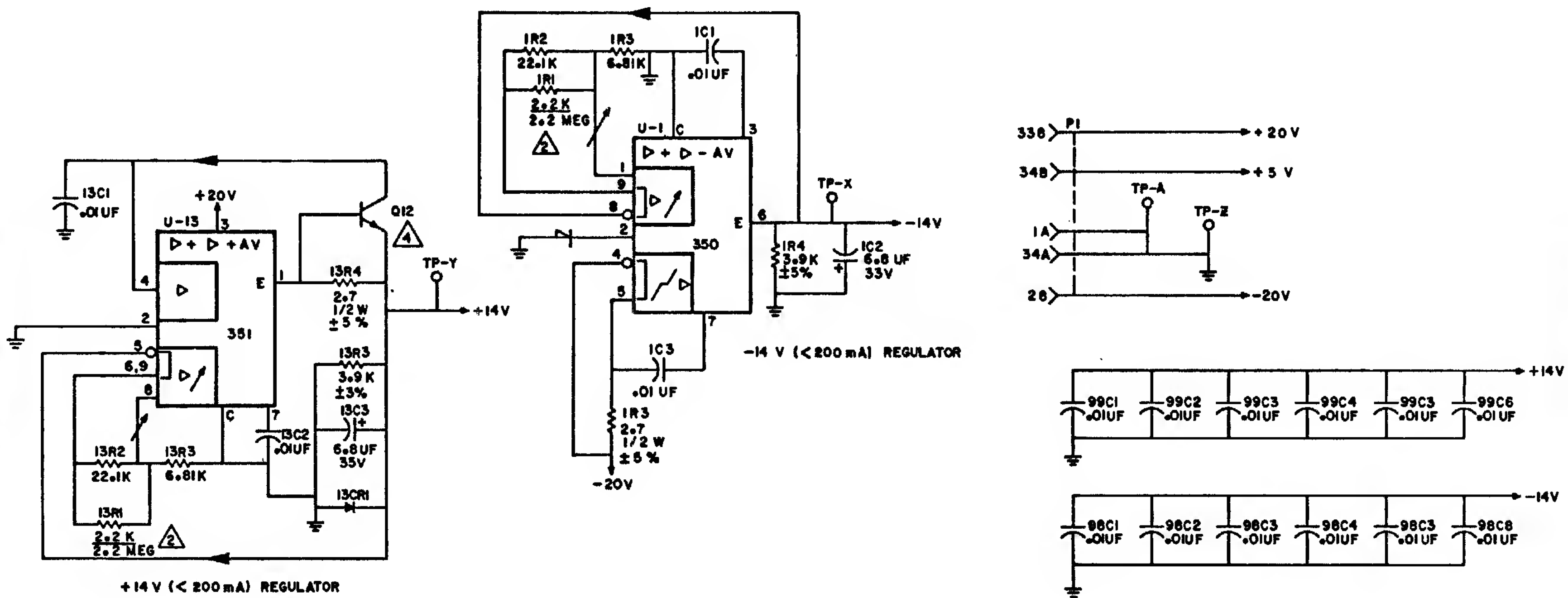
TITLE: SCHEMATIC DIAGRAM VOLTAGE GENERATOR, TRACK SERVO TYPE ECGV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54112607	4

SHEET 1 OF 2

54112607

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
VOLTAGE GENERATOR,
TRACK SERVO
TYPE ECGV

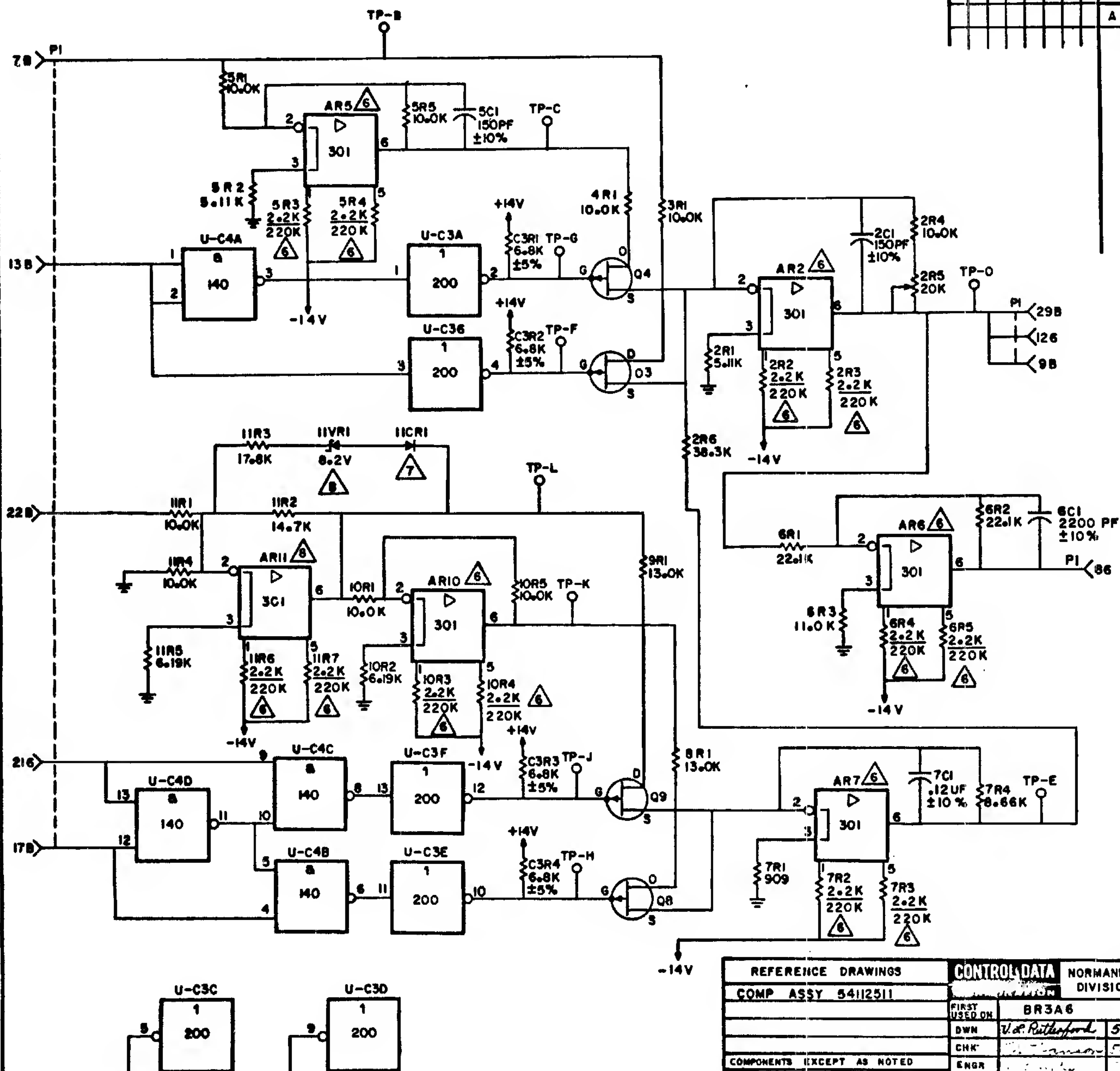
CODE IDENT 19333 | C | DWG NO 54112607 | CD 4
SHEET 2

54112607

SHEET	REVISION	STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		5-1-73		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, FET'S 50216200
   ALL DIODES, GERMANIUM, 116D1200

2. SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.

3. TRANSISTOR, SNPN, 2N3646, 50210310.

4. IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

5. IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.

6. MATCHED COMPONENTS. SEE 70740600.

7. DIODE, SILICON, 24553500

8. DIODE, ZENER, 50240111, ±5% TOLERANCE.

REFERENCE DRAWINGS
COMP ASSY 54112511

COMPONENTS EXCEPT AS NOTED			
RES	±1%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A6
DWN	V.L. Rutherford 5-8-73
CHK	5-9-73
ENGR	
MFG	
APPR	

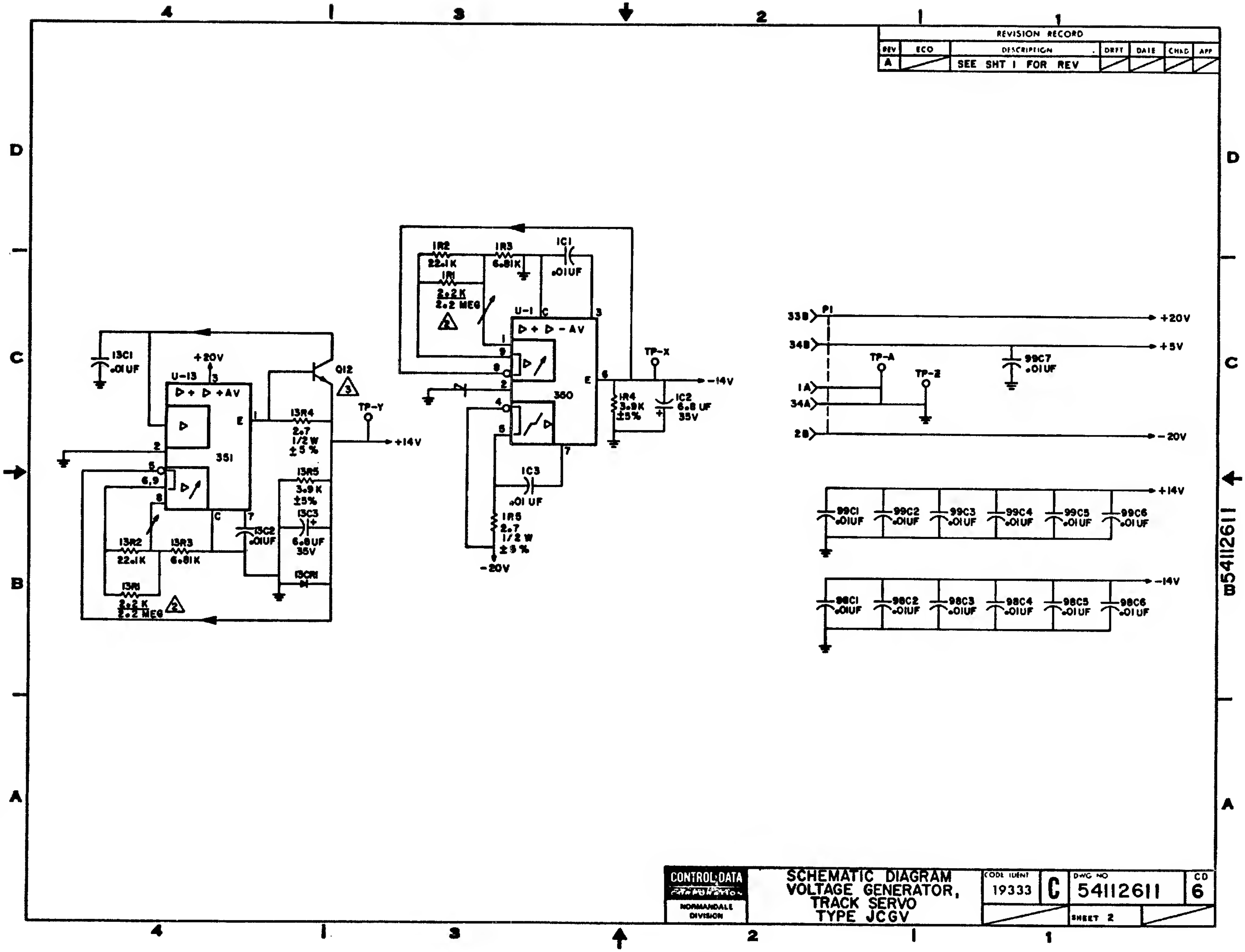
TITLE: SCHEMATIC DIAGRAM VOLTAGE GENERATOR, TRACK SERVO TYPE JCGV

CODE IDENT	SIZE	DRAWING NUMBER	CO
19333	C	54112611	6

SHEET 1 OF 2

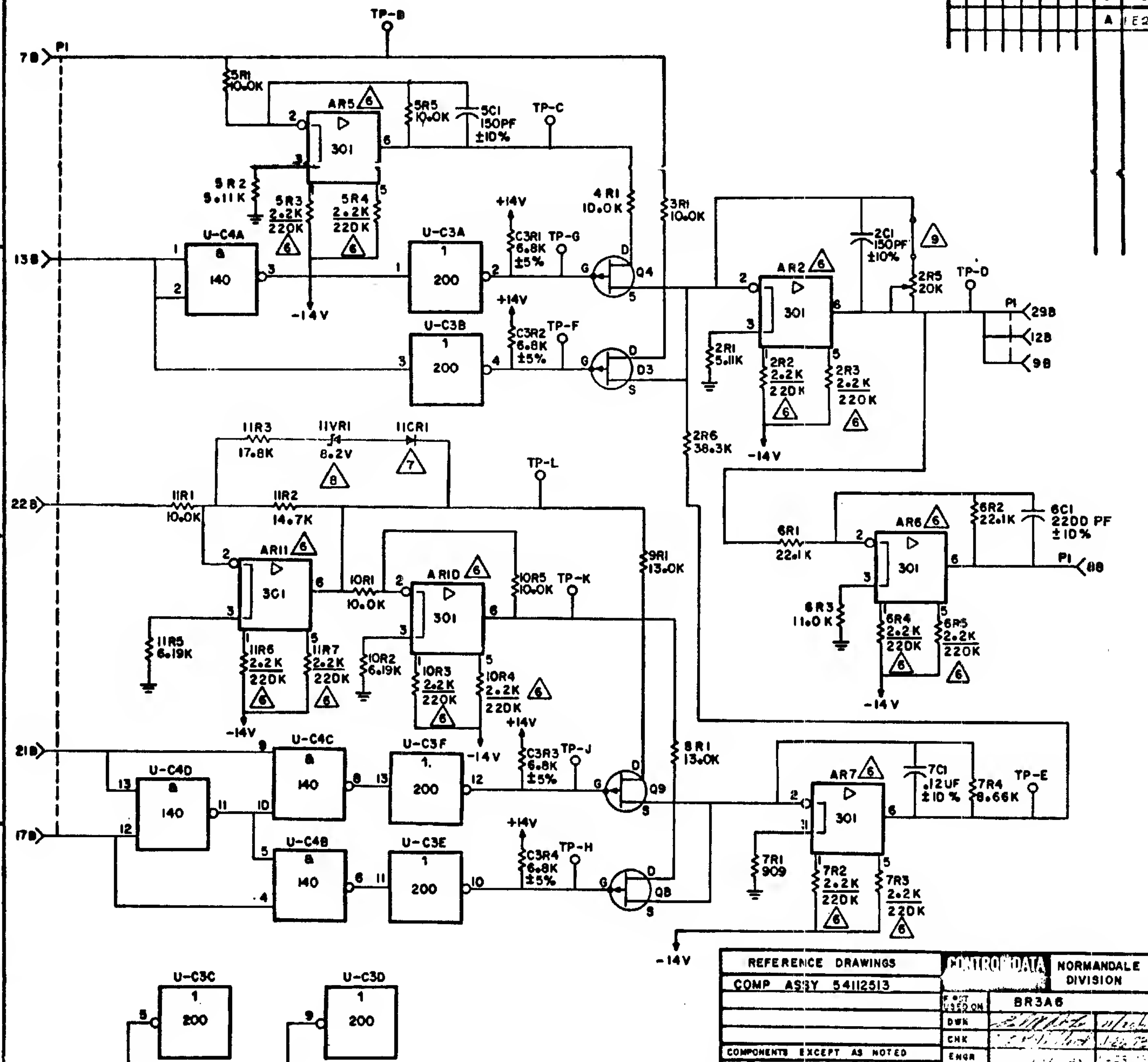
HPD

54112611


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHT 1 FOR REV
U-13
+20V
Q12
13C1 .01UF
351
13R4 2.7 1/2 W ±5%
13R5 3.9K ±5%
13C3 6.8UF 35V
13CR1
13C2 .01UF
13R2 22.1K
13R3 6.81K
13R1 2.2K 2.2 MEG
TP-Y
+14V
1R2 22.1K
1R3 6.81K
1C1 .01UF
1R1 2.2K 2.2 MEG
U-1
360
TP-X
-14V
1R4 3.9K ±5%
1C2 6.8 UF 35V
1C3 .01 UF
1R5 2.7 1/2 W ±5%
-20V
33B P1 +20V
34B +5V
TP-A
TP-Z
99C7 .01UF
1A
34A
2B -20V
+14V
99C1 .01UF 99C2 .01UF 99C3 .01UF 99C4 .01UF 99C5 .01UF 99C6 .01UF
-14V
98C1 .01UF 98C2 .01UF 98C3 .01UF 98C4 .01UF 98C5 .01UF 98C6 .01UF
54112611
CONTROL DATA CORPORATION
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
VOLTAGE GENERATOR, TRACK SERVO TYPE JCGV
CODE IDENT 19333
C
DWG NO 54112611
CD 6
SHEET 2

70629100 F

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	1E23666	RELEASED		12-7-73		CK



NOTE:

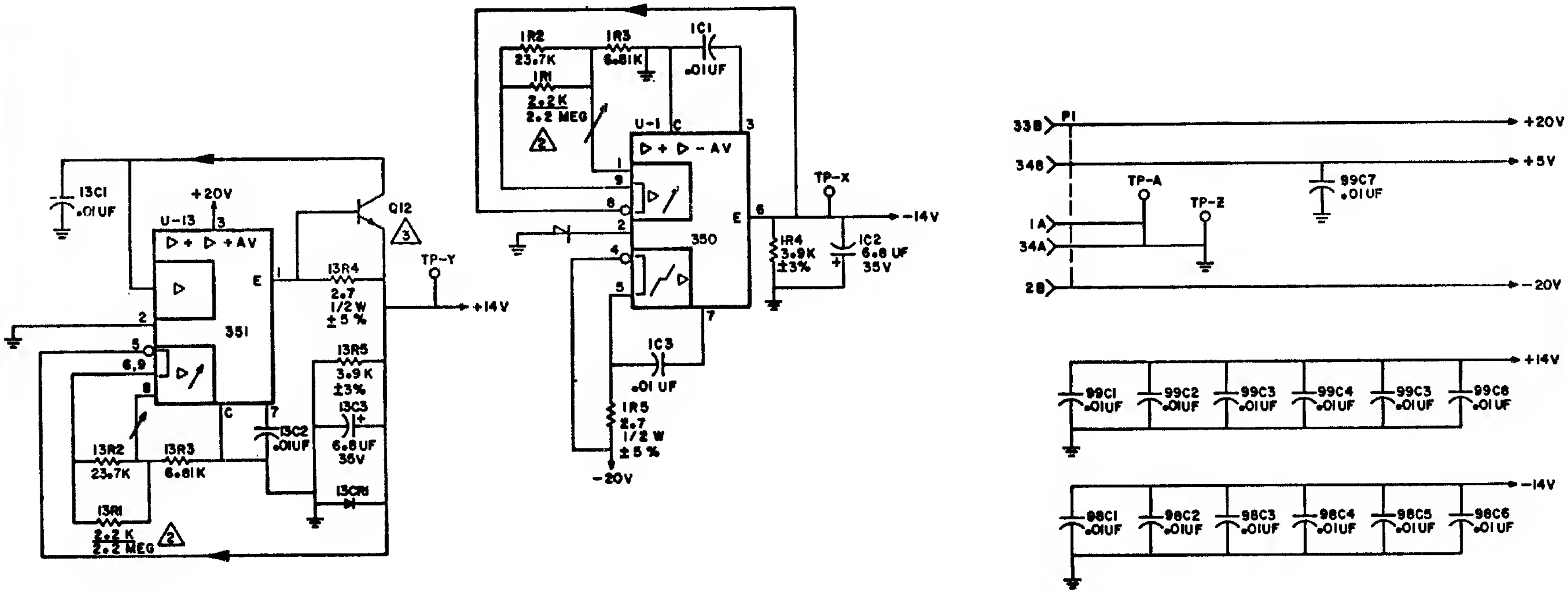
1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, FET'S 50218200
   ALL DIODES, GERMANIUM, 11801200
2. SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.
3. TRANSISTOR, 5NPN, 2N3646, 50210310.
4. IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
5. IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
6. MATCHED COMPONENTS. SEE 70740800.
7. DIODE, SILICON, 24553500
8. DIODE, ZENER, 50240111, ±5% TOLERANCE.
9. INSULATED JUMPER

REFERENCE DRAWINGS	CONTROL DATA NORMANDALE DIVISION	TITLE
COMP ASSY 54112513	NEXT USED ON: BR3A6	SCHEMATIC DIAGRAM VOLTAGE GENERATOR, TRACK SERVO TYPE KCGV
COMPONENTS EXCEPT AS NOTED	DWN / CHK / ENGR / MFG / APPR	CODE IDENT 19333 · C · DRAWING NUMBER 54112613 · CD 2
RES ±1% OHMS 1/4W		SHEET 1 OF 2
CAP -30%		

54112613

4-42.1

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



B54112613

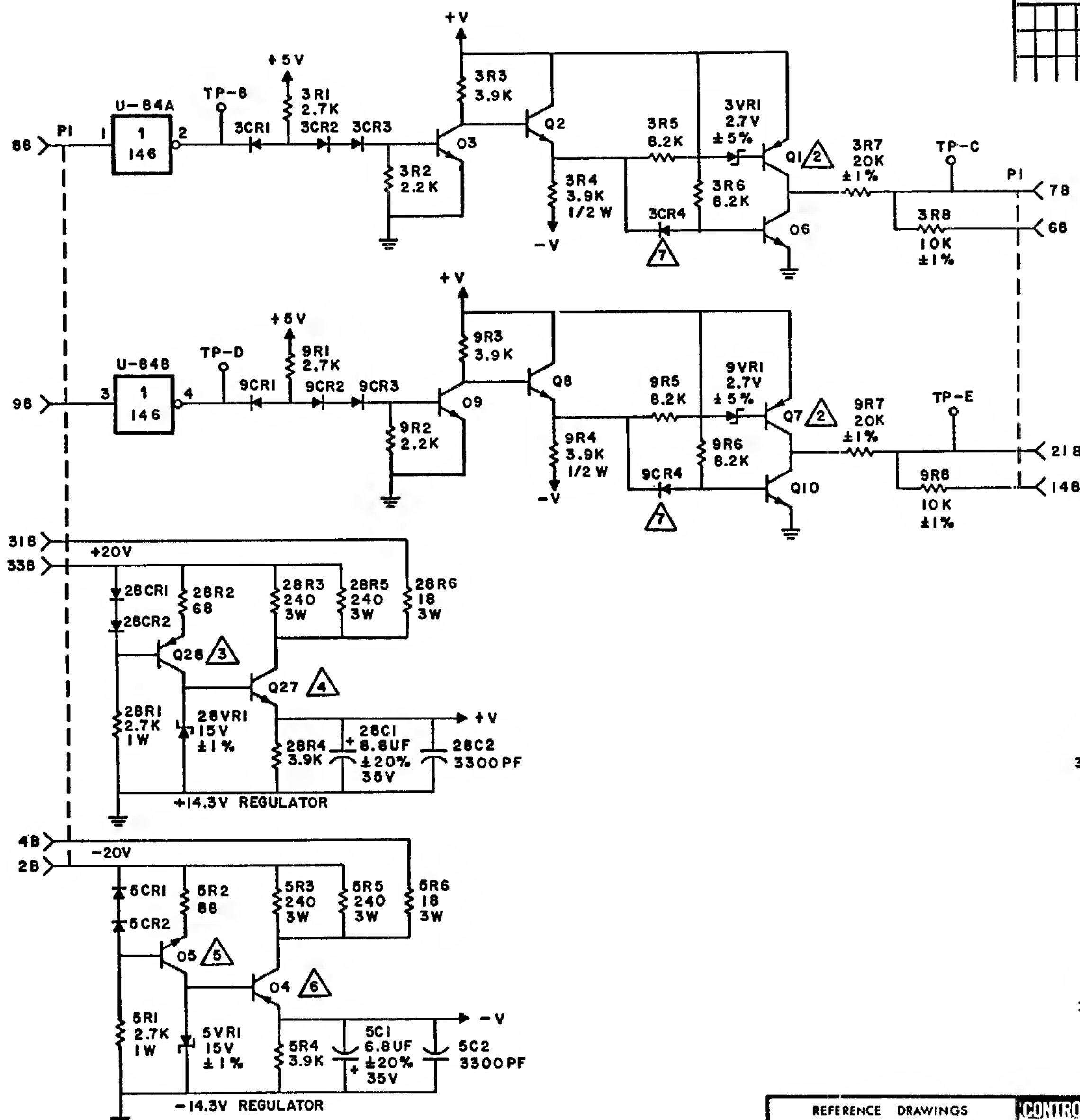
CONTROL DATA
NORMANDALE DIVISION

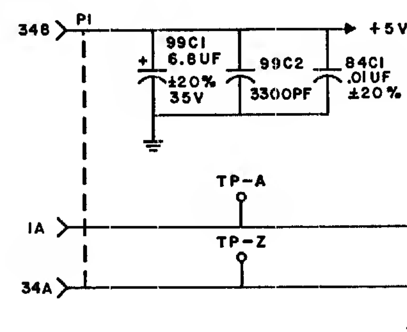
SCHEMATIC DIAGRAM
VOLTAGE GENERATOR,
TRACK SERVO
TYPE KCGV

CODE IDENT 19333 | C | DWG NO 54112613 | CD 2

SHEET 2

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED			[illegible]	[illegible]
	B	PE21812	28VR1 AND 5VR1 WERE 5% ASSY NO. WAS 54116500.	DM	[illegible]	[illegible]	INR
	C	PE29310 PE23000	DOC SIZE & SYM CHANGE	[illegible]	[illegible]	[illegible]	[illegible]





NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL TRANSISTORS SNPN, 2N3642, 50210510.
   ALL DIODES SILICON, 92115023

2. TRANSISTOR SILICON, PNP, 2N3638, 50210610.
3. TRANSISTOR SILICON, PNP, 2N4406, 50221500.
4. TRANSISTOR SILICON, NPN, 2N4922, 50220901.
5. TRANSISTOR SILICON, NPN, 2N3020, 50211900.
6. TRANSISTOR SILICON, PNP, 2N4919, 50221001.
7. DIODE GERMANIUM, 11801200.
8. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GRD AND PIN 14 TO +5V
9. +V = +14.3V
   -V = -14.3V

54116600 B

REFERENCE DRAWINGS
COMPONENT ASSY 54116501

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	G. MARTIN	5-20-70
CHK	D. RADCLIFFE	6-17-70
ENGR	R.E. McCANN	8-5-70
MFG	L.W. OLSON	8-26-70
APPD	T. McDONALD	8-27-70

TITLE

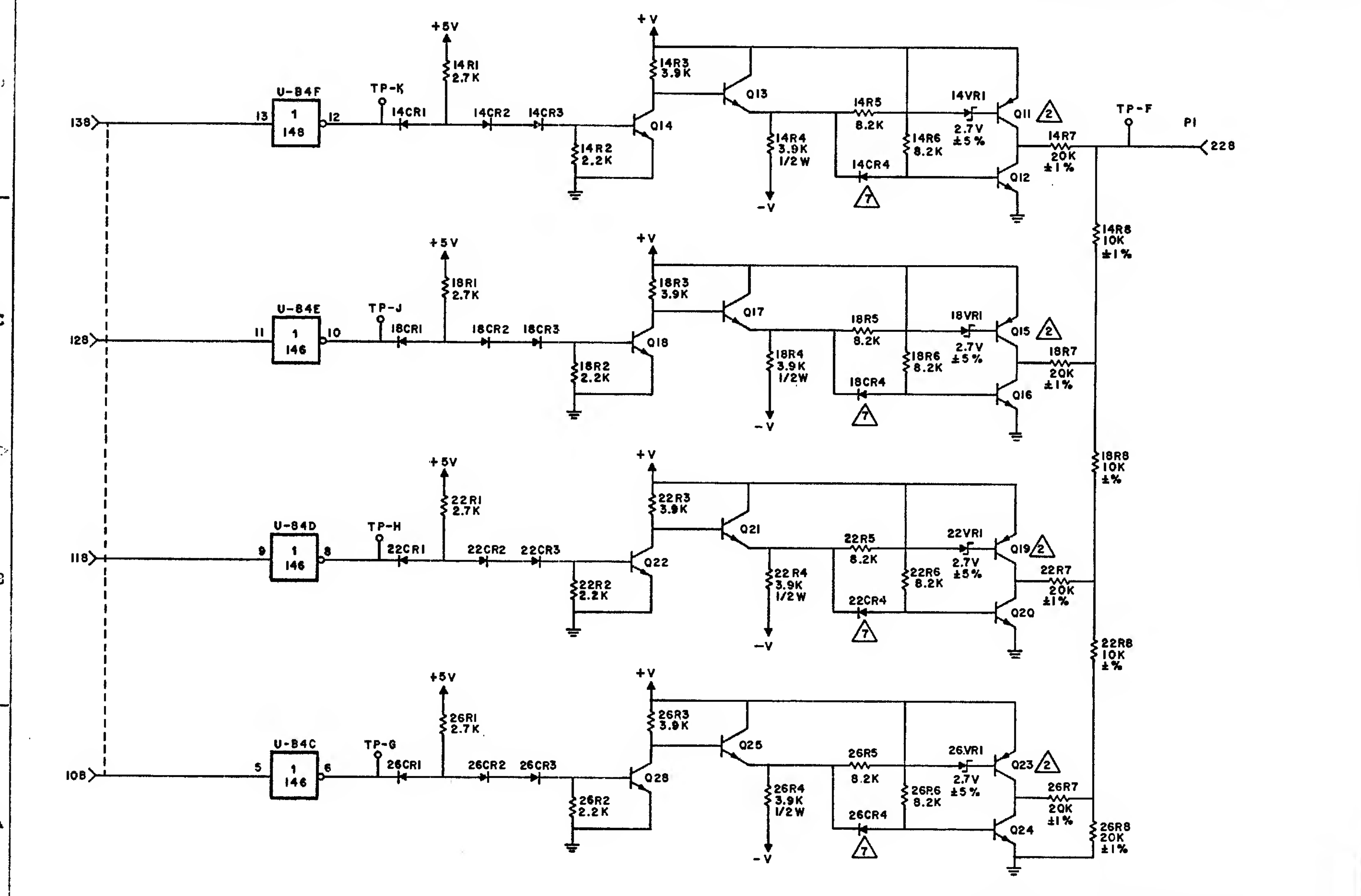
SCHEMATIC DIAGRAM D/A CONVERTER TYPE ØCSV

CODE IDENT 19333 — C — DRAWING NUMBER 54116600 — CD 5

SHEET 1 OF 2

REVISION RECORD

LTR	ECO	DESCRIPTION	DFT	DATE	CHKD	APP
C		SEE SHEET 1 FOR REV				

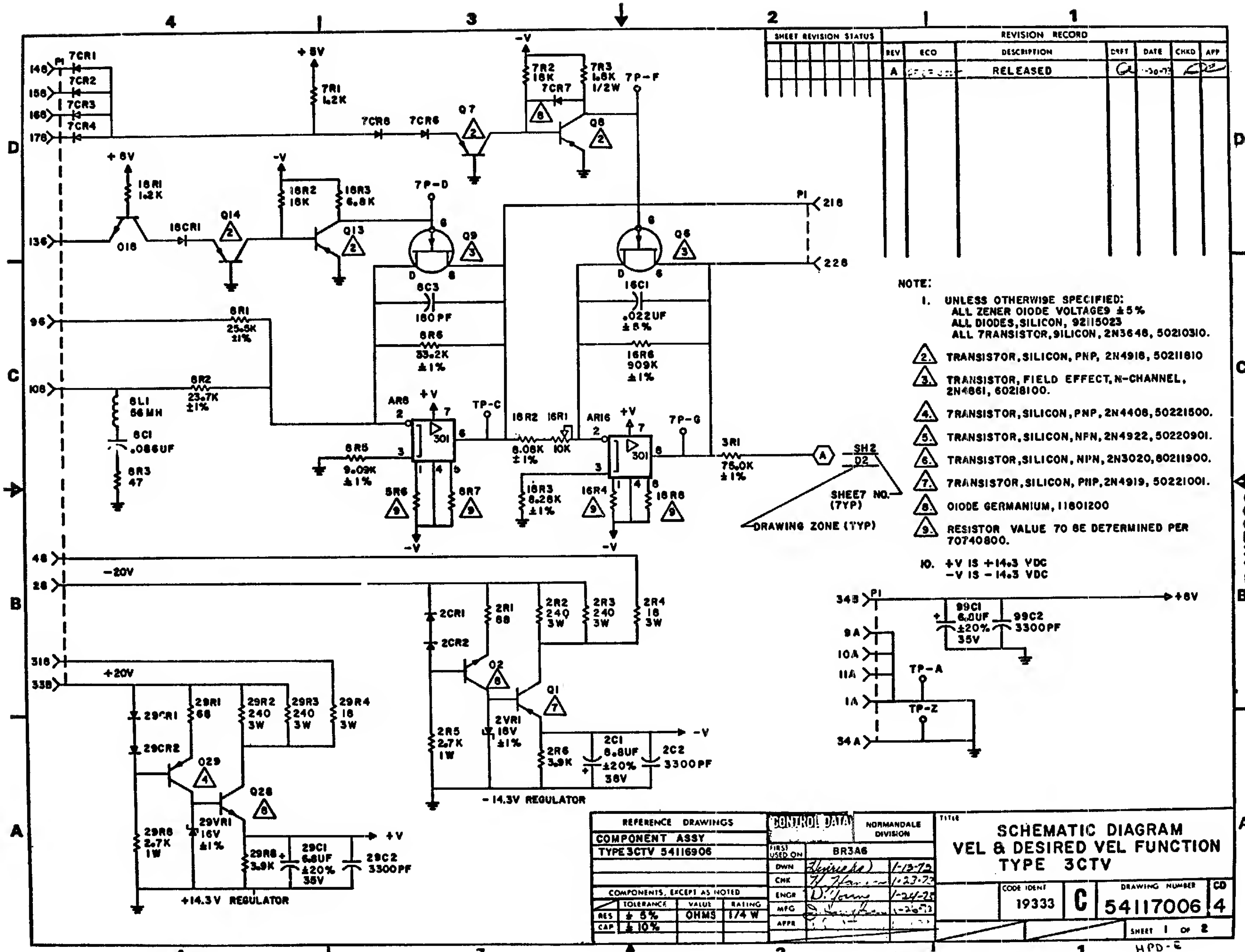


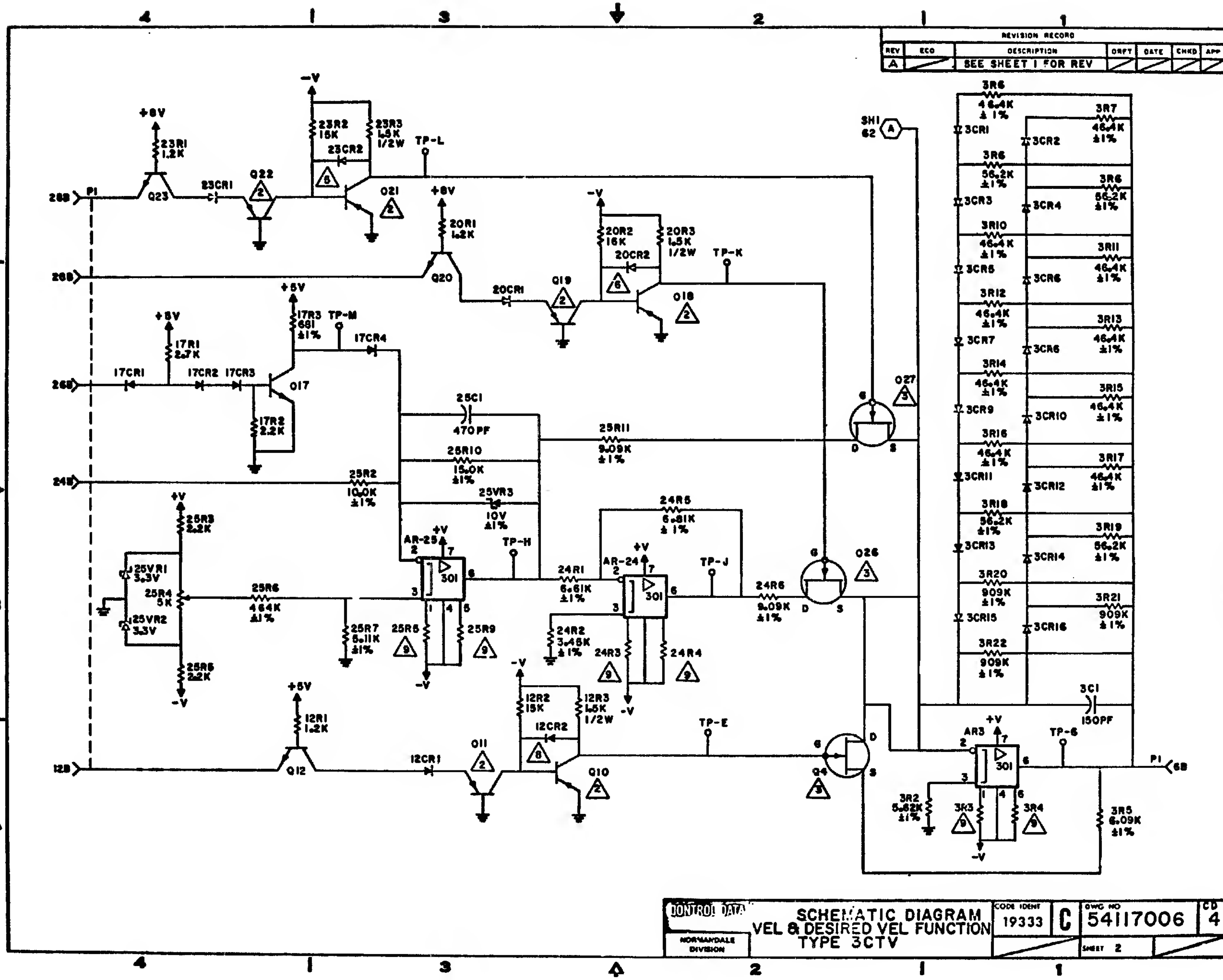
SCHEMATIC DIAGRAM
D/A CONVERTER
TYPE ØCSV

54116600 | CD 5 | SH 2

54116600

70629100 E


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | RELEASED
SHEET REVISION STATUS
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL ZENER DIODE VOLTAGES ±5%
ALL DIODES, SILICON, 92115023
ALL TRANSISTOR, SILICON, 2N3646, 50210310.
2 TRANSISTOR, SILICON, PNP, 2N4916, 50211610
3 TRANSISTOR, FIELD EFFECT, N-CHANNEL, 2N4861, 60218100.
4 TRANSISTOR, SILICON, PNP, 2N4408, 50221500.
5 TRANSISTOR, SILICON, NPN, 2N4922, 50220901.
6 TRANSISTOR, SILICON, NPN, 2N3020, 50211900.
7 TRANSISTOR, SILICON, PNP, 2N4919, 50221001.
8 DIODE GERMANIUM, 11801200
9 RESISTOR VALUE TO BE DETERMINED PER 70740800.
10. +V IS +14.3 VDC
-V IS -14.3 VDC
SHEET NO. (TYP)
DRAWING ZONE (TYP)
-14.3V REGULATOR
+14.3V REGULATOR
REFERENCE DRAWINGS
COMPONENT ASSY
TYPE 3CTV 54116906
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ± 5% | OHMS | 1/4 W
CAP ± 10%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3A6
DWN 1-13-72
CHK 1-23-72
ENGR 1-24-72
MFG
APPR
TITLE
SCHEMATIC DIAGRAM
VEL & DESIRED VEL FUNCTION
TYPE 3CTV
CODE IDENT 19333
C
DRAWING NUMBER 54117006
CD 4
SHEET 1 OF 2
HPD-E
54117006



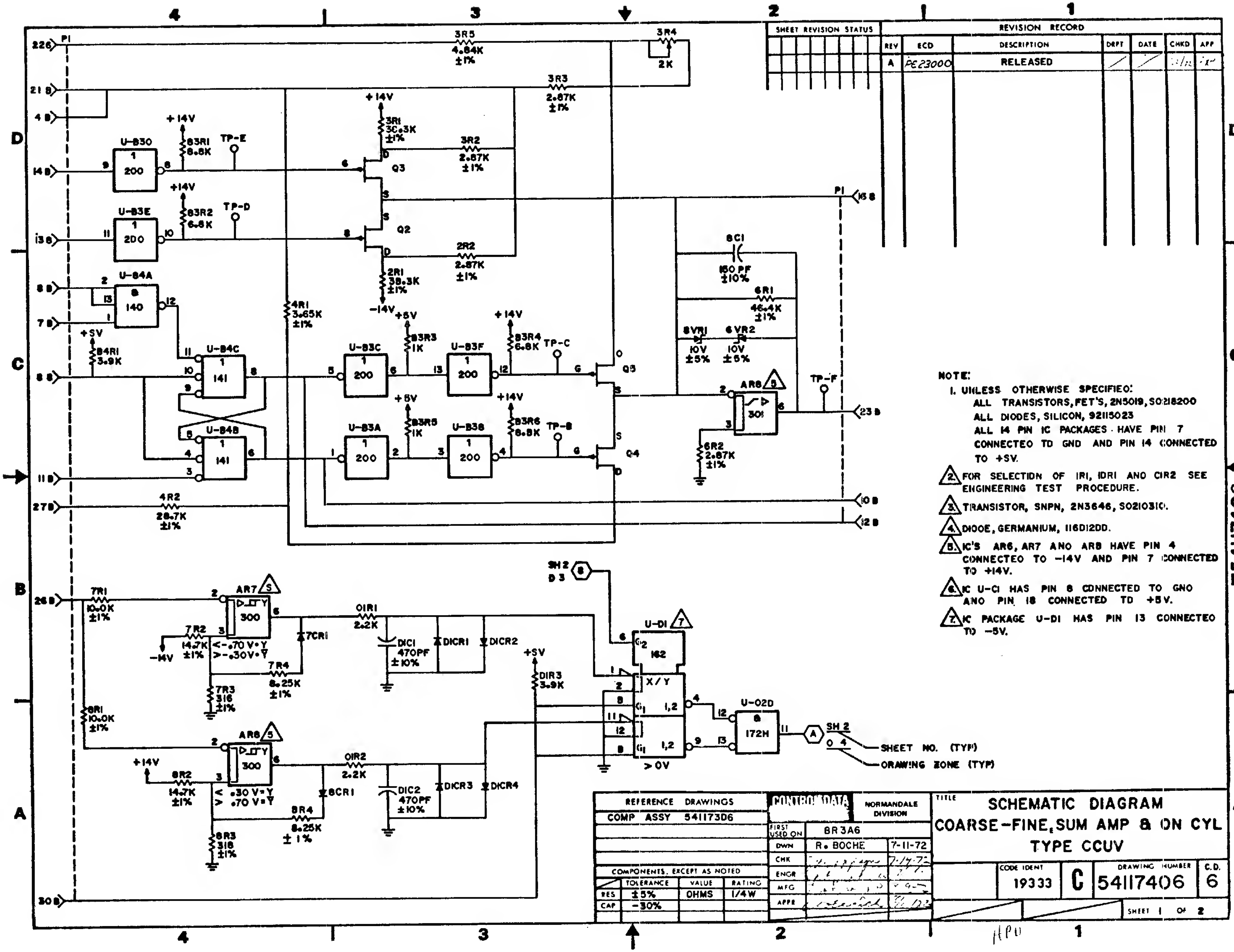
CONTROL DATA

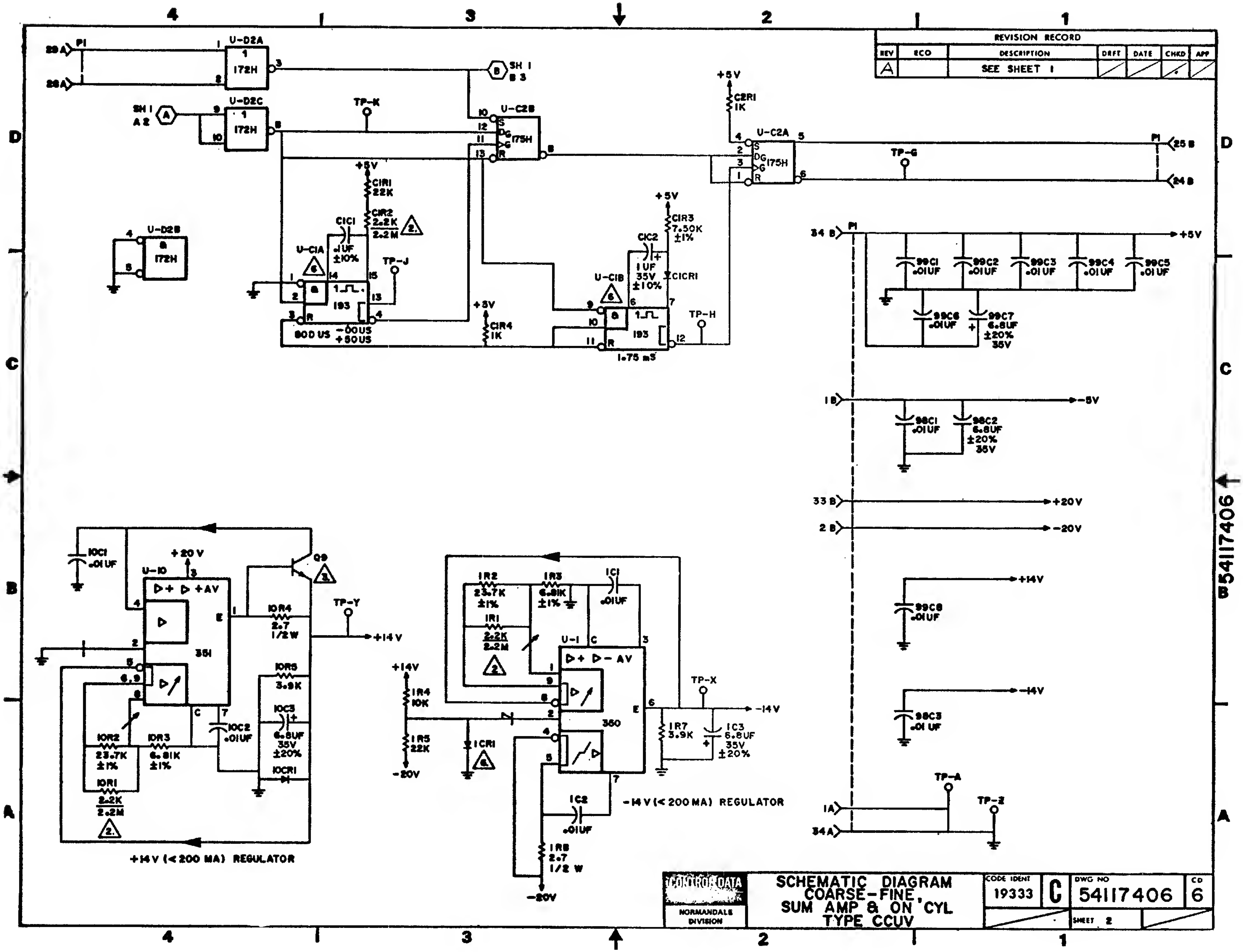
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
VEL & DESIRED VEL FUNCTION
TYPE 3CTV

CODE IDENT		DWG NO	CD
19333	C	54117006	4
		SHEET 2	

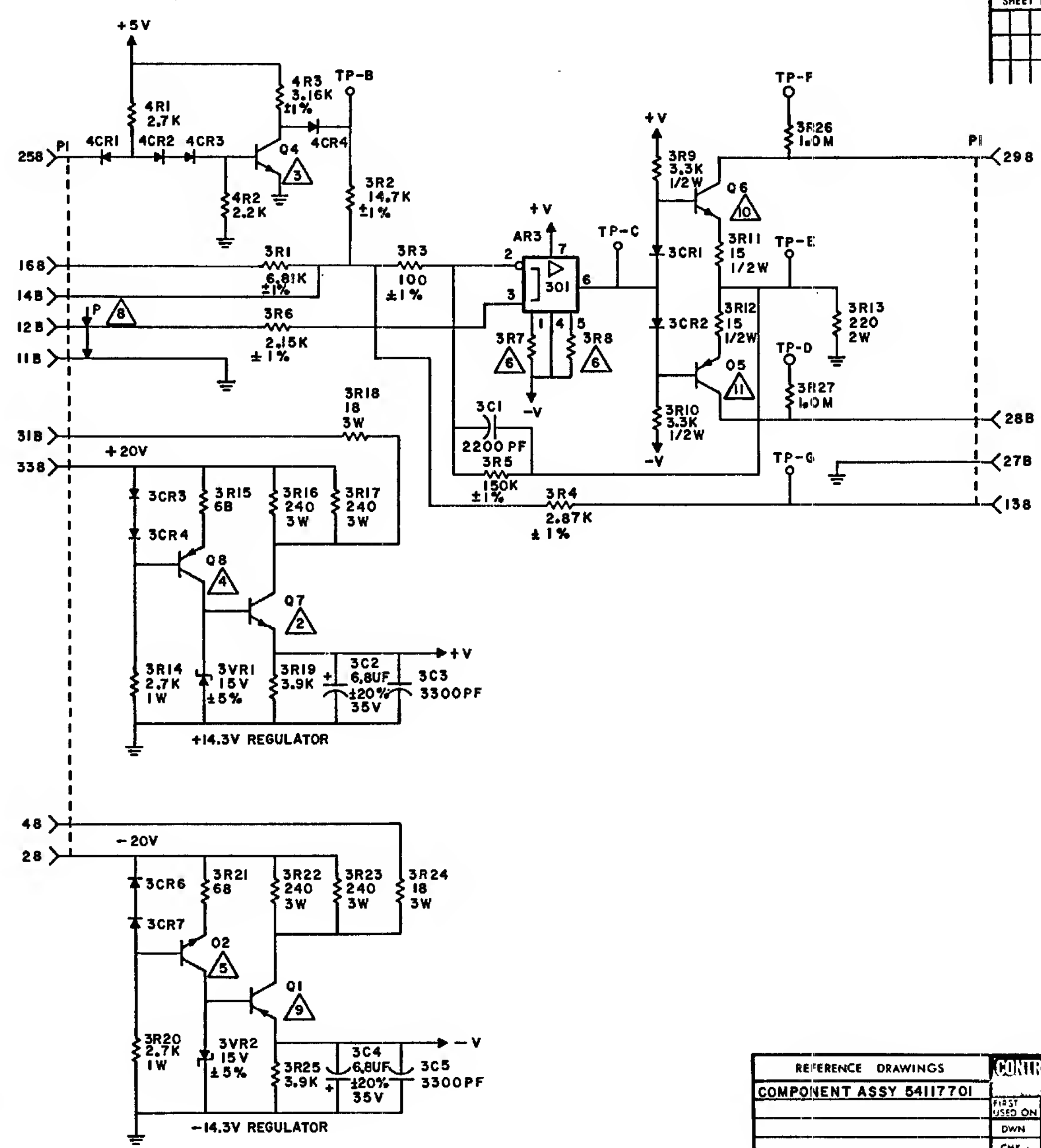
70629100 E


SHEET REVISION STATUS
REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A PE23000 RELEASED
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, FET'S, 2N5019, 50218200
ALL DIODES, SILICON, 92115023
ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. FOR SELECTION OF 1R1, 1DR1 AND 1CR2 SEE ENGINEERING TEST PROCEDURE.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. DIODE, GERMANIUM, 116D1200.
5. IC'S AR6, AR7 AND AR8 HAVE PIN 4 CONNECTED TO −14V AND PIN 7 CONNECTED TO +14V.
6. IC U-C1 HAS PIN 8 CONNECTED TO GND AND PIN 18 CONNECTED TO +5V.
7. IC PACKAGE U-D1 HAS PIN 13 CONNECTED TO −5V.
SHEET NO. (TYP)
DRAWING ZONE (TYP)
REFERENCE DRAWINGS
COMP ASSY 54117306
COMPONENTS, EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHMS 1/4W
CAP −30%
CONTROL DATA NORMANDALE DIVISION
FIRST USED ON 8R3A6
DWN R. BOCHE 7-11-72
CHK
ENGR
MFG
APPR
TITLE SCHEMATIC DIAGRAM
COARSE-FINE, SUM AMP & ON CYL
TYPE CCUV
CODE IDENT 19333
C
DRAWING NUMBER 54117406
C.D. 6
SHEET 1 OF 2
54117406 B


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
+14V (< 200 MA) REGULATOR
-14V (< 200 MA) REGULATOR
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM COARSE-FINE SUM AMP & ON CYL TYPE CCUV
CODE IDENT 19333
C
DWG NO 54117406
CD 6
SHEET 2
54117406

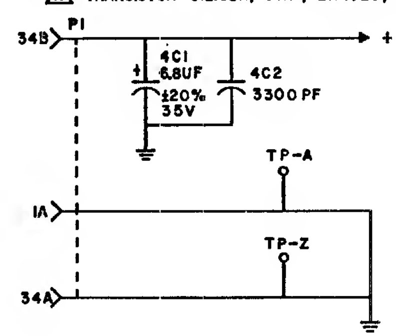
70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL DIODES SILICON, 92115023
2. TRANSISTOR SILICON, NPN, 2N4922, 50220901.
3. TRANSISTOR SILICON, NPN, 2N3646, 50210310.
4. TRANSISTOR SILICON, PNP, 2N4406, 50221500.
5. TRANSISTOR SILICON, NPN, 2N3020, 50211900.
6. RESISTOR VALUE TO BE SELECTED PER 70740800.
7. +V IS +14.3 VDC
   -V IS -14.3 VDC
8. PAIRED CONDUCTORS ARE NOT TWISTED.
9. TRANSISTOR SILICON PNP, 2N4919, 50221001.
10. TRANSISTOR SILICON, NPN, 2N4923, 50220902
11. TRANSISTOR SILICON, PNP, 2N4920, 50221002



54117801

REFERENCE DRAWINGS
COMPONENT ASSY 54117701

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	8R301	
DWN	K STREETER	10-2-71
CHK	H. Hansen	10-5-71
ENGR		10/5/71
MFG		10/5/71
APPR		10-6-71

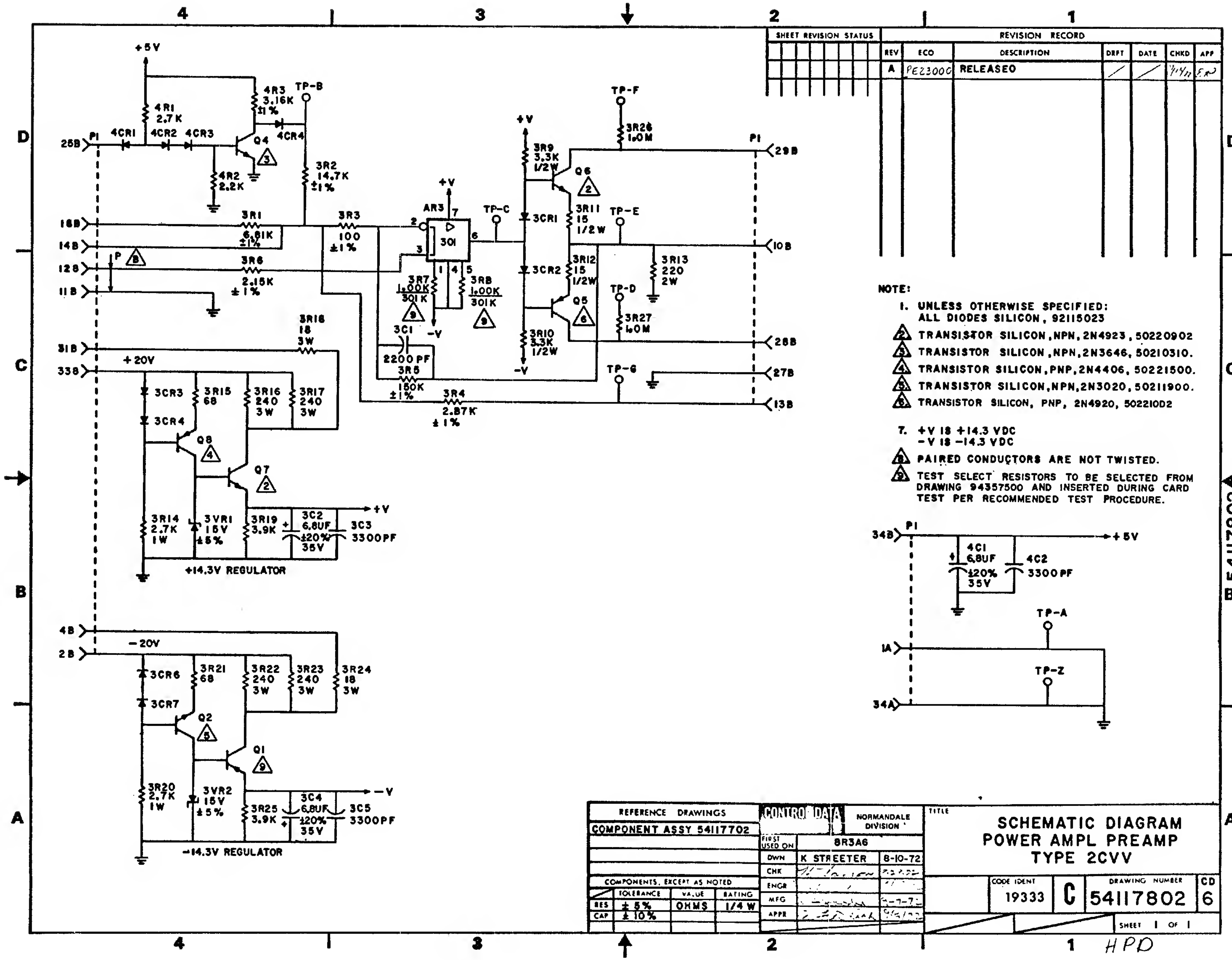
TITLE

SCHEMATIC DIAGRAM POWER AMPL PREAMP TYPE 1CVV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54117801	8

SHEET 1 OF 1

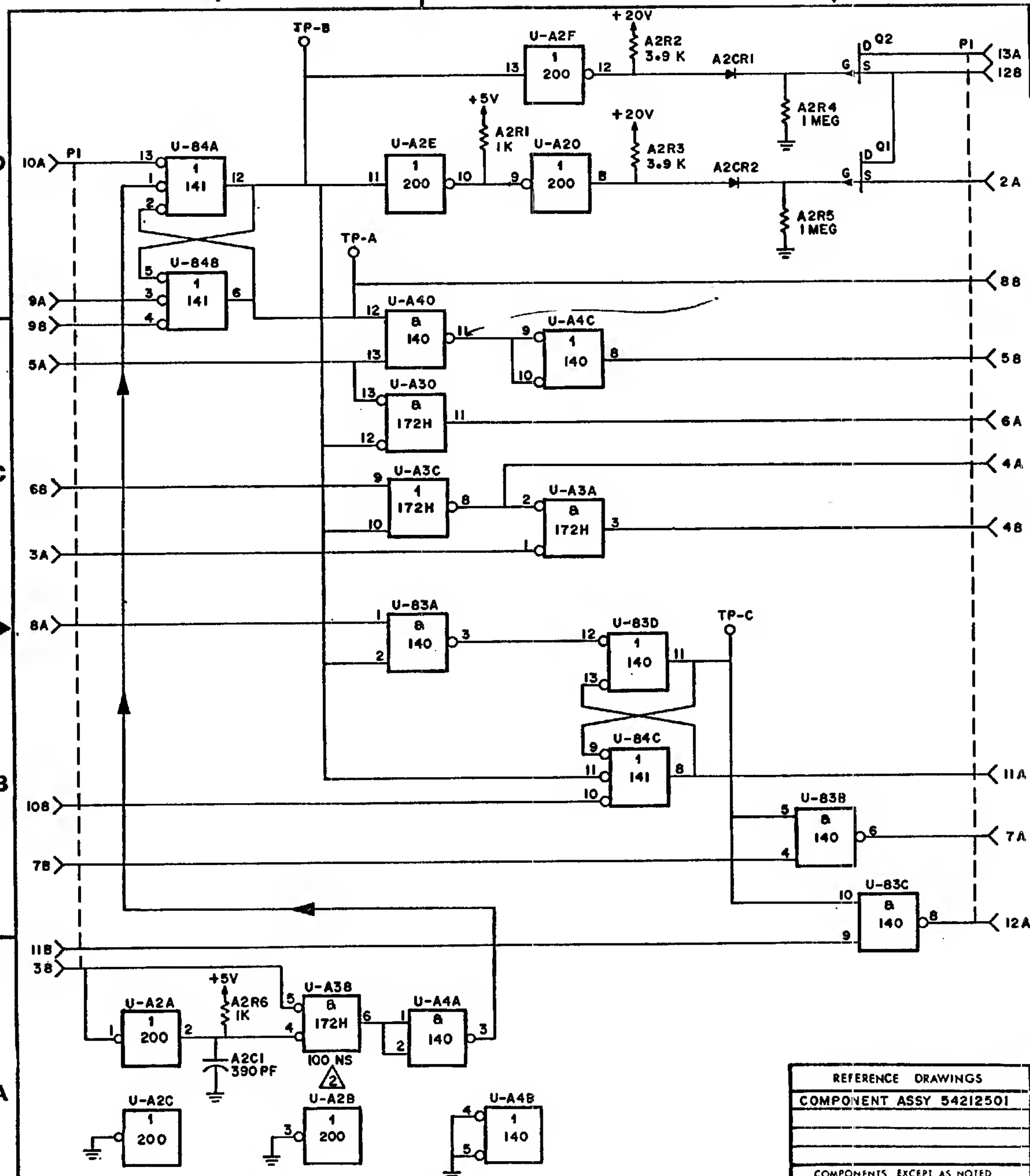
HPD


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23000 | RELEASED
+5V
4R1 2.7K
4R3 3.16K ±1%
TP-B
4CR1 4CR2 4CR3 4CR4
Q4
4R2 2.2K
3R2 14.7K ±1%
25B P1
18B 14B 12B 11B
3R1 6.81K ±1%
3R3 100 ±1%
P
3R6 2.15K ±1%
AR3 301
+V
TP-C
3R7 1.00K 301K
3R8 1.00K 301K
-V
3C1 2200 PF
3R5 150K ±1%
3R4 2.87K ±1%
+V
3R9 3.3K 1/2W
Q6
3CR1
3R11 15 1/2W
TP-E
3CR2
3R12 15 1/2W
3R13 220 2W
Q5
3R10 3.3K 1/2W
-V
TP-F
3R26 1.0M
29B
10B
TP-D
3R27 1.0M
28B
TP-G
27B
13B
31B
33B
+20V
3R18 18 3W
3CR3 3R15 68 3R16 240 3W 3R17 240 3W
3CR4
Q8
Q7
3R14 2.7K 1W
3VR1 15V ±5%
3R19 3.9K
3C2 6.8UF ±20% 35V
3C3 3300PF
+V
+14.3V REGULATOR
4B
2B
-20V
3CR6 3R21 68 3R22 240 3W 3R23 240 3W 3R24 18 3W
3CR7
Q2
Q1
3R20 2.7K 1W
3VR2 15V ±5%
3R25 3.9K
3C4 6.8UF ±20% 35V
3C5 3300PF
-V
-14.3V REGULATOR
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL DIODES SILICON, 92115023
2 TRANSISTOR SILICON, NPN, 2N4923, 50220902
3 TRANSISTOR SILICON, NPN, 2N3646, 50210310.
4 TRANSISTOR SILICON, PNP, 2N4406, 50221500.
5 TRANSISTOR SILICON, NPN, 2N3020, 50211900.
6 TRANSISTOR SILICON, PNP, 2N4920, 50221002
7. +V IS +14.3 VDC
-V IS -14.3 VDC
8 PAIRED CONDUCTORS ARE NOT TWISTED.
9 TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
34B P1
+5V
4C1 6.8UF ±20% 35V
4C2 3300PF
TP-A
1A
TP-Z
34A
54117802
REFERENCE DRAWINGS
COMPONENT ASSY 54117702
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON 8R3A6
DWN K STREETER 8-10-72
CHK
ENGR
MFG
APPR
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ± 5% | OHMS | 1/4 W
CAP ± 10%
TITLE
SCHEMATIC DIAGRAM
POWER AMPL PREAMP
TYPE 2CVV
CODE IDENT 19333
C
DRAWING NUMBER 54117802
CD 6
SHEET 1 OF 1
HPD

SHEET REVISION STATUS										

REVISION RECORD

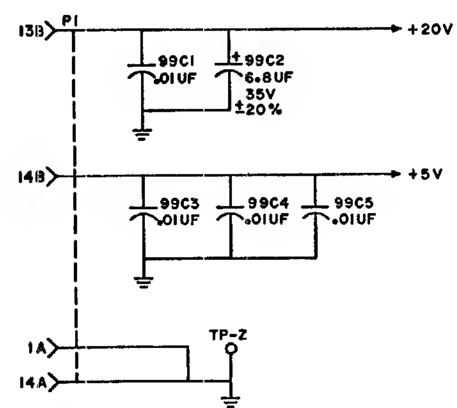
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	FE23000	RELEASED		4-28-72		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, P CHANNEL J FET, 50218200.
   ALL DIODES, SILICON, 24553500.
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMPONENT ASSY 54212501

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	8R3AIG
DWN	R. KONECNY
CHK	W. Hanson
ENGR	F.R.B. / W.A.R.
MFG	
APPR	

TITLE: SCHEMATIC DIAGRAM OFFSET CONTROL TYPE AEGV

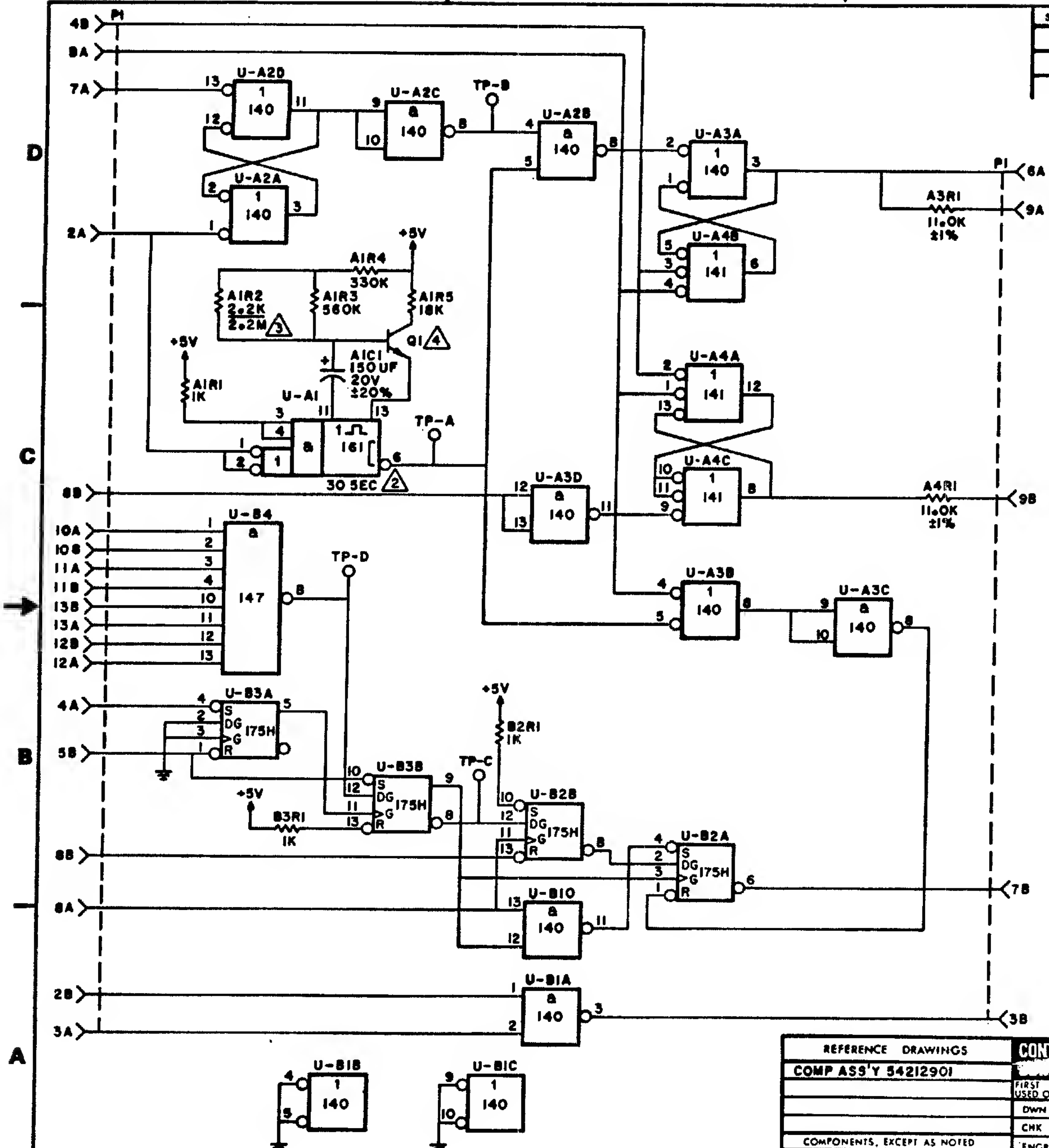
CODE IDENT		DRAWING NUMBER	CO
19333	C	54212601	6

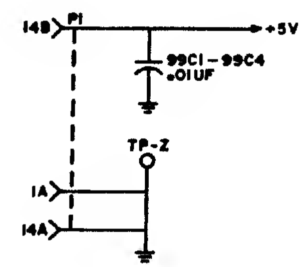
SHEET 1 OF 1

54212601

HPD

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED				





NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIMES FOR REFERENCE ONLY.
3. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 46325900 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
4. TRANSISTOR, SNPN, 2N3565, 50210710.

REFERENCE DRAWINGS
COMP ASS'Y 54212901

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR3A8B	
DWN	S. ZAK	10-16-72
CHK		10-20-72
ENGR		
MFG		
APPR		

TITLE
SCHEMATIC DIAGRAM UNLOAD/RELOAD & INDEX ERROR TYPE AEHV

CODE IDENT		DRAWING NUMBER	C.O.
19333	C	54213001	8

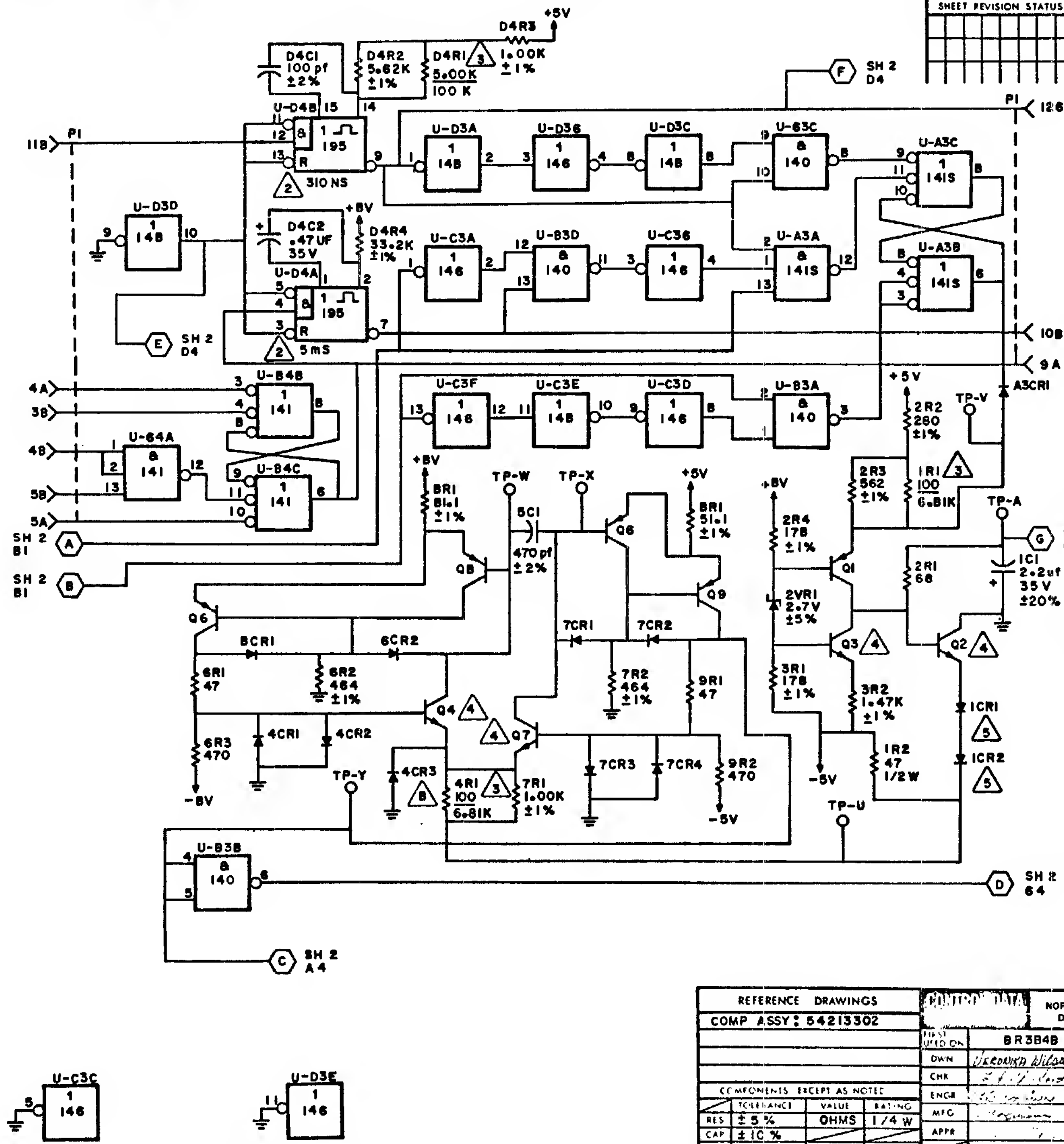
SHEET 1 OF 1

HPD

54213001

70629100 E

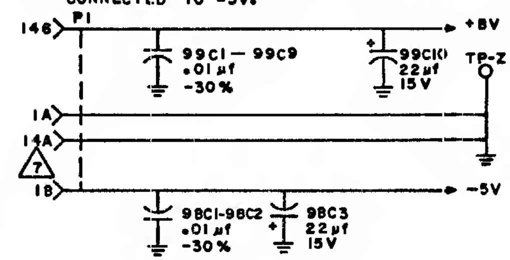
SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE[illegible]	RELEASED		[illegible]		[illegible]



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   ALL DIODES, SILICON, SCHOTTY, 50241400.

2. DELAY TIME FOR REFERENCE ONLY.
3. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMEDED TEST PROCEDURE.
4. ALL TRANSISTORS, SNPN, 2N3648, 50210310.
5. DIODES, SILICON, 92115023.
6. DIODES, SILICON, 92115021.
7. CONNECTOR PINS 2,3,10,11,12,13, ROW A ARE GROUNDED.
8. IC U-A2, ELEMENT NO. 162, HAS PIN 13 CONNECTED TO -5V.



REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMP ASSY: 54213302	FIRST USED ON	BR3B4B
	DWN	Veronica Wilson 8/30/73
	CHK	[illegible]
	ENGR	[illegible]
	MFG	[illegible]
	APPR	

COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

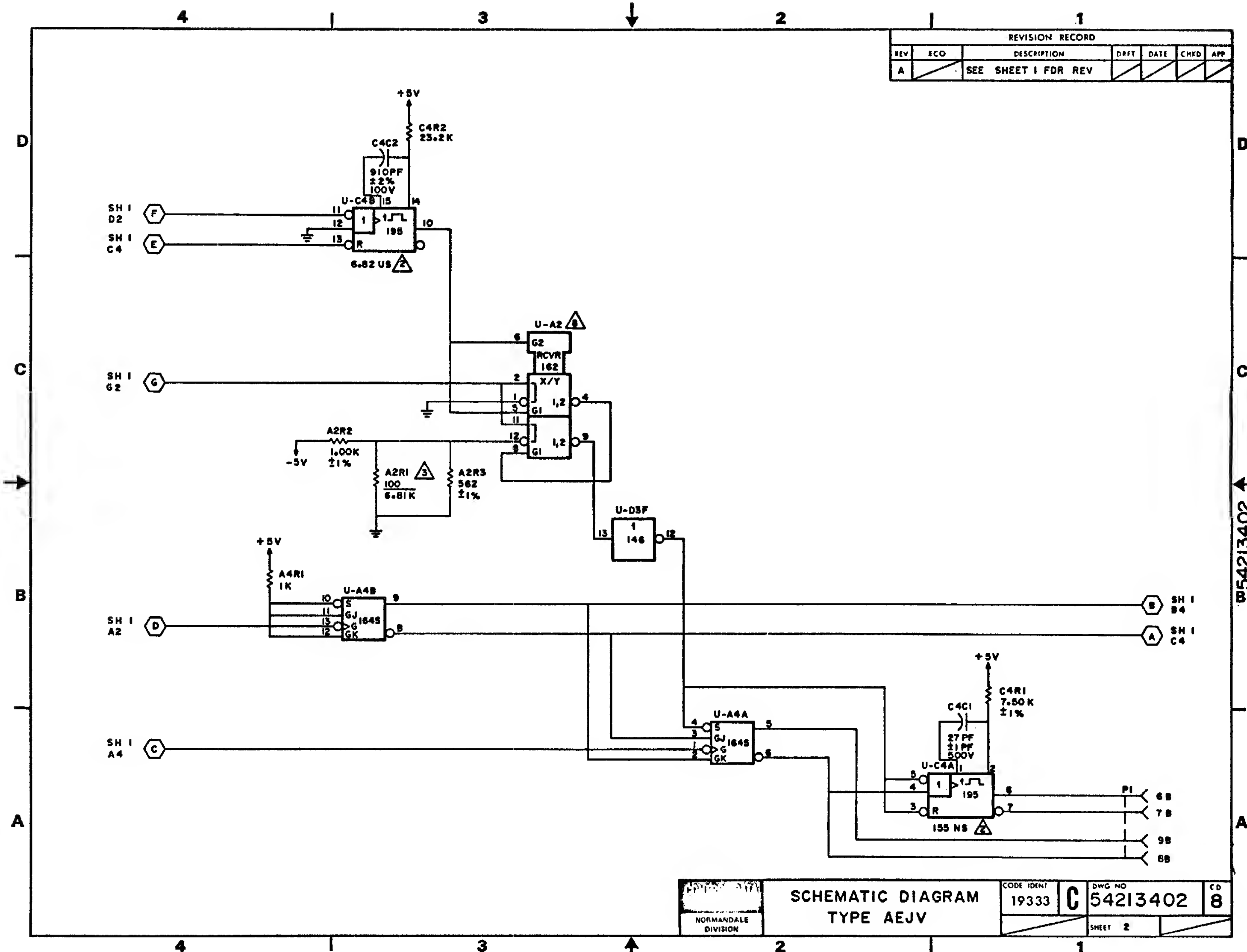
SCHEMATIC DIAGRAM 806 KHZ PLO TYPE AEJV

CODE IDENT 19333 | C | DRAWING NUMBER 54213402 | CD 8

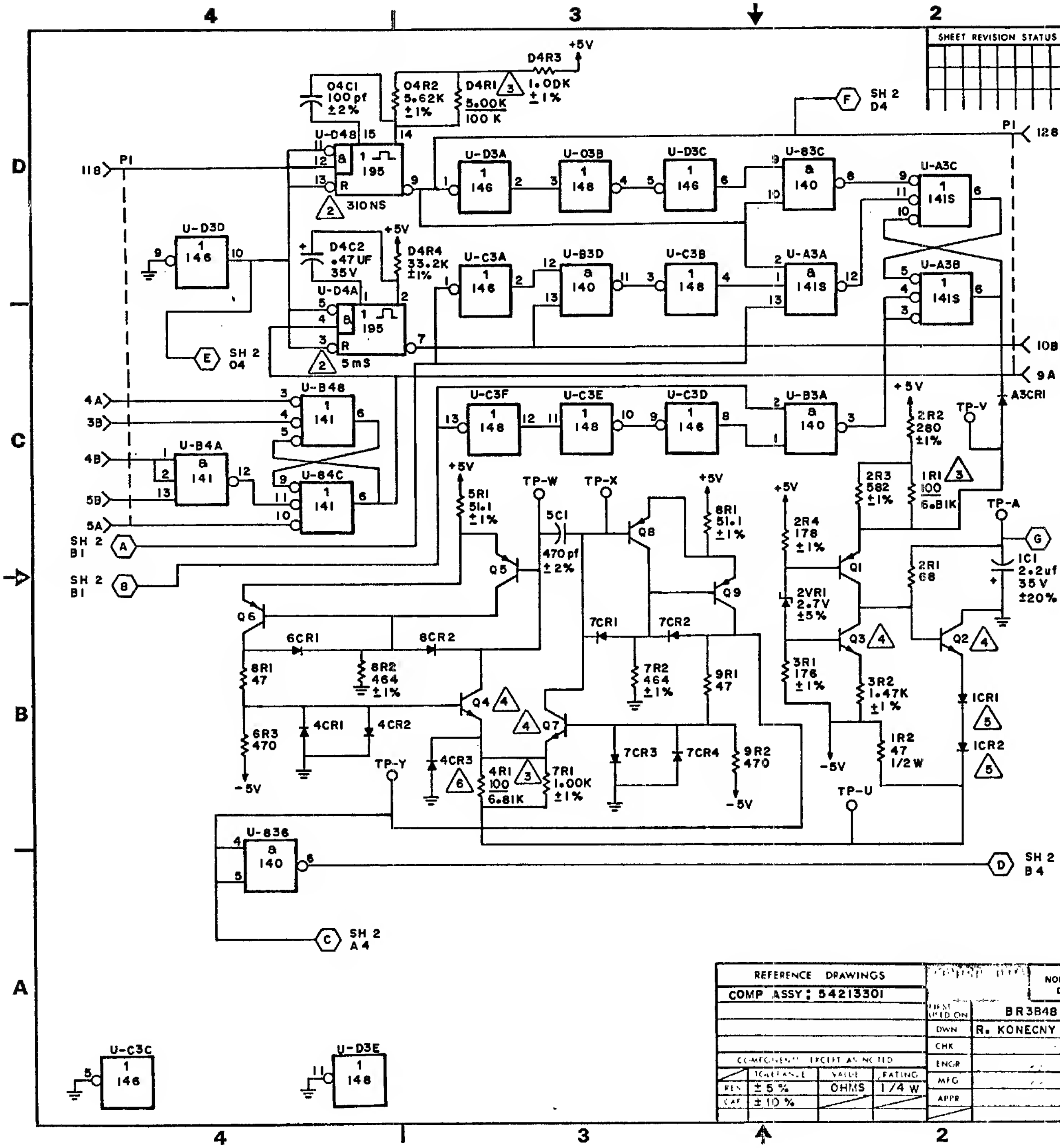
SHEET 1 OF 2

54213402

HPD


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
+5V
C4R2 23.2K
C4C2 910PF ±2% 100V
U-C4B 195
6.82 US
SH 1 D2
SH 1 C4
U-A2 RCVR 162
X/Y
SH 1 G2
A2R2 1.00K ±1%
-5V
A2R1 100 / 6.81K
A2R3 562 ±1%
U-D3F 146
+5V
A4R1 1K
U-A4B 164S
SH 1 A2
SH 1 B4
SH 1 C4
U-A4A 164S
SH 1 A4
+5V
C4R1 7.50K ±1%
C4C1 27 PF ±1 PF 500V
U-C4A 195
155 NS
P1
6B
7B
9B
8B
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE AEJV
CODE IDENT 19333
C
DWG NO 54213402
CD 8
SHEET 2
54213402

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED				



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.
   - ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
   - ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   - ALL DIODES, SILICON, SCHOTTY, 50241400.

2. DELAY TIME FOR REFERENCE ONLY.

3. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.

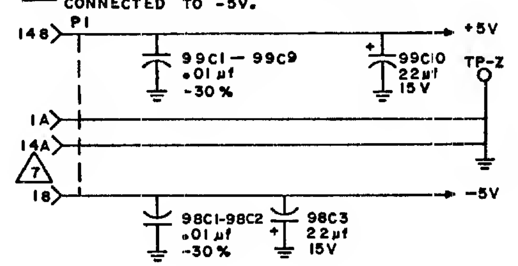
4. ALL TRANSISTORS, SNPN, 2N3646, 50210310.

5. DIODES, SILICON, 92115023.

6. DIODES, SILICON, 92115021.

7. CONNECTOR PINS 2,3,10,11,12,13, ROW A ARE GROUNDED.

8. IC U-A2, ELEMENT NO. 162, HAS PIN 13 CONNECTED TO -5V.



REFERENCE DRAWINGS	
COMP ASSY: 54213301	
COMPONENTS EXCEPT AS NOTED	
TOLERANCE / VALUE / RATING	
RES: ±5%	OHMS, 1/4 W
CAP: ±10%	

NORMANDALE DIVISION

FIRST USED ON: BR3848

DWN: R. KONECNY 5-21-73

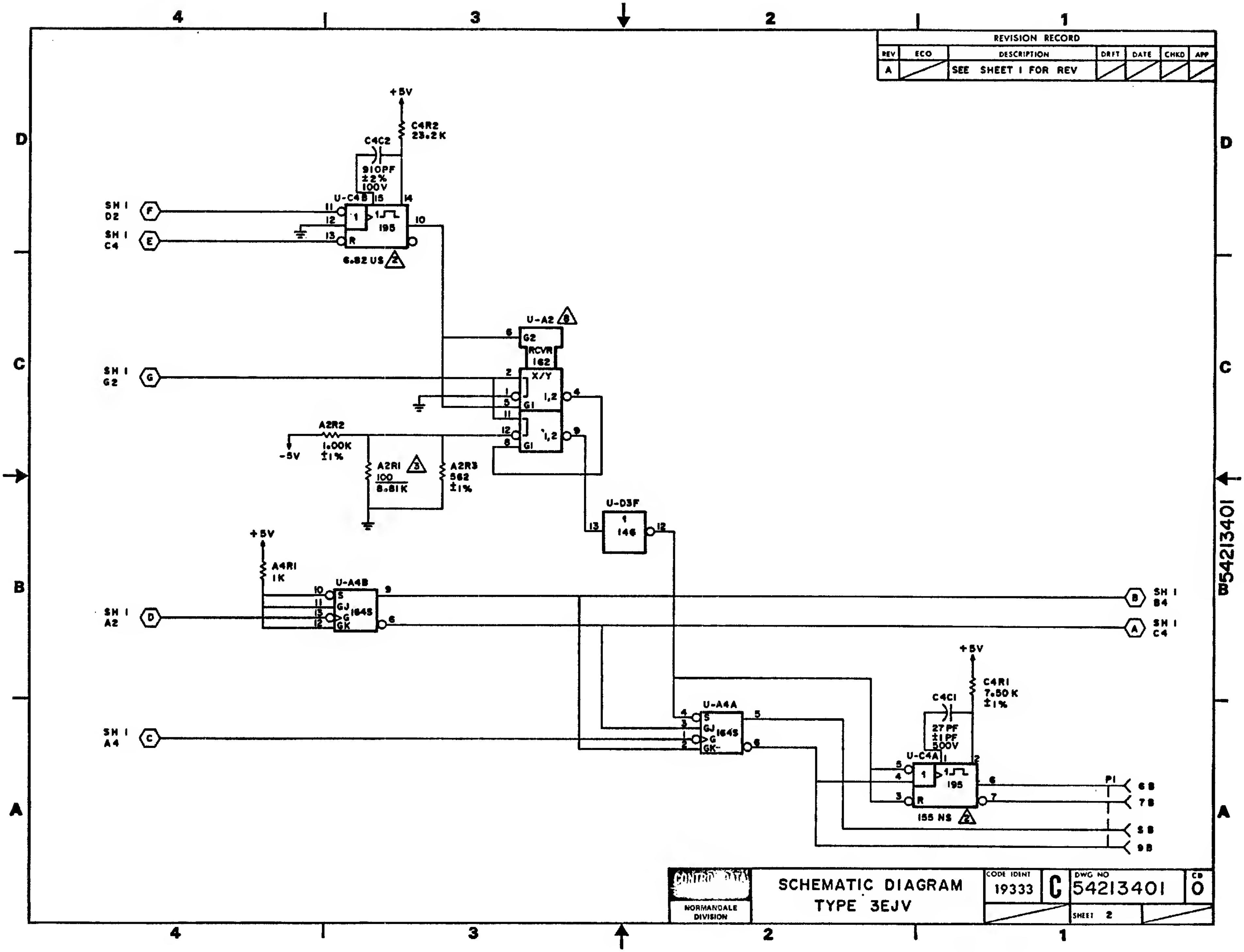
CHK / ENGR / MFG / APPR

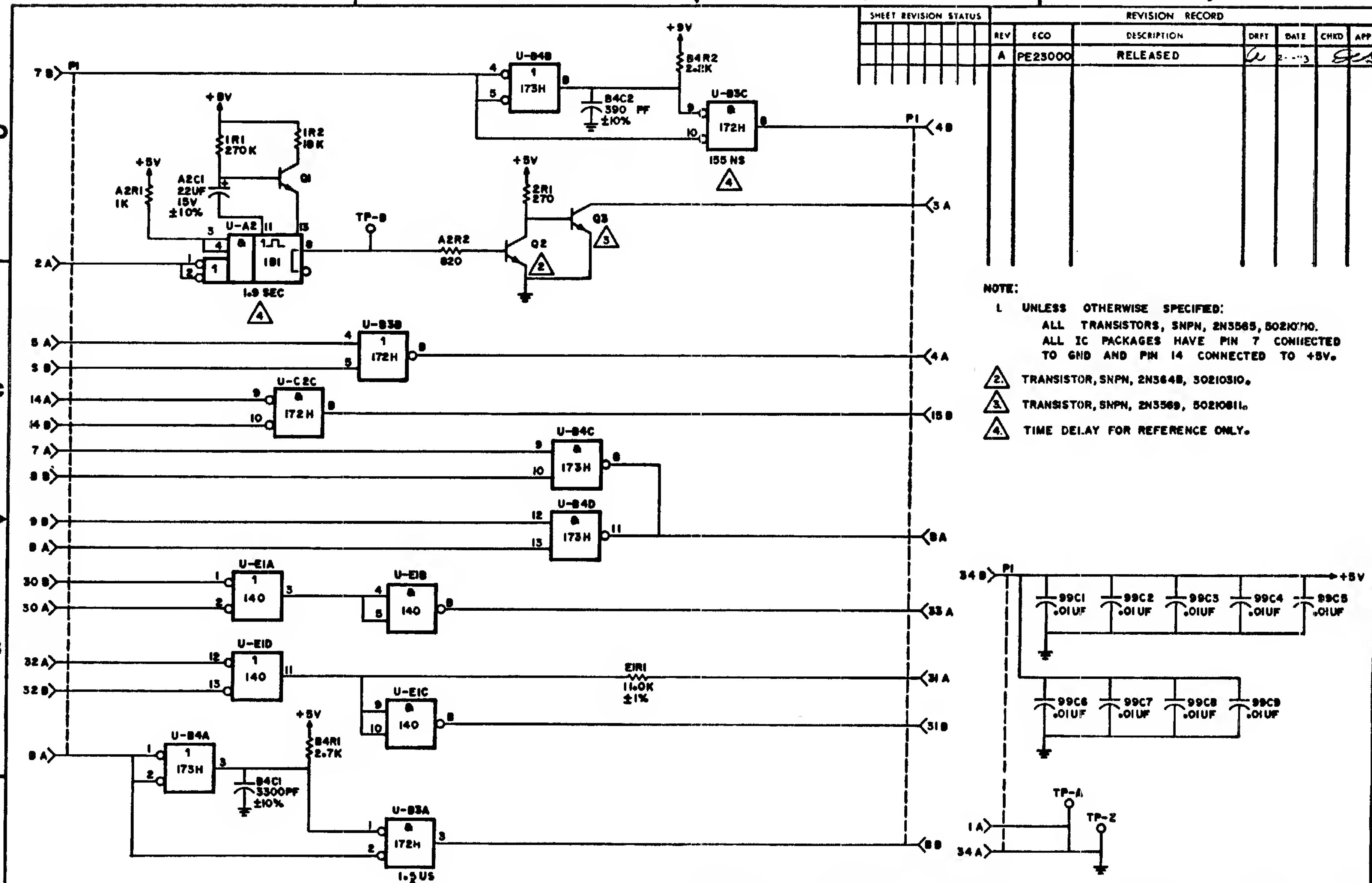
TITLE: SCHEMATIC DIAGRAM 806 KHZ PLO TYPE 3EJV

CODE IDENT 19333 | C | DRAWING NUMBER 54213401 | CD 0

SHEET 1 OF 2

54213401


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
+5V
C4R2 23.2K
C4C2 910PF ±2% 100V
U-C4B
195
6.82 US
SH 1 D2
SH 1 C4
U-A2
RCVR 162
X/Y
SH 1 G2
A2R2 1.00K ±1%
-5V
A2R1 100 8.81K
A2R3 562 ±1%
U-D3F
146
+5V
A4R1 1K
U-A4B
164S
SH 1 A2
SH 1 B4
SH 1 C4
SH 1 A4
U-A4A
164S
+5V
C4R1 7.50K ±1%
C4C1 27PF ±1PF 500V
U-C4A
195
155 NS
P1
6B
7B
8B
9B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 3EJV
CODE IDENT 19333
C
DWG NO 54213401
CD 0
SHEET 2
54213401



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3565, 50210710.
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. TRANSISTOR, SNPN, 2N3648, 50210310.

3. TRANSISTOR, SNPN, 2N3569, 50210811.

4. TIME DELAY FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASSY 54215701

COMPONENTS EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

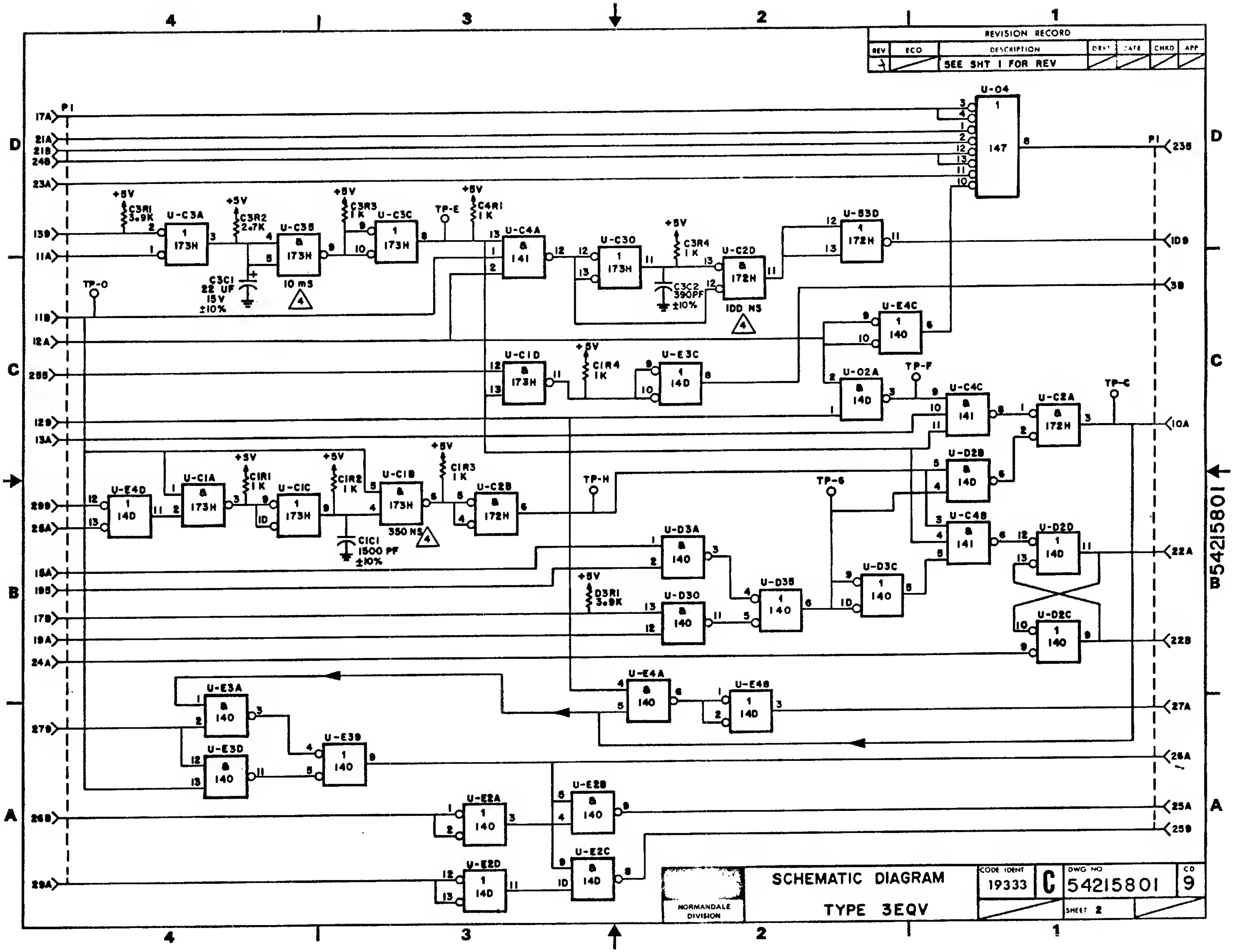
BR3AIG

DWN		1-25-73
CHK		1-25-73
ENGR		1-7-73
MFG		2-9-73
APPR		

SCHEMATIC DIAGRAM
WRITE SYNC CLOCK, CYL PULSE
AFY, PARITY ERROR, COVER LATCH
TYPE 3EQV

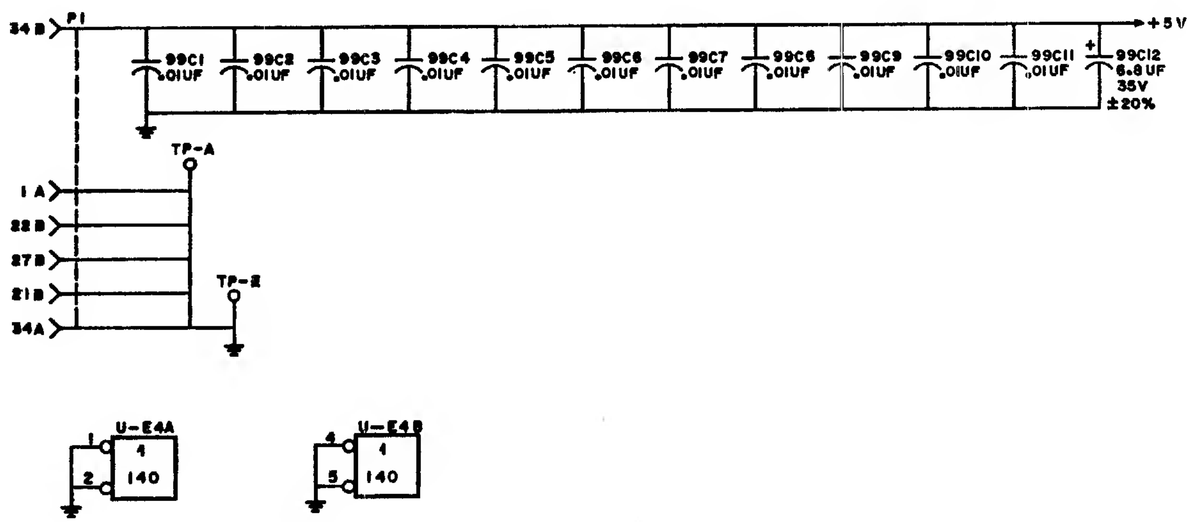
CODE IDENT 19333 — C — DRAWING NUMBER 54215801 — C.D. 9

SHEET 1 OF 2


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
SEE SHT 1 FOR REV
SCHEMATIC DIAGRAM
TYPE 3EQV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54215801
CD 9
SHEET 2
54215801

70629100 E

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N2221, 50210102.
   ALL DIODES, SILICON, 24553500.
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIMES FOR REF ONLY.

54216201

REFERENCE DRAWINGS			
COMP ASSY 54216101			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	–30%		

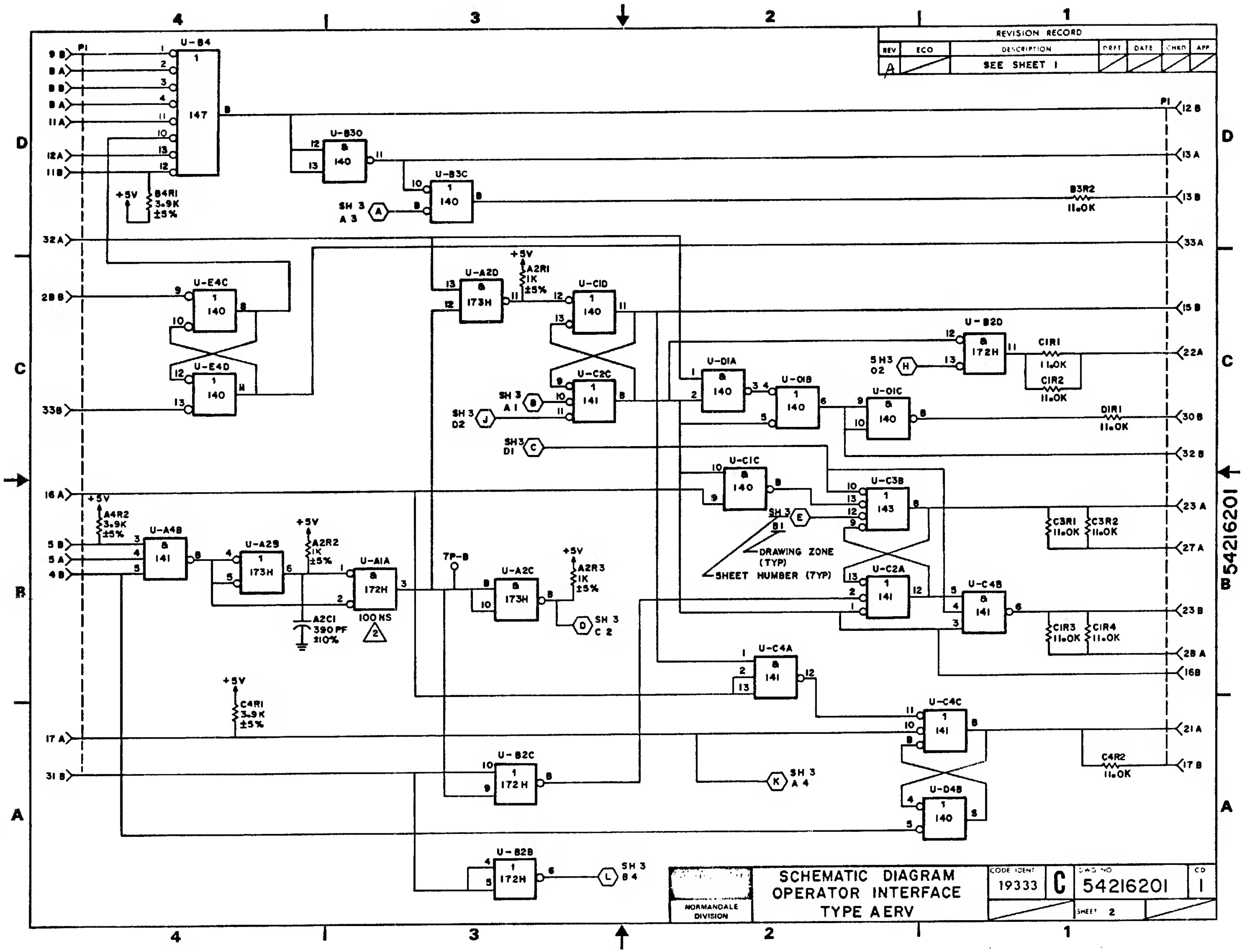
CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A1G	
DWN	D. G. TUTTLE	1-25-72
CHK		12-14-72
ENGR		12-14-72
MFG		
APPD		

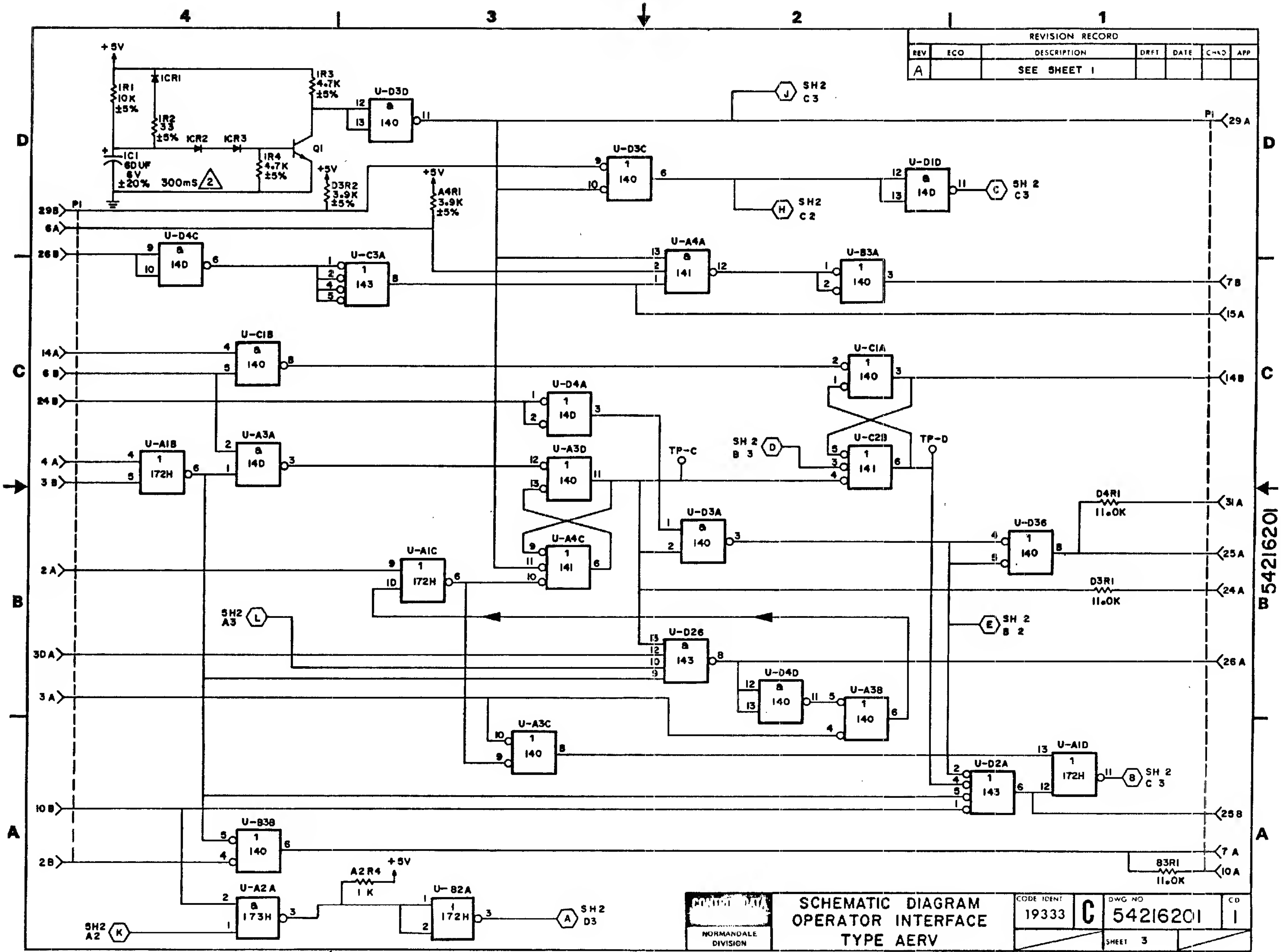
TITLE
SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE AERV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54216201	1

SHEET 1 OF 3


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
U-B4 147
U-B3D 140
U-B3C 140
U-E4C 140
U-E4D 140
U-A2D 173H
U-C1D 140
U-C2C 141
U-D1A 140
U-D1B 140
U-D1C 140
U-B2D 172H
U-C1C 140
U-C3B 143
U-C2A 141
U-C4B 141
U-C4A 141
U-C4C 141
U-D4B 140
U-A4B 141
U-A2B 173H
U-A1A 172H
U-A2C 173H
U-B2C 172H
U-B2B 172H
B4R1 3.9K ±5%
A2R1 1K ±5%
A4R2 3.9K ±5%
A2R2 1K ±5%
A2R3 1K ±5%
A2C1 390 PF ±10%
100 NS
C4R1 3.9K ±5%
B3R2 11.0K
C1R1 11.0K
C1R2 11.0K
D1R1 11.0K
C3R1 11.0K
C3R2 11.0K
C1R3 11.0K
C1R4 11.0K
C4R2 11.0K
DRAWING ZONE (TYP)
SHEET NUMBER (TYP)
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
OPERATOR INTERFACE
TYPE AERV
CODE IDENT 19333
C
DWG NO 54216201
CD 1
SHEET 2
54216201

70629100 F



NORMANDALE DIVISION

SCHEMATIC DIAGRAM
OPERATOR INTERFACE
TYPE AERV

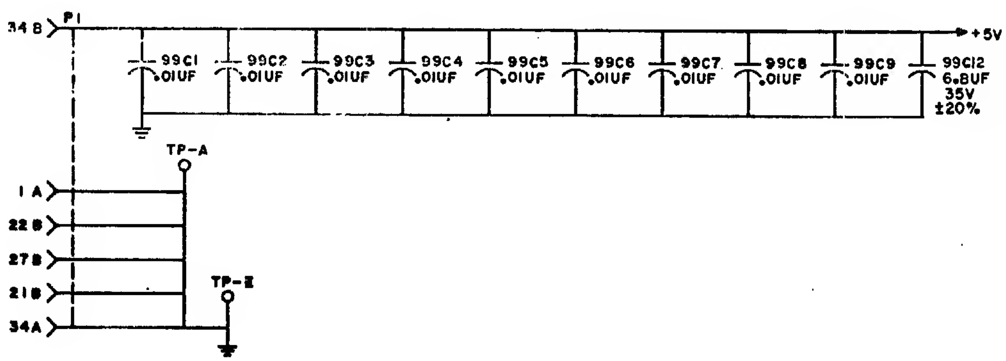
CODE IDENT		DWG NO	CD
19333	C	54216201	1
		SHEET 3	

54216201

4-60.1/4-60.2

70629100 F

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED		7-11-73		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N2221, 50210102.
   ALL DIODES, SILICON, 24553500.
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. DELAY TIMES FOR REF ONLY.

REFERENCE DRAWINGS			
COMP ASSY 54216102			
COMPONENTS EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3848	
DWN	V. WILSON	6-20-73
CHK		7/73
ENGR		
MFG		
APPR		

TITLE

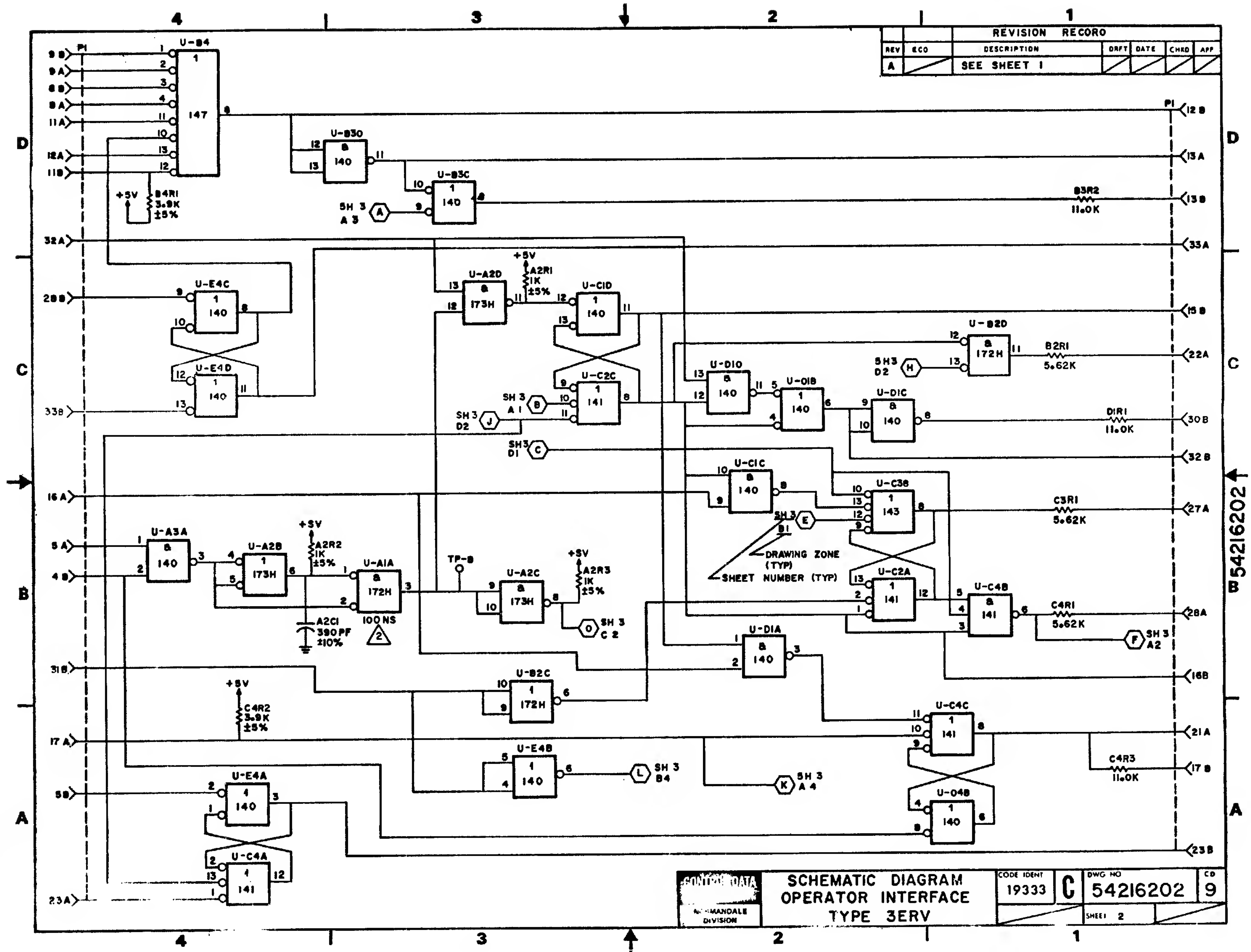
SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE 3ERV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54216202	9

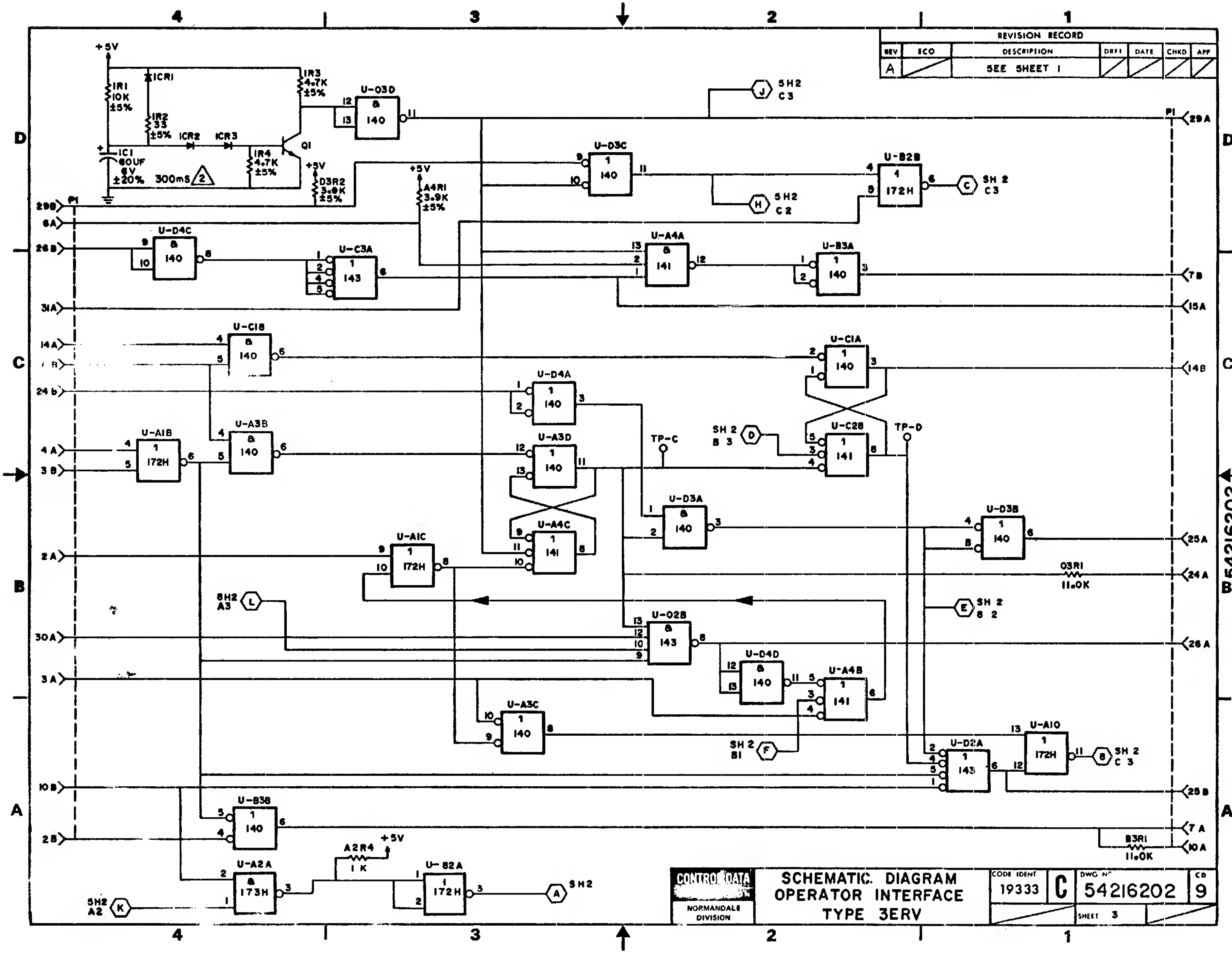
SHEET 1 OF 3

B54216202

4-60.4



70629100 F



REVISION RECORD

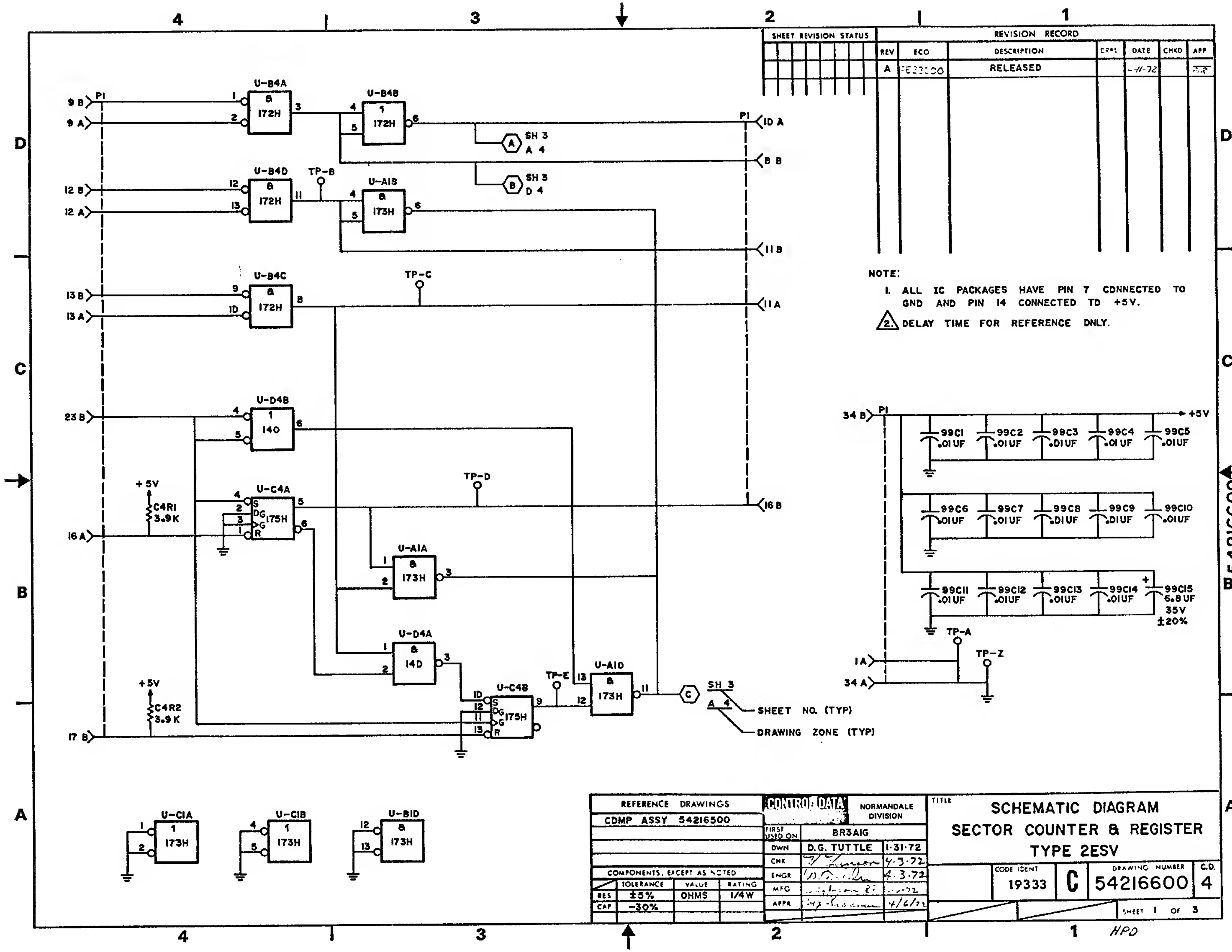
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
OPERATOR INTERFACE
TYPE 3ERV

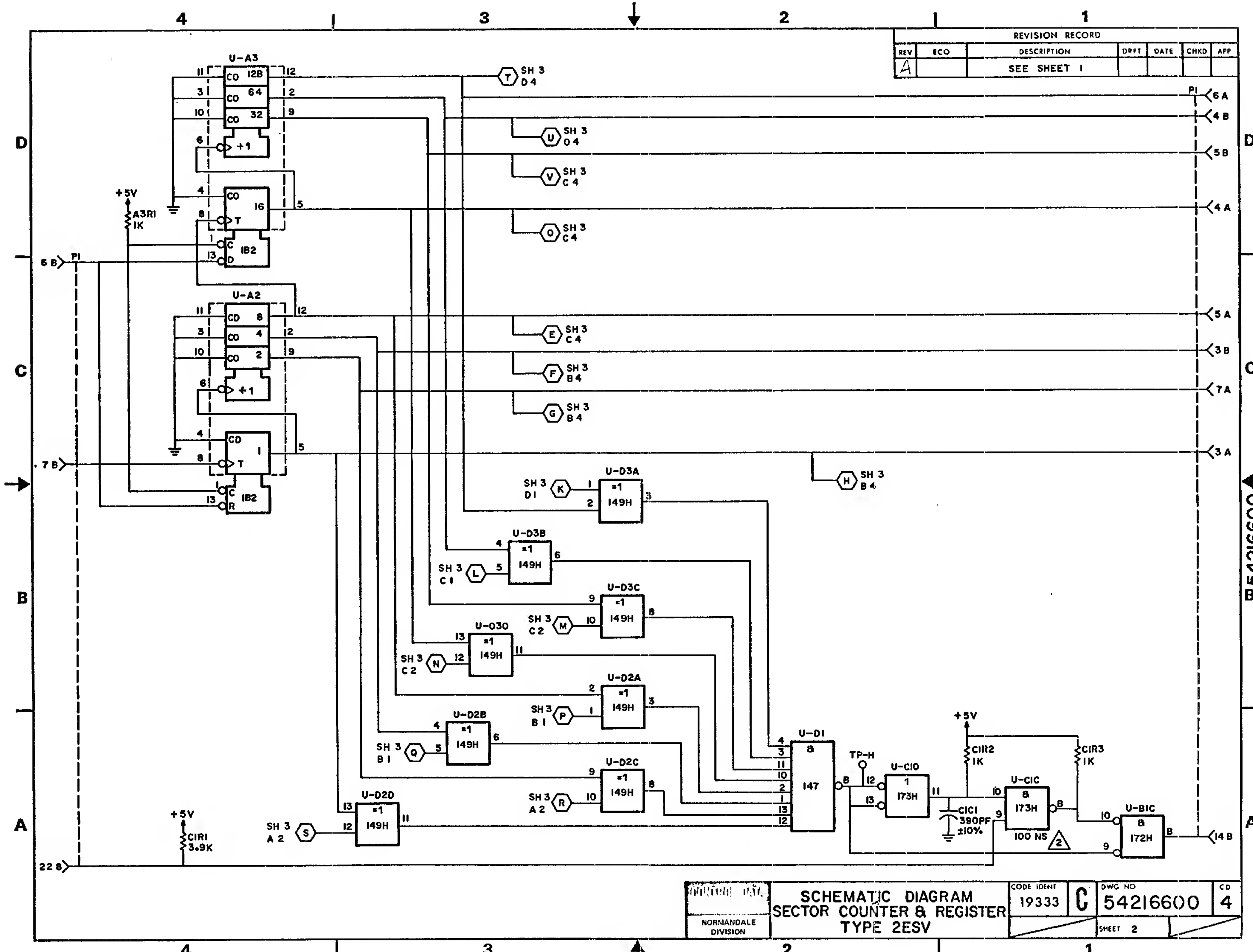
CODE IDENT 19333 C
DWG NO 54216202
CD 9
SHEET 3

54216202

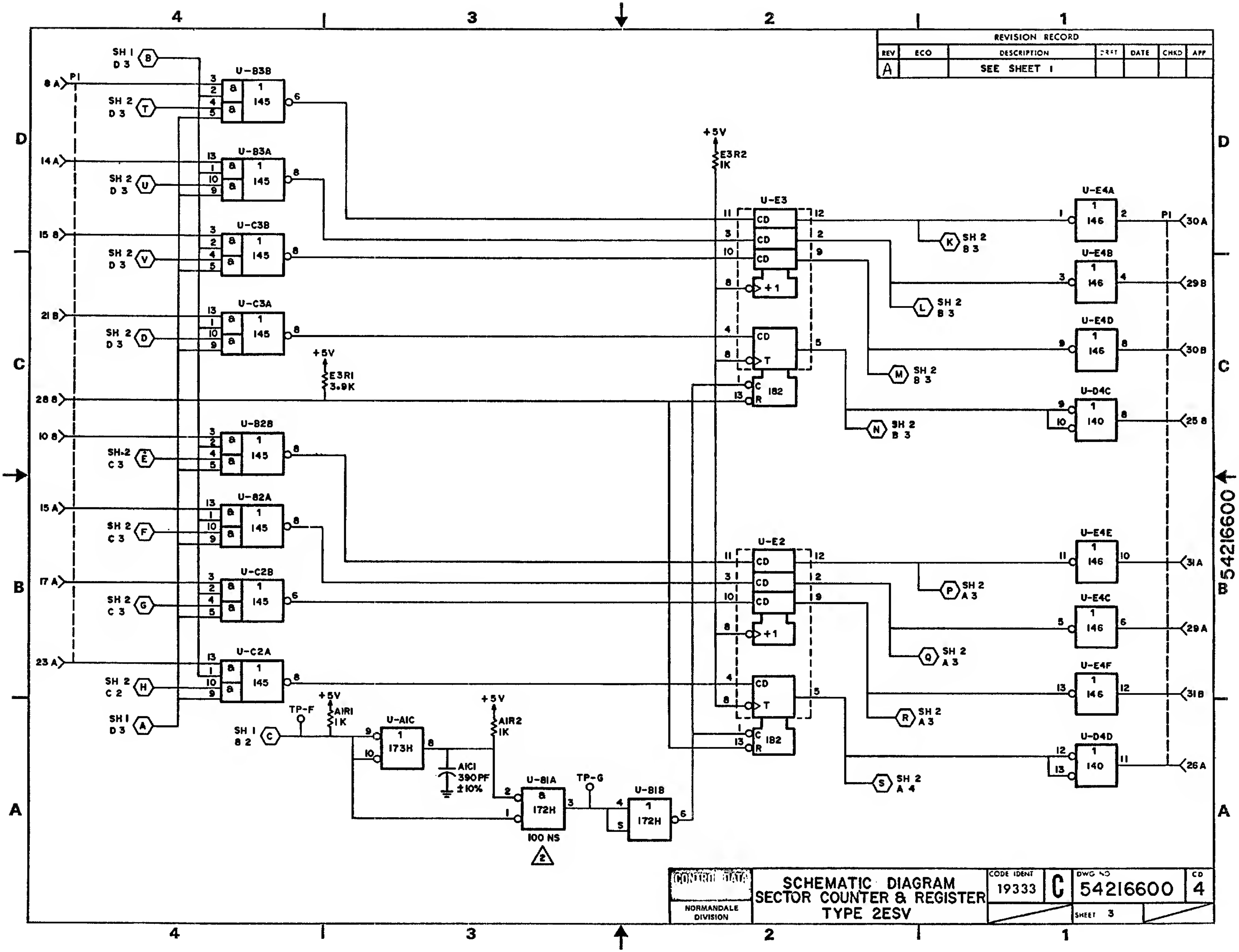

SHEET REVISION STATUS
REVISION RECORD
REV
ECO
DESCRIPTION
DATE
CHKD
APP
A
RELEASED
NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIME FOR REFERENCE ONLY.
U-B4A
172H
U-B4B
172H
U-B4D
172H
U-A1B
173H
U-B4C
172H
U-D4B
140
U-C4A
175H
U-A1A
173H
U-D4A
140
U-C4B
175H
U-A1D
173H
U-C1A
173H
U-C1B
173H
U-B1D
173H
TP-B
TP-C
TP-D
TP-E
TP-A
TP-Z
C4R1
3.9K
C4R2
3.9K
+5V
P1
9 B
9 A
12 B
12 A
13 B
13 A
23 B
16 A
17 B
10 A
8 B
11 B
11 A
16 B
34 B
1 A
34 A
SH 3
A 4
SH 3
D 4
SH 3
A 4
SHEET NO. (TYP)
DRAWING ZONE (TYP)
99C1
.01 UF
99C2
.01 UF
99C3
.01 UF
99C4
.01 UF
99C5
.01 UF
99C6
.01 UF
99C7
.01 UF
99C8
.01 UF
99C9
.01 UF
99C10
.01 UF
99C11
.01 UF
99C12
.01 UF
99C13
.01 UF
99C14
.01 UF
99C15
6.8 UF
35V
±20%
REFERENCE DRAWINGS
CDMP ASSY 54216500
COMPONENTS, EXCEPT AS NOTED
TOLERANCE
VALUE
RATING
RES
±5%
OHMS
1/4W
CAP
-30%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON
BR3AIG
DWN
D.G. TUTTLE
1-31-72
CHK
4-3-72
ENGR
4-3-72
MFG
APPR
4/6/72
TITLE
SCHEMATIC DIAGRAM
SECTOR COUNTER & REGISTER
TYPE 2ESV
CODE IDENT
19333
C
DRAWING NUMBER
54216600
C.D.
4
SHEET 1 OF 3
54216600
HPD

70629100 E

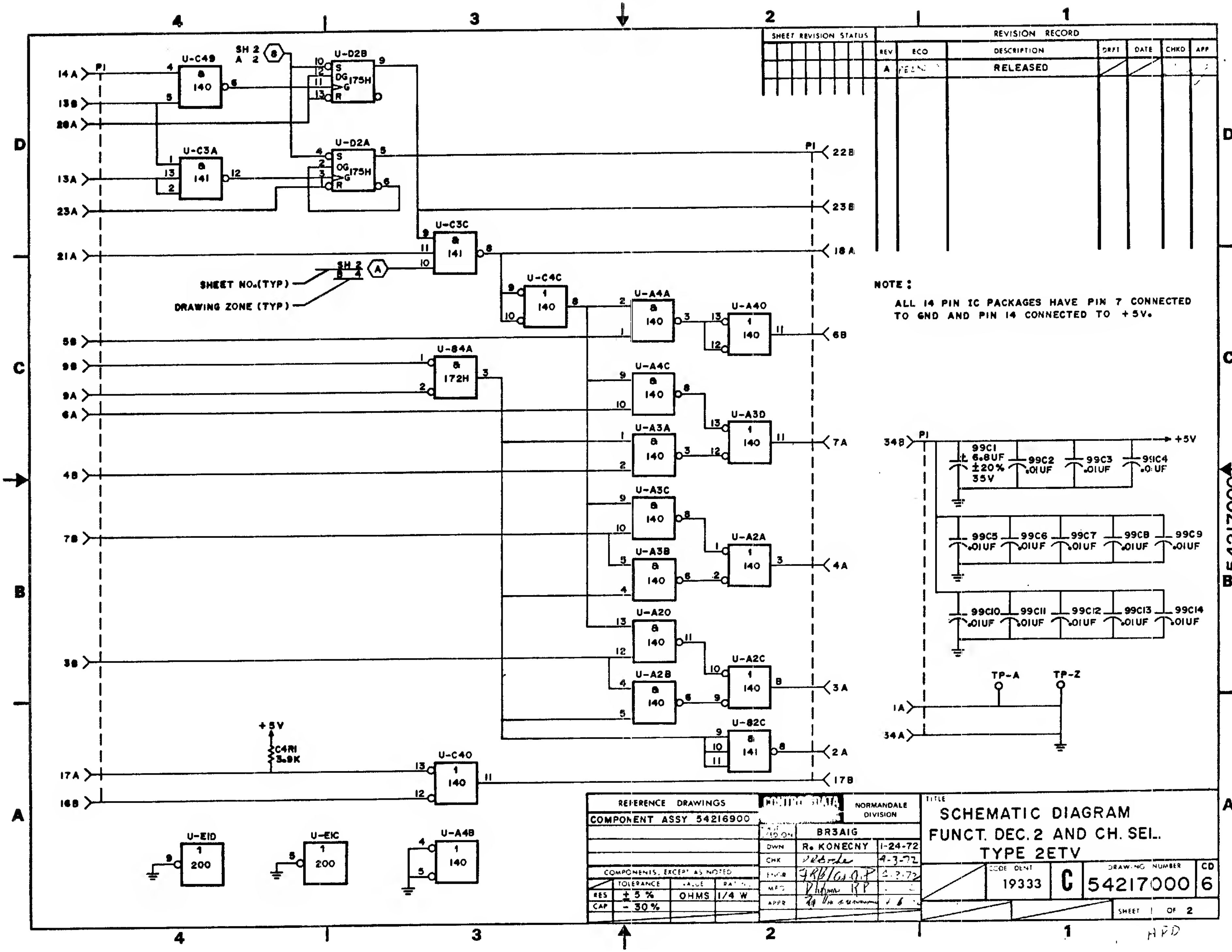
70629100 E

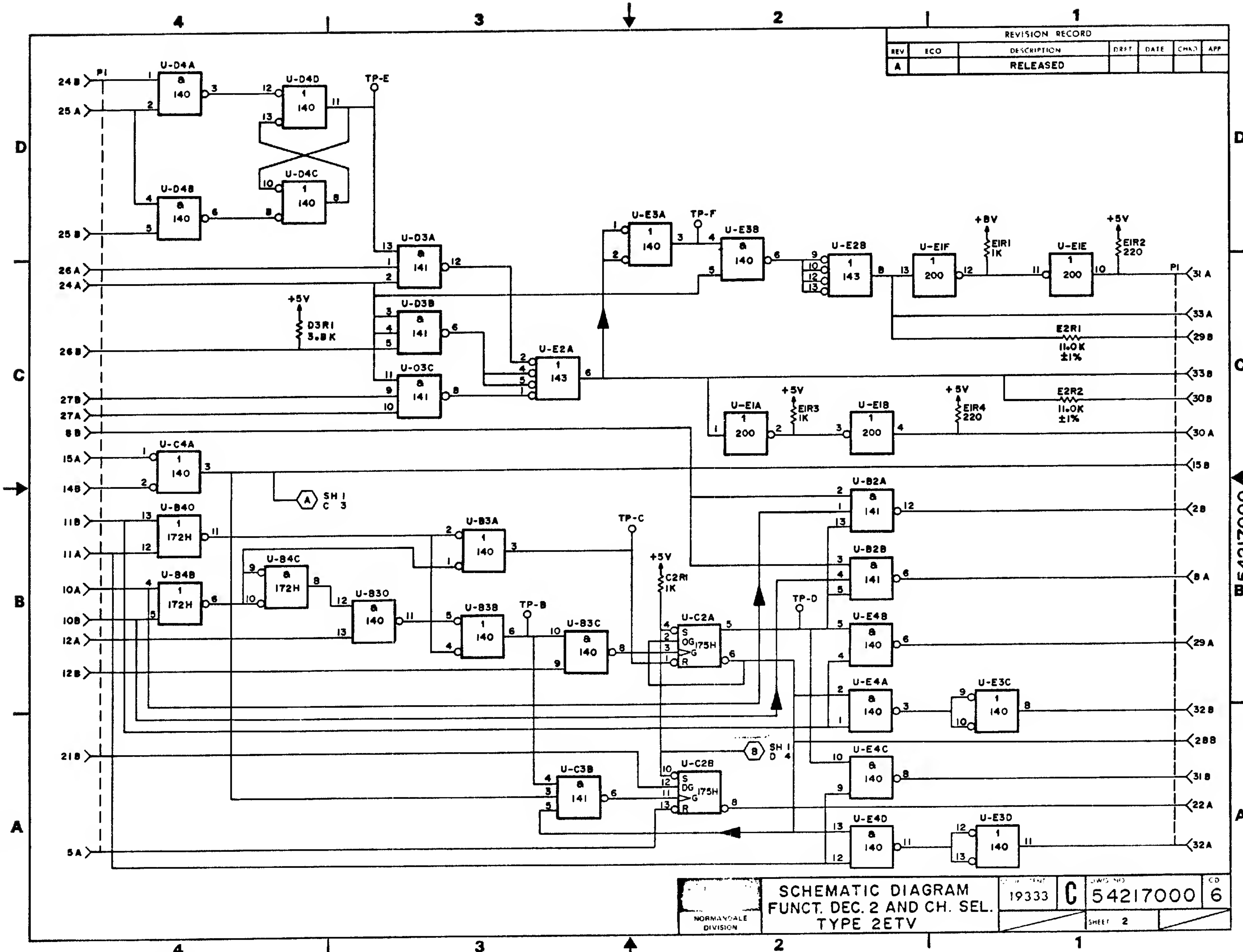


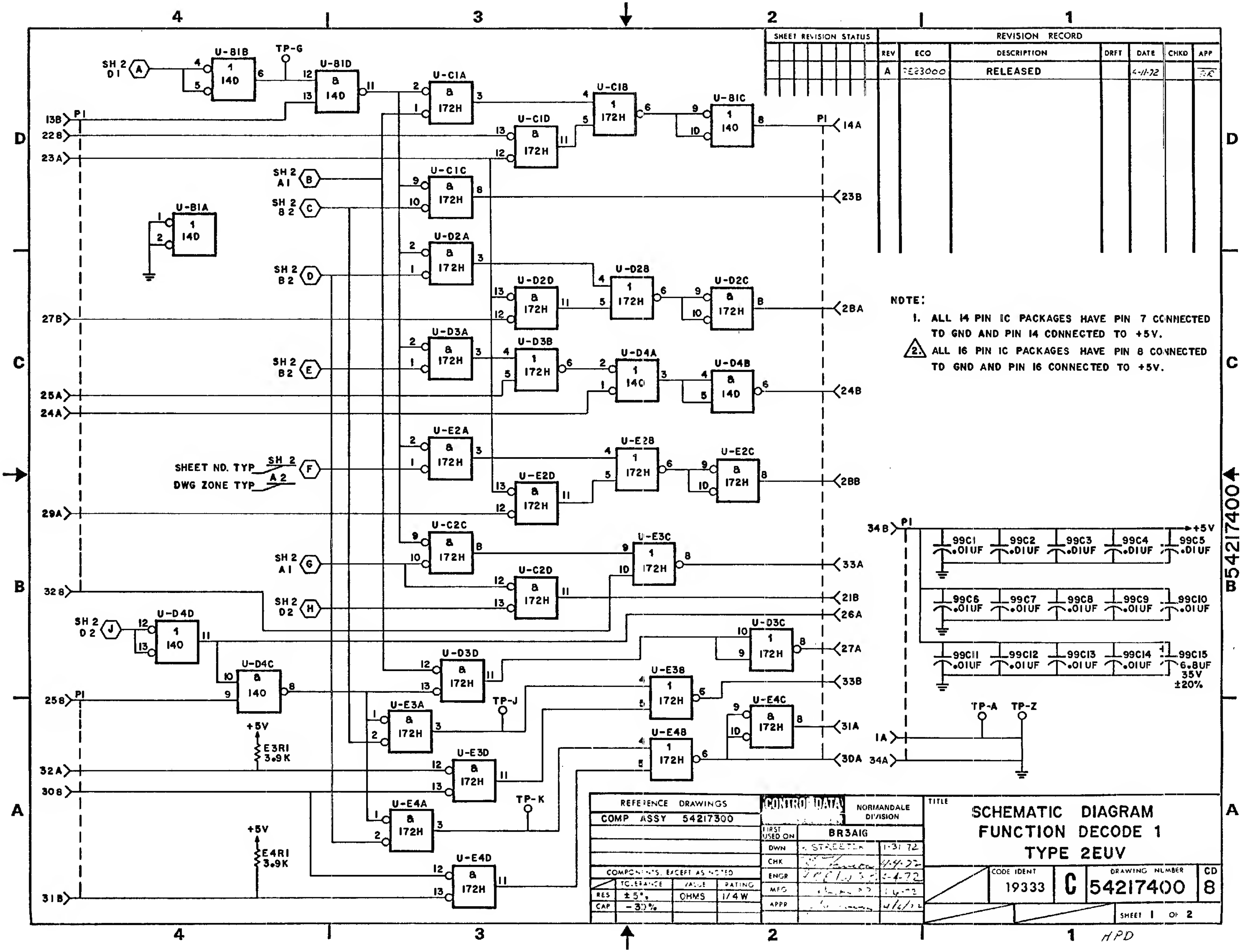
REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
A
SEE SHEET 1
U-A3
U-A2
U-D3A
U-D3B
U-D3C
U-D3D
U-D2A
U-D2B
U-D2C
U-D2D
U-D1
U-C1D
U-C1C
U-B1C
TP-H
A3R1 1K
C1R1 3.9K
C1R2 1K
C1R3 1K
C1C1 390PF ±10%
100 NS
+5V
SCHEMATIC DIAGRAM
SECTOR COUNTER & REGISTER
TYPE 2ESV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54216600
CD 4
SHEET 2
54216600


REVISION RECORD
REV A ECO DESCRIPTION SEE SHEET 1 DRFT DATE CHKD APP
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
SECTOR COUNTER & REGISTER
TYPE 2ESV
CODE IDENT 19333
C
DWG NO 54216600
CD 4
SHEET 3
54216600

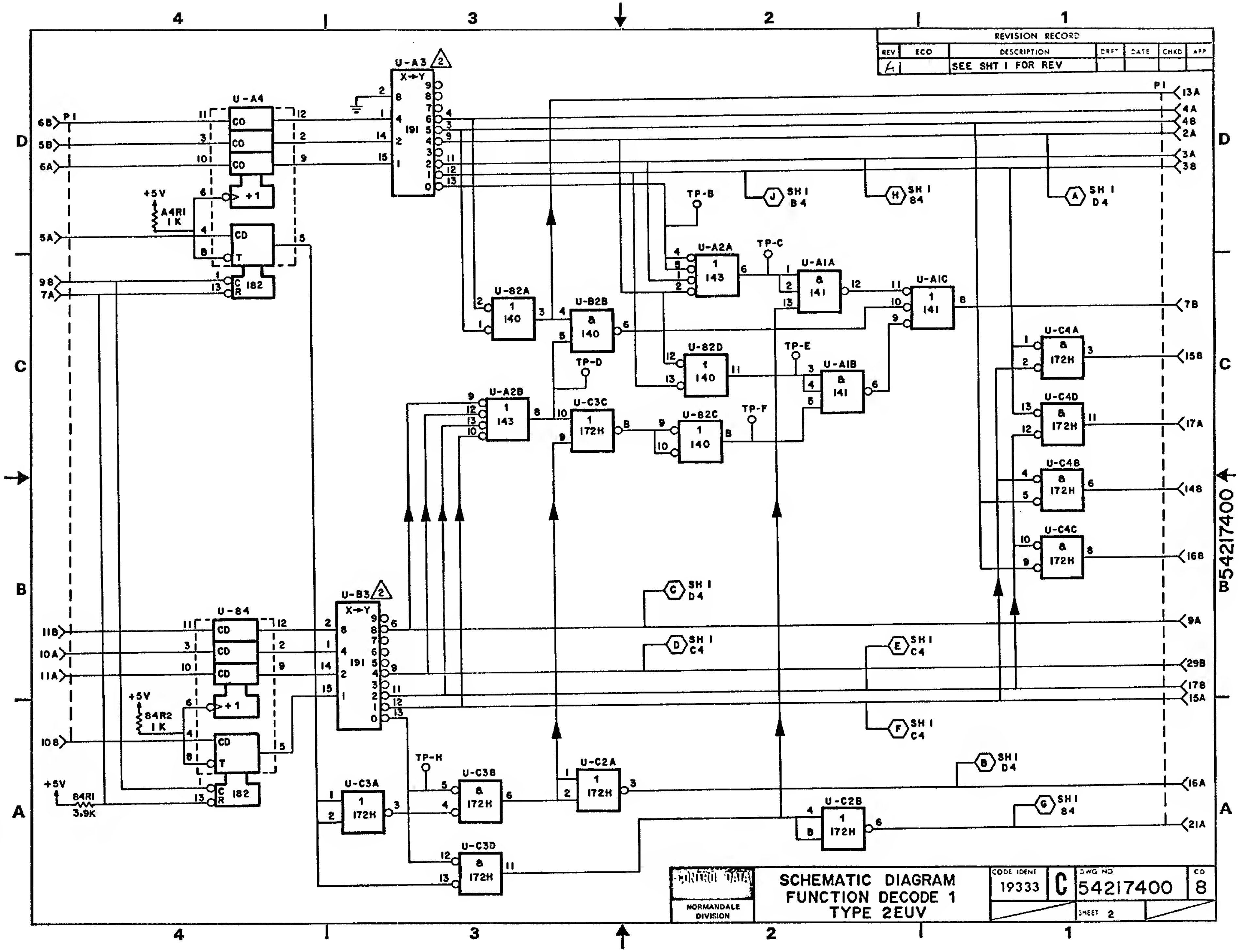
70629100 E

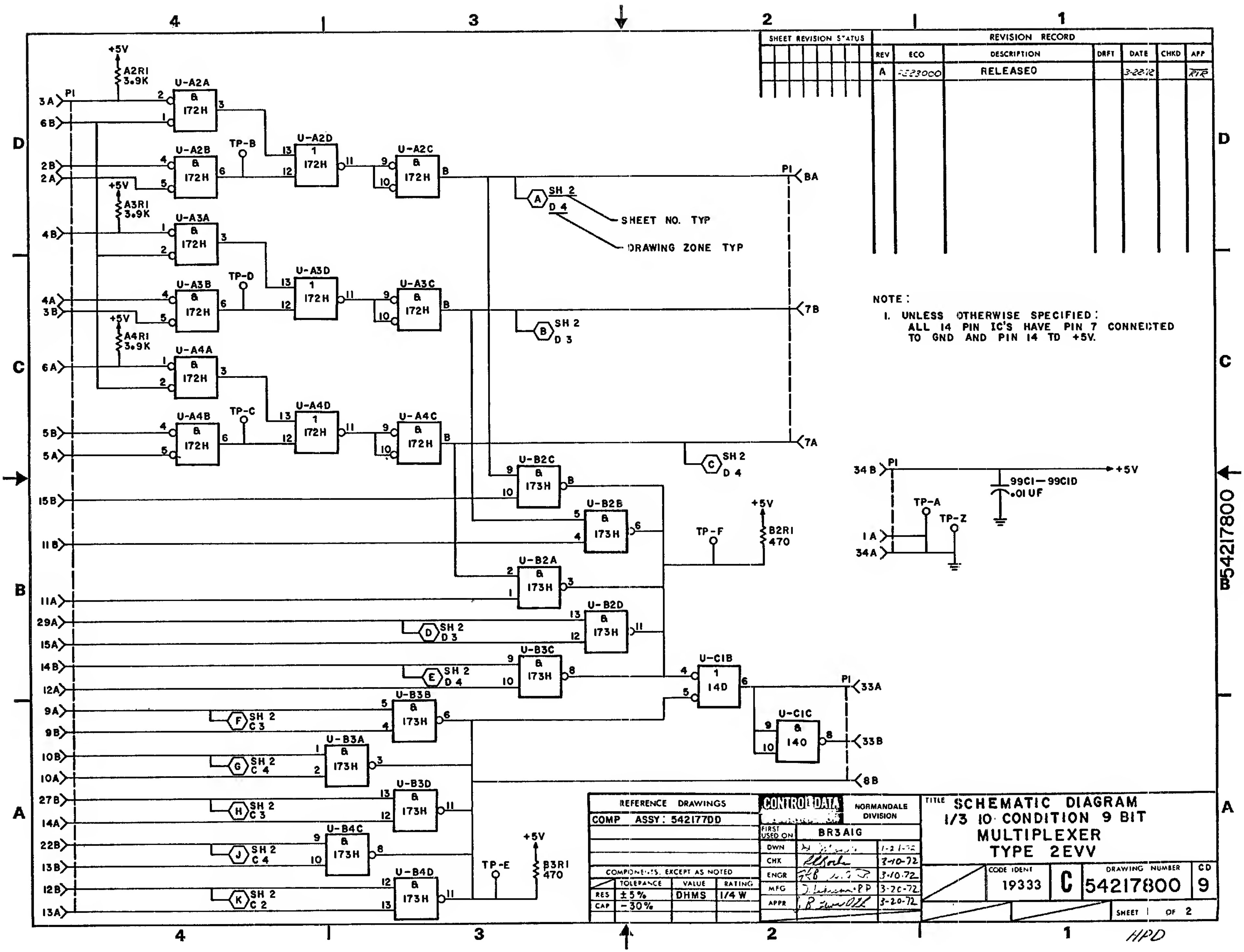

NOTE:
ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
SHEET NO. (TYP)
DRAWING ZONE (TYP)
REVISION RECORD
SHEET REVISION STATUS
REV
ECO
DESCRIPTION
A
RELEASED
REFERENCE DRAWINGS
COMPONENT ASSY 54216900
NORMANDALE DIVISION
BR3AIG
R. KONECNY
1-24-72
COMPONENTS, EXCEPT AS NOTED
TOLERANCE
RES ± 5 %
CAP - 30 %
OHMS
1/4 W
SCHEMATIC DIAGRAM
FUNCT. DEC. 2 AND CH. SEL.
TYPE 2ETV
19333
C
54217000
6
SHEET 1 OF 2
54217000

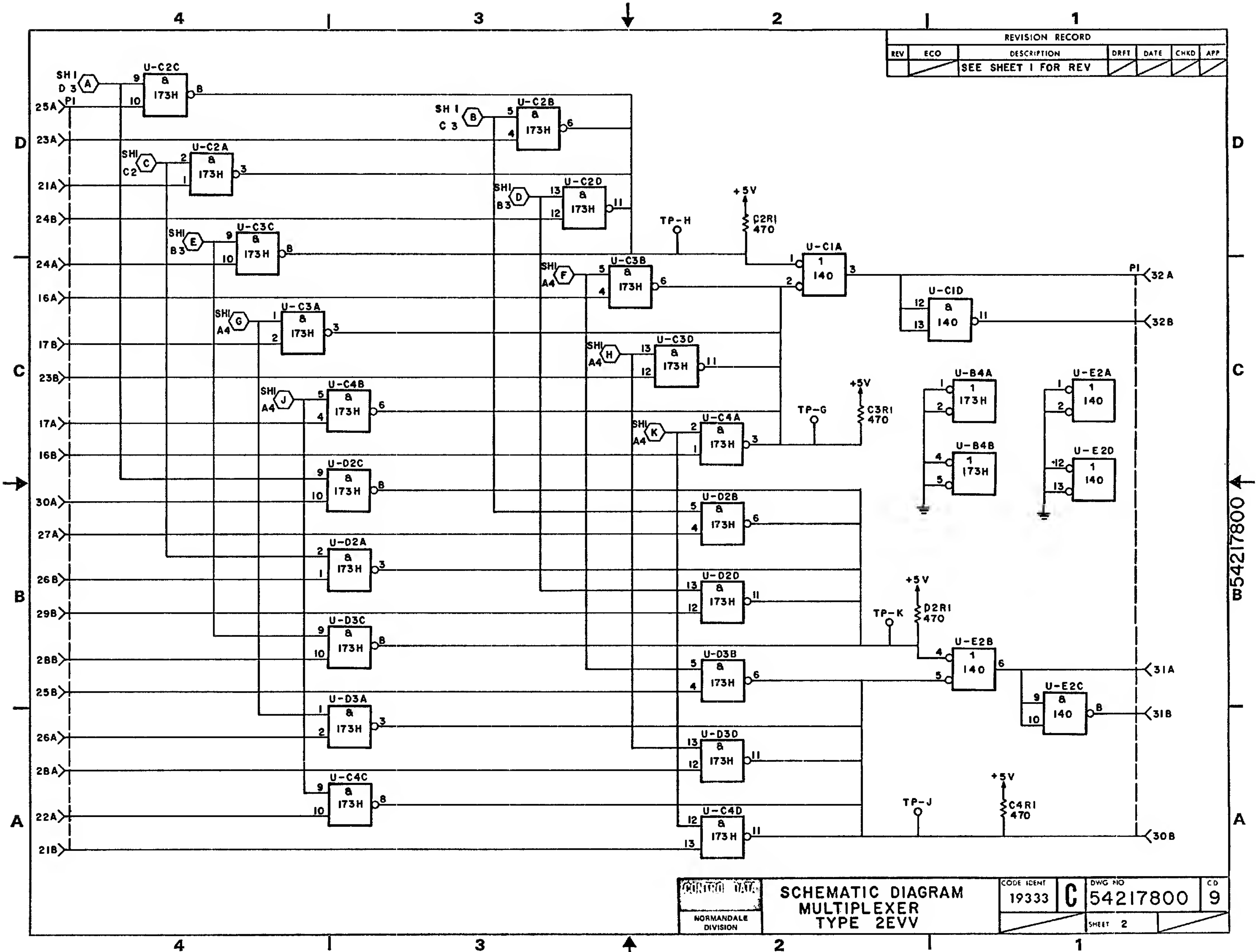

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | RELEASED
SCHEMATIC DIAGRAM
FUNCT. DEC. 2 AND CH. SEL.
TYPE 2ETV
NORMANDALE DIVISION
19333
C
54217000
6
SHEET 2
54217000
U-D4A
U-D4B
U-D4C
U-D4D
U-D3A
U-D3B
U-D3C
U-E2A
U-E3A
U-E3B
U-E2B
U-E1F
U-E1E
U-E1A
U-E1B
U-C4A
U-B4D
U-B4C
U-B4B
U-B3A
U-B3D
U-B3B
U-B3C
U-C2A
U-C2B
U-C3B
U-B2A
U-B2B
U-E4B
U-E4A
U-E3C
U-E4C
U-E4D
U-E3D
TP-E
TP-F
TP-C
TP-B
TP-D
D3R1 3.8K
E1R1 1K
E1R2 220
E2R1 11.0K ±1%
E2R2 11.0K ±1%
E1R3 1K
E1R4 220
C2R1 1K
+5V
P1
SH 1 C 3
SH 1 D 4



SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | FE23000 | RELEASED | | 4-11-72 | |
NOTE:
1. ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
SHEET NO. TYP
DWG ZONE TYP
REFERENCE DRAWINGS
COMP ASSY 54217300
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3AIG
DWN
CHK
ENGR
MFG
APPR
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% OHMS 1/4 W
CAP -30%
TITLE
SCHEMATIC DIAGRAM
FUNCTION DECODE 1
TYPE 2EUV
CODE IDENT 19333
C
DRAWING NUMBER 54217400
CD 8
SHEET 1 OF 2
54217400
HPD

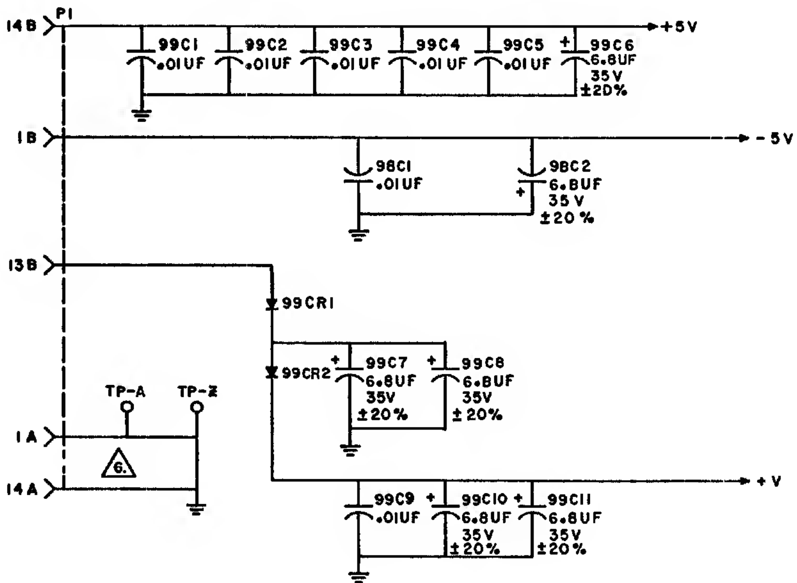

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | | SEE SHT 1 FOR REV
U-A3
U-A4
U-B4
U-B3
U-A2A
U-A2B
U-A1A
U-A1B
U-A1C
U-B2A
U-B2B
U-B2C
U-B2D
U-C3A
U-C3B
U-C3C
U-C3D
U-C2A
U-C2B
U-C4A
U-C4B
U-C4C
U-C4D
TP-B
TP-C
TP-D
TP-E
TP-F
TP-H
+5V
A4R1 1K
B4R2 1K
B4R1 3.9K
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FUNCTION DECODE 1
TYPE 2EUV
CODE IDENT 19333
C
DWG NO 54217400
CD 8
SHEET 2


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | RELEASED | 3-22-72
NOTE:
1. UNLESS OTHERWISE SPECIFIED: ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
SHEET NO. TYP
DRAWING ZONE TYP
99C1—99C1D .01 UF
REFERENCE DRAWINGS
COMP ASSY: 542177DD
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3A1G
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% OHMS 1/4 W
CAP -30%
DWN 1-21-72
CHK 3-10-72
ENGR 3-10-72
MFG 3-20-72
APPR 3-20-72
TITLE SCHEMATIC DIAGRAM
1/3 IO CONDITION 9 BIT
MULTIPLEXER
TYPE 2EVV
CODE IDENT 19333
C
DRAWING NUMBER 54217800
CD 9
SHEET 1 OF 2
HPD
54217800


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SEE SHEET 1 FOR REV
U-C2C 173H
U-C2B 173H
U-C2A 173H
U-C2D 173H
U-C3C 173H
U-C3B 173H
U-C3A 173H
U-C3D 173H
U-C4B 173H
U-C4A 173H
U-D2C 173H
U-D2B 173H
U-D2A 173H
U-D2D 173H
U-D3C 173H
U-D3B 173H
U-D3A 173H
U-D3D 173H
U-C4C 173H
U-C4D 173H
U-C1A 140
U-C1D 140
U-B4A 173H
U-B4B 173H
U-E2A 140
U-E2D 140
U-E2B 140
U-E2C 140
TP-H
TP-G
TP-K
TP-J
+5V
C2R1 470
C3R1 470
D2R1 470
C4R1 470
25A 23A 21A 24B 24A 16A 17B 23B 17A 16B 30A 27A 26B 29B 28B 25B 26A 28A 22A 21B
32A 32B 31A 31B 30B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
MULTIPLEXER
TYPE 2EVV
CODE IDENT 19333
C
DWG NO 54217800
CD 9
SHEET 2

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED		[illegible]		[illegible]
	B	PE 30523	INCREASE YIELD	[illegible]	[illegible]	[illegible]	[illegible]



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL DIODES, SILICON, 24553500
   ALL ZENER DIODE VOLTAGE TOL. ±5%
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V
2. COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
3. IC, TYPE 579, HAS PIN 8 CONNECTED TO GND; PIN 16 TO +V.
4. IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.
5. DELAY TIME FOR REFERENCE ONLY.
6. ALL UNUSED PINS ARE GROUNDED.
   PIN 2B IS A SPARE.
7. IC, TYPE 193, HAS PIN 8 CONNECTED TO GND; PIN 16 TO +5V.

5422I000

REFERENCE DRAWINGS
COMP ASSY: 5422D900

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

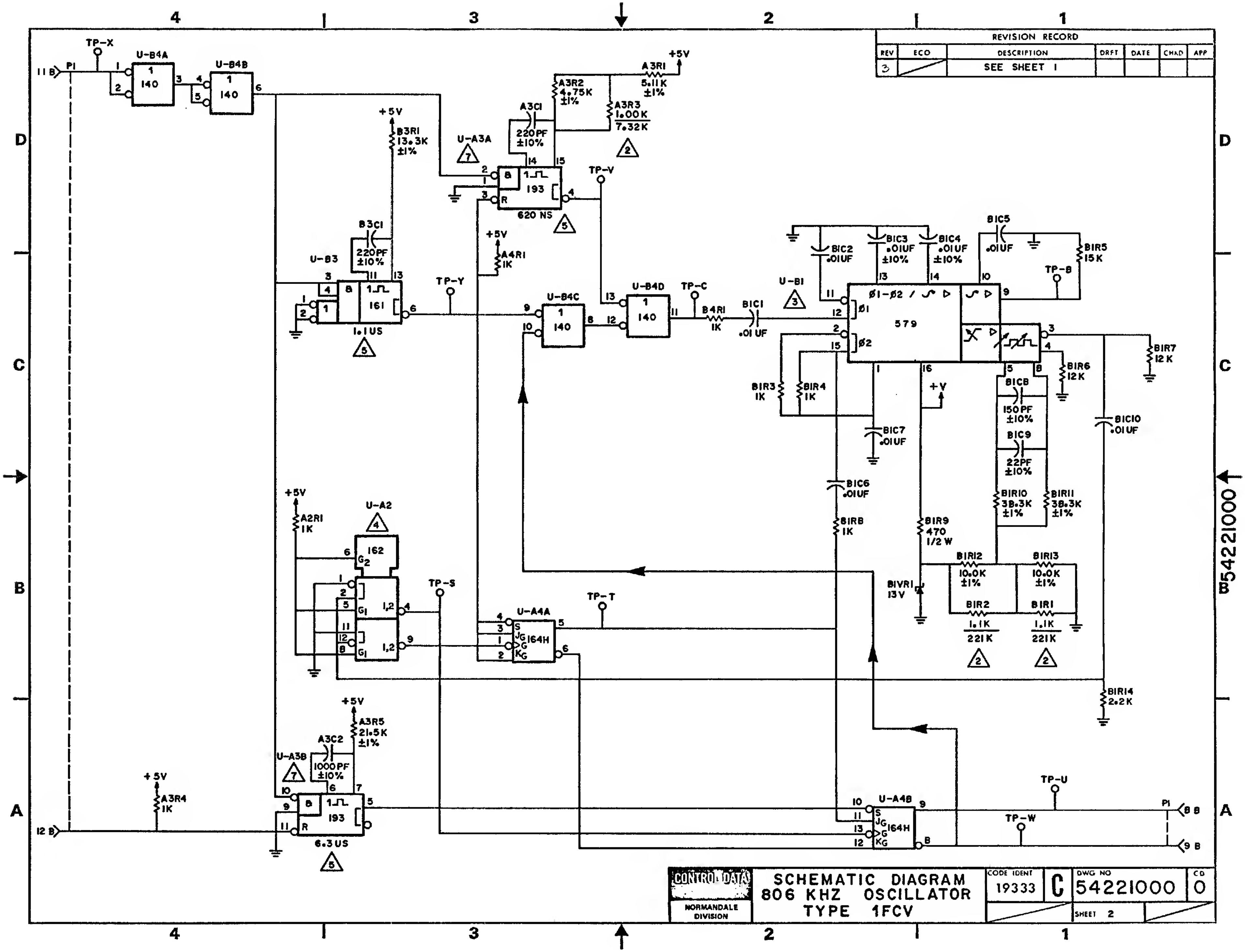
FIRST USED ON	BR3A3	
DWN	[illegible]	[illegible]-71
CHK	[illegible]	12-27-71
ENGR	[illegible]	
MFG	[illegible]	[illegible]-71
APPR	[illegible]	[illegible]-72

TITLE SCHEMATIC DIAGRAM 806 KHZ OSCILLATOR TYPE 1FCV

CODE IDENT 19333 | C | DRAWING NUMBER 5422I000 | CD 0

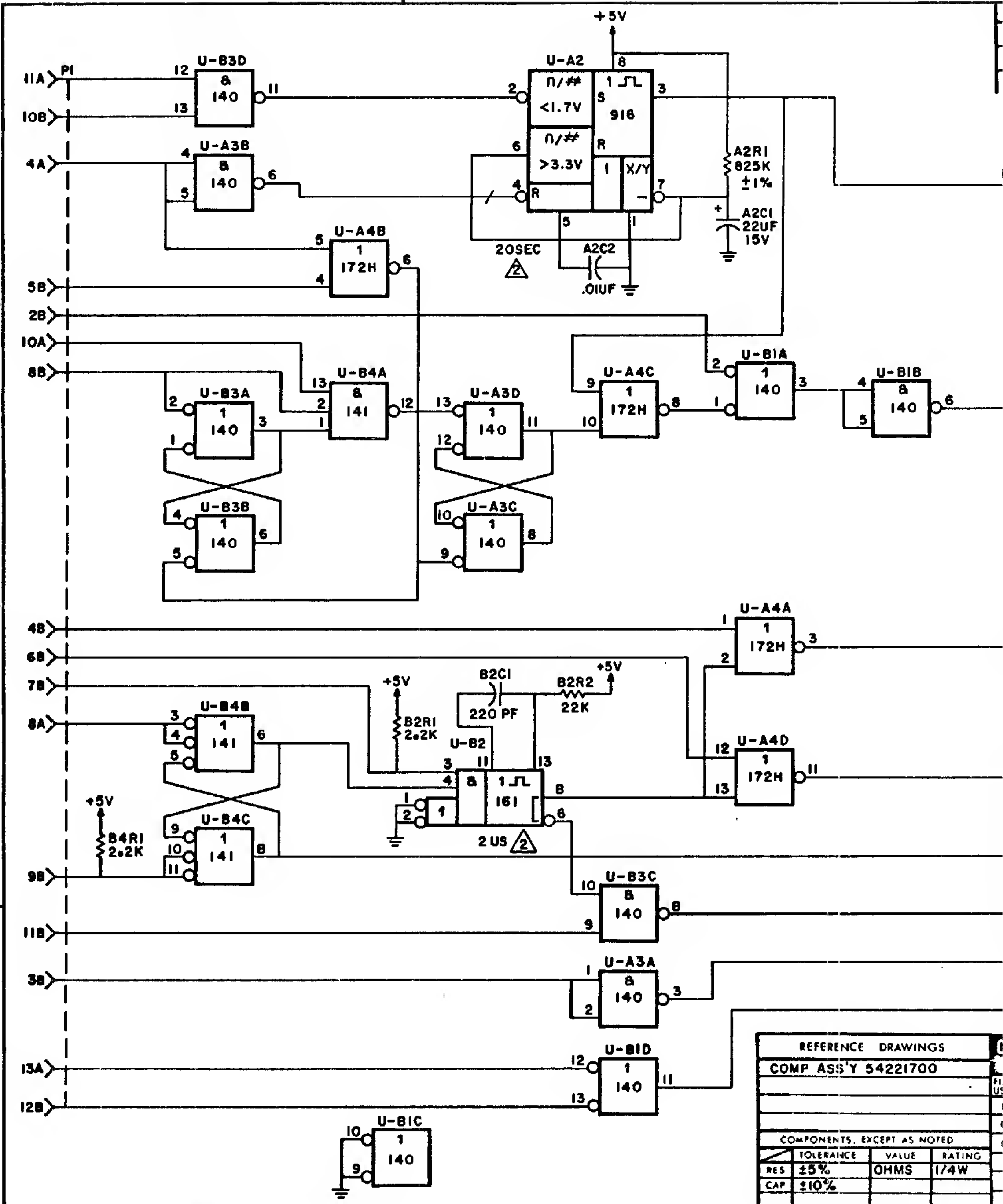
SHEET 1 OF 2

HPD


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
3 SEE SHEET 1
U-B4A
U-B4B
U-B3
U-A3A
U-B4C
U-B4D
U-B1
579
U-A2
162
U-A4A
164H
U-A3B
193
6.3 US
U-A4B
620 NS
1.1 US
TP-X
TP-Y
TP-V
TP-C
TP-B
TP-S
TP-T
TP-U
TP-W
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
806 KHZ OSCILLATOR
TYPE 1FCV
CODE IDENT 19333
C
DWG NO 54221000
CD 0
SHEET 2
54221000

70629100 E

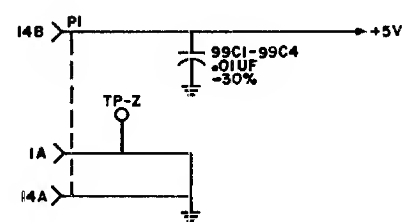
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				
B	PE35028	RESISTOR VALUE CHANGE	RB	2-22-73		INR
C	PE35118	CHG 916 ELEMENT SYMBOL	VW	4-24-73		



NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMP ASS'Y 54221700

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	±10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR302	
DWN	S. ZAK	10-23-72
CHK		
ENGR		
MFG		11-1-72
APPR		11-1-72

TITLE

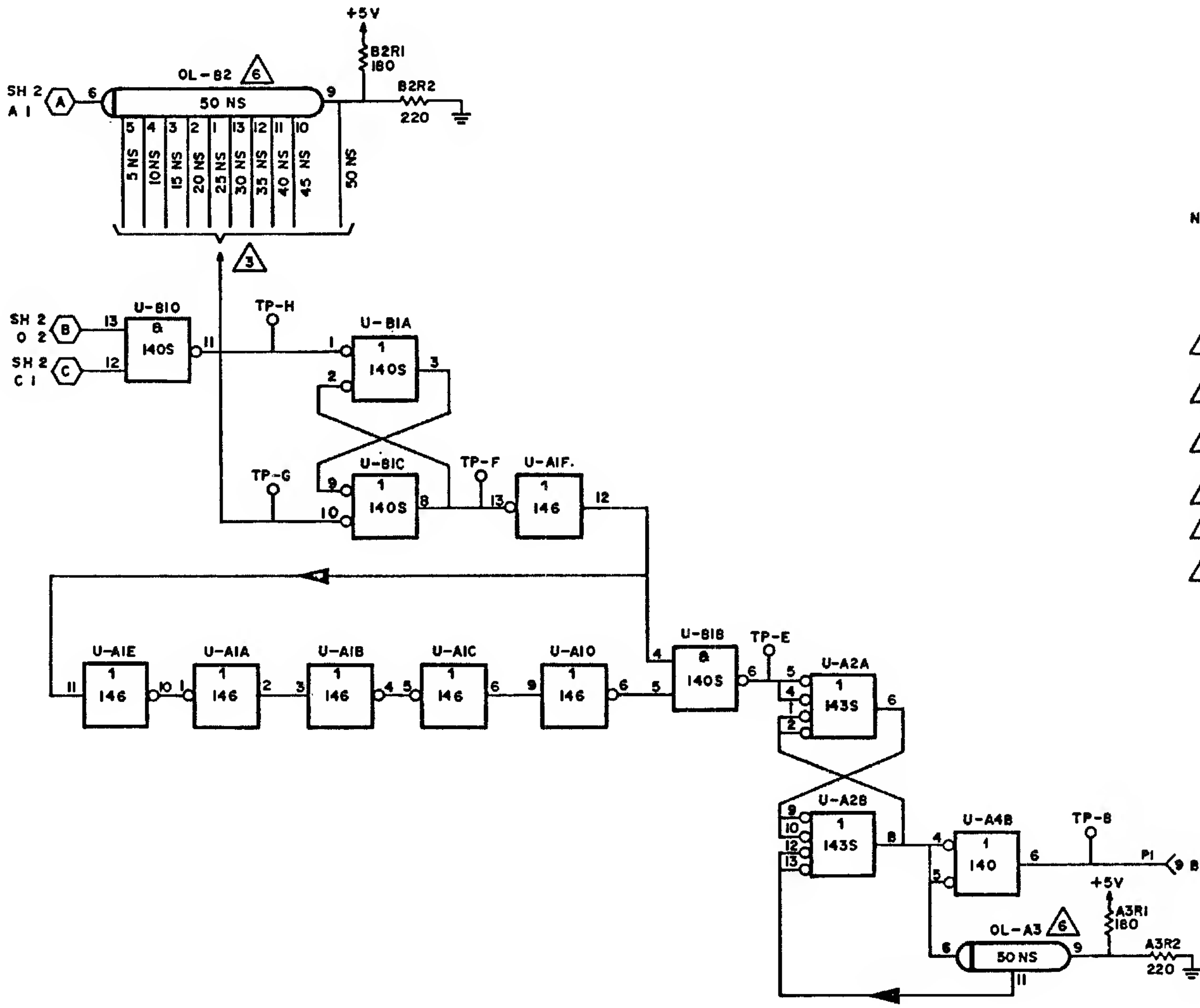
SCHEMATIC DIAGRAM MOTOR ENABLE & ON LINE CLEAR TYPE 2FEV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54221800	3

SHEET 1 OF 1

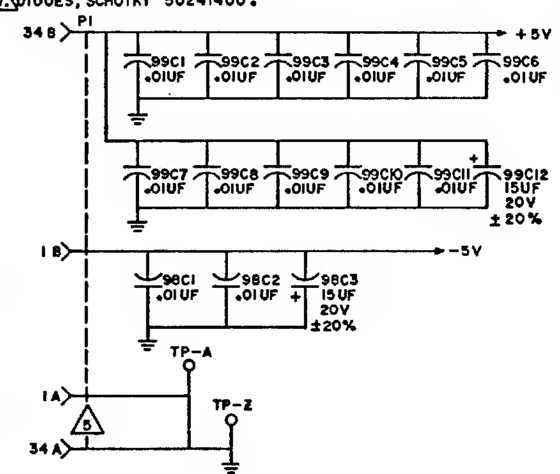
B54221800

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED		5-11-72		[illegible]



NOTE:

1. UNLESS OTERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL TRANSISTORS, SILICON, NPN, 2N3646, 50210310.
   ALL DIODES 24553500.
2. IC PACKAGES U-D3 AND U-E3 HAVE PIN 13 CONNECTED TO -5V.
3. DELAY TAPS ARE EVERY 5.00 NS ± 10% DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
4. DELAY TAPS ARE EVERY 15.00 NS ± 10% DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
5. CONNECTOR PINS 1A THRU 34A ARE GROUNDED.
6. DELAY LINES B2, B3, AND A3 HAVE PINS 7 AND 8 CONNECTED TO GND.
7. DIODES, SCHOTKY 50241400.



54223402

REFERENCE DRAWINGS
COMP ASSY 54223302

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		
IND	±10%		

NORMANDALE DIVISION

FIRST USED ON: BR3A1

DWN	O.G. TUTTLE	5-10-72
CHK	[illegible]	5-[illegible]-72
ENGR	[illegible]	[illegible]
MFG	[illegible]	5-[illegible]-72
APPR	[illegible]	5-[illegible]

TITLE: SCHEMATIC DIAGRAM DATA LATCH TYPE AFJV

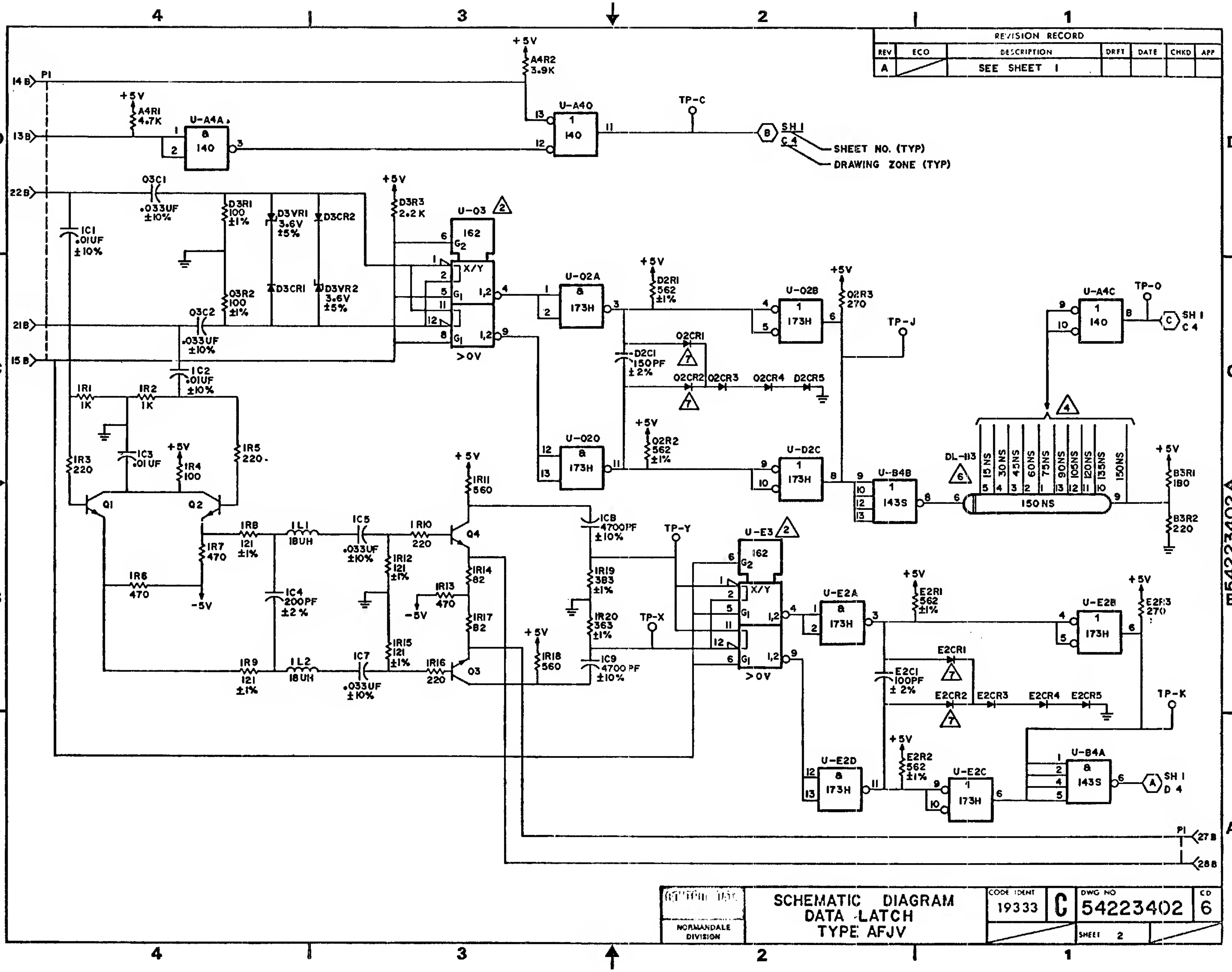
CODE IDENT 19333 | C | DRAWING NUMBER 54223402 | C.D. 6

SHEET 1 OF 2

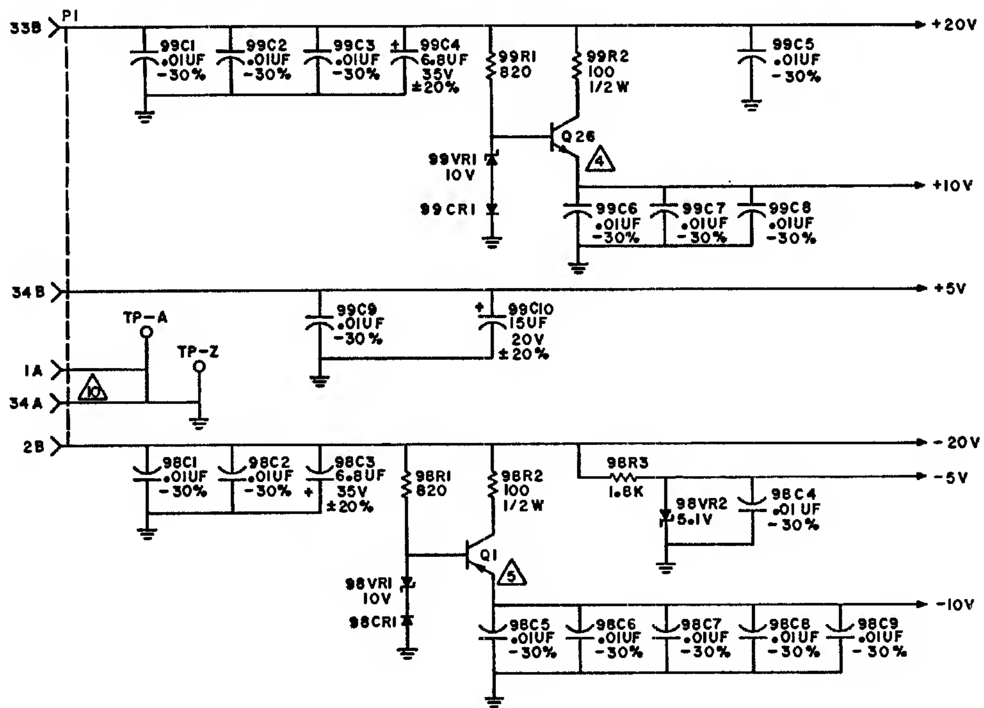
HPD

70629100 E

70629100 E


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | | SEE SHEET 1
SHEET NO. (TYP)
DRAWING ZONE (TYP)
U-A4A
U-A4D
U-A4C
U-D3
U-D2A
U-D2B
U-D2C
U-D2D
U-B4B
U-E3
U-E2A
U-E2B
U-E2C
U-E2D
U-B4A
DL-113
150NS
TP-C
TP-D
TP-J
TP-Y
TP-X
TP-K
SCHEMATIC DIAGRAM
DATA LATCH
TYPE AFJV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54223402
CD 6
SHEET 2
54223402

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23...	RELEASED		2-17-71		RH



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4916, 50211610
   ALL DIODES, SILICON, 92115023
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%

2. TRANSISTOR, SNPN, 2N2221, 50210102.
3. TRANSISTOR, ARRAY, QUAD, CA3018, 50251100.
4. TRANSISTOR, SNPN, 2N3569, 50210811.
5. TRANSISTOR, SPNP, 2N3638, 50210610.
6. TRANSISTOR, SNPN, 2N3646, 50210310.
7. TRANSISTOR, SPNP, 2N4258, 50211510.
8. TRANSISTOR, SPNP, 2N5230, 50212200.
9. DIODE, SILICON, 92115021.
10. PINS 1A THRU 34A ARE CONNECTED TO GND.
11. IC, TYPE 308, HAS PIN 7 CONNECTED TO +10V AND PIN 4 CONNECTED TO -10V.
12. PIN 10 OF U-12 AND U-14 CONNECTED TO GND.
13. PIN 10 OF U-2, U-19 AND U-25 CONNECTED TO -10V.

REFERENCE DRAWINGS		
COMP ASSY: 54224100		
COMPONENTS, EXCEPT AS NOTED		
TOLERANCE	VALUE	RATING
RES ±5%	OHMS	1/4 W
CAP ±10%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR3A1	
DWN		2-3-71
CHK		12-15-71
ENGR		2-15-71
MFG		12-16-71
APPR		12-16-71

TITLE
SCHEMATIC DIAGRAM ACG AMPLIFIER TYPE 1FLV

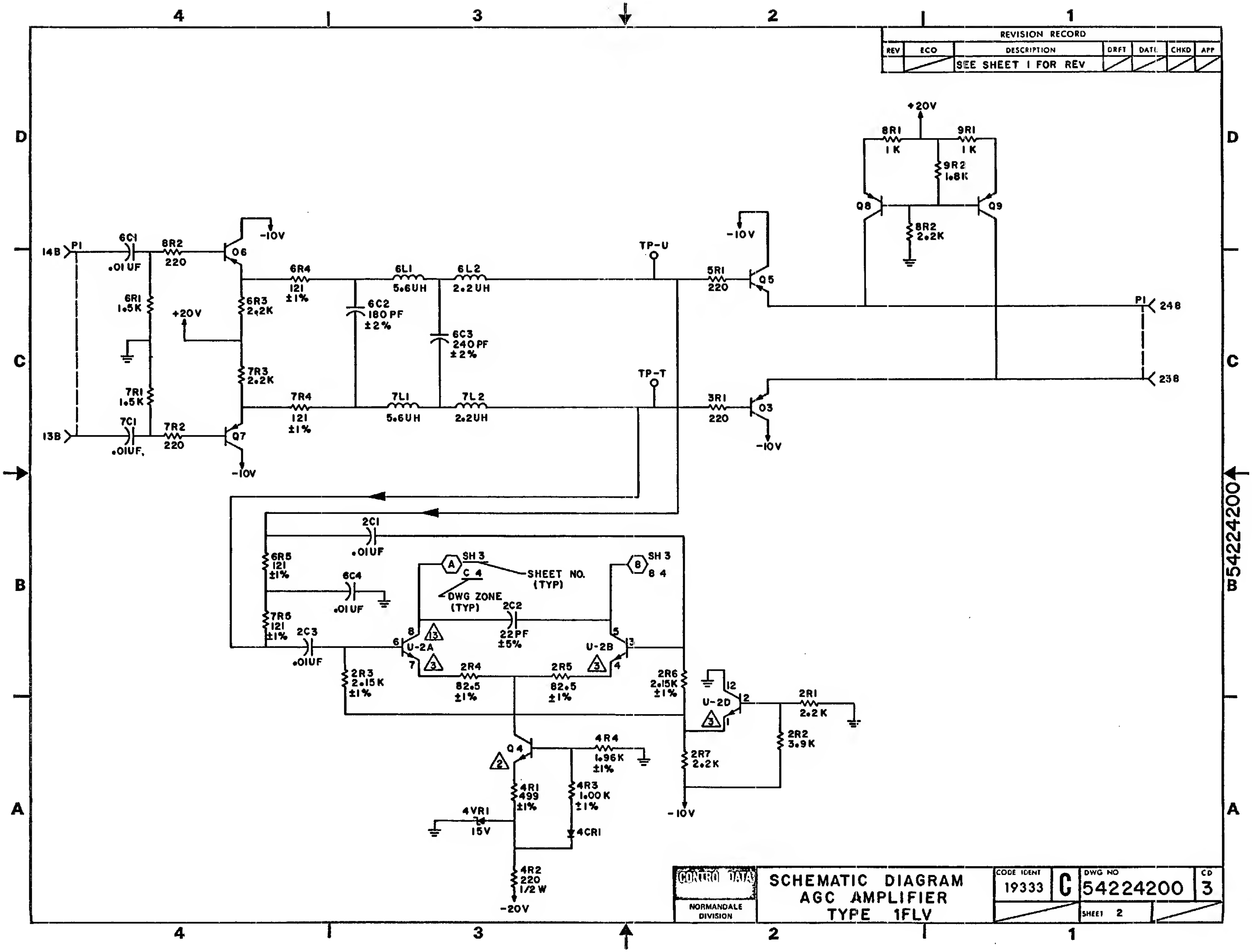
CODE IDENT		DRAWING NUMBER	CD
19333	C	54224200	3

SHEET 1 OF 3

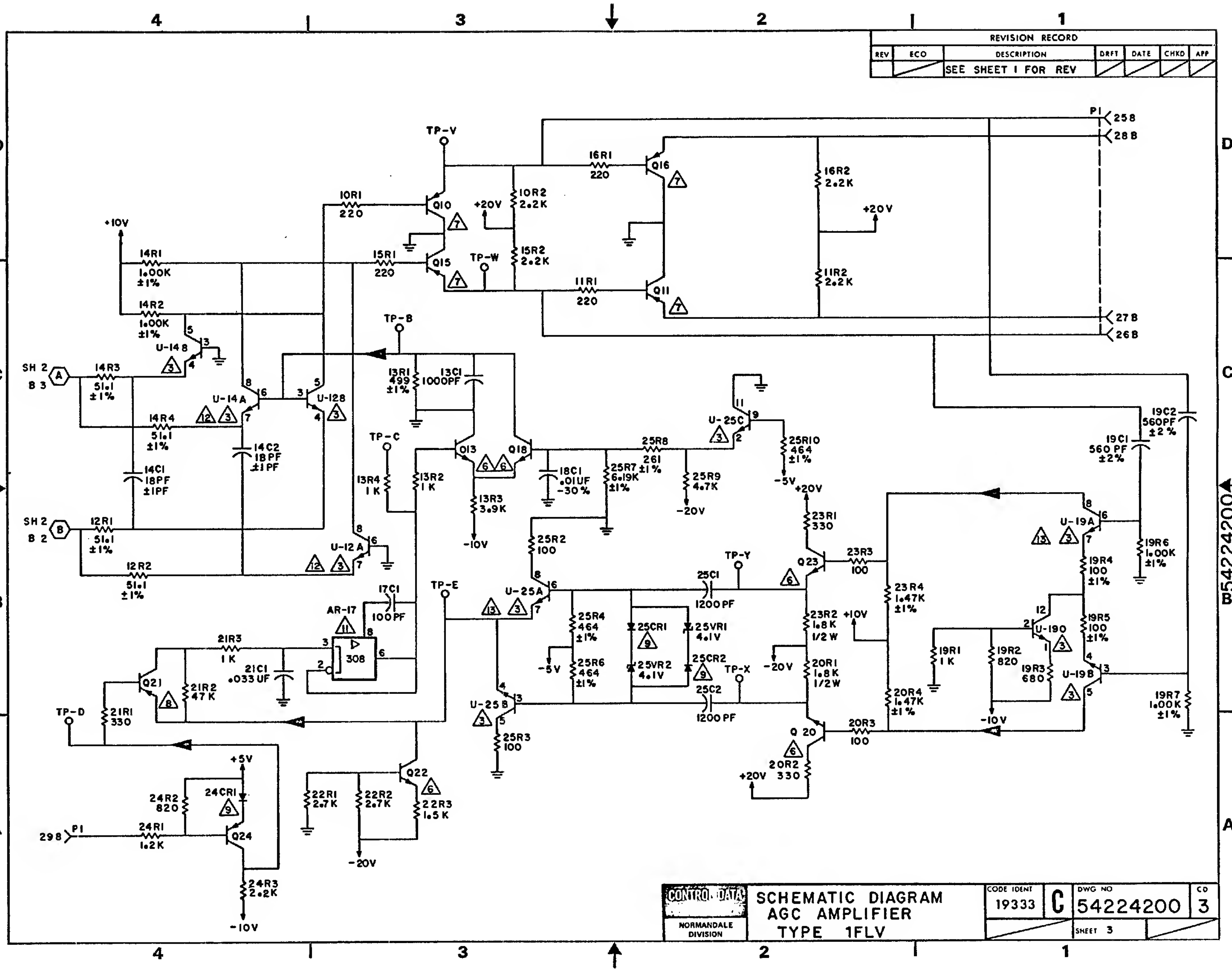
54224200

HPD

70629100 E


REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
SEE SHEET 1 FOR REV
+20V
8R1
1K
9R1
1K
9R2
1.8K
Q8
Q9
8R2
2.2K
14B
P1
6C1
.01UF
8R2
220
Q6
-10V
6R1
1.5K
6R3
2.2K
+20V
7R3
2.2K
7R1
1.5K
7C1
.01UF.
7R2
220
Q7
13B
-10V
6R4
121
±1%
6L1
5.6UH
6L2
2.2UH
6C2
180PF
±2%
6C3
240PF
±2%
7R4
121
±1%
7L1
5.6UH
7L2
2.2UH
TP-U
TP-T
5R1
220
Q5
3R1
220
Q3
-10V
-10V
P1
24B
23B
2C1
.01UF
6R5
121
±1%
6C4
.01UF
7R5
121
±1%
2C3
.01UF
SH 3
C 4
SHEET NO.
(TYP)
DWG ZONE
(TYP)
SH 3
B 4
2C2
22PF
±5%
U-2A
U-2B
2R3
2.15K
±1%
2R4
82.5
±1%
2R5
82.5
±1%
2R6
2.15K
±1%
U-2D
2R1
2.2K
2R2
3.9K
2R7
2.2K
-10V
Q4
4R4
1.96K
±1%
4R1
499
±1%
4R3
1.00K
±1%
4VR1
15V
4CR1
4R2
220
1/2 W
-20V
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
AGC AMPLIFIER
TYPE 1FLV
CODE IDENT
19333
C
DWG NO
54224200
CD
3
SHEET 2
54224200

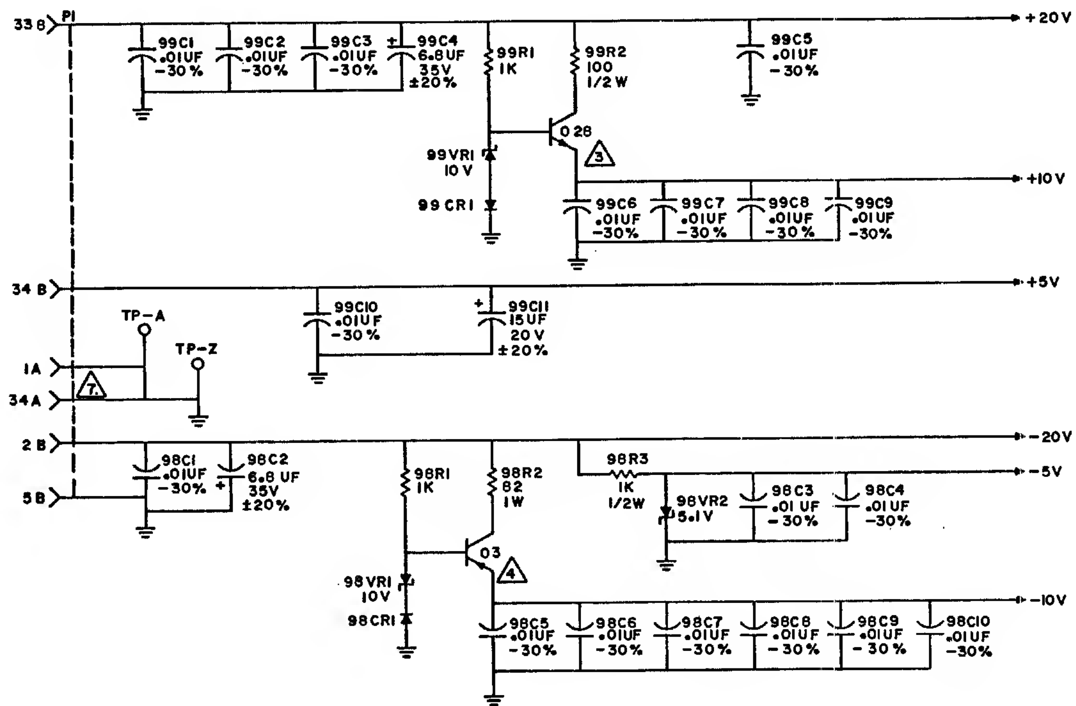
4-78



54224200

70629100 E

70629100 E



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4916, 50211610.
   ALL DIODES, SILICON, 24553500.
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%.

2. TRANSISTOR, ARRAY, QUAD, CA3018, 50251100.

3. TRANSISTOR, SNPN, 2N3569, 50210811.

4. TRANSISTOR, SPNP, 2N4919, 50221001.

5. TRANSISTOR, SPNP, 2N4258, 50211510.

6. TRANSISTOR, SNPN, 24562100.

7. PINS 1A THRU 34A ARE CONNECTED TO GND.

8. IC, TYPE 308, HAS PIN 7 CONNECTED TO +10V AND PIN 4 CONNECTED TO -10V.

9. PIN 10 OF U-10 AND U-11 CONNECTED TO GND.

10. PIN 10 OF U-2, U-9 AND U-27 CONNECTED TO -10V.

11. TRANSISTOR, SPNP, 2N5230, 50212200.

12. TEST SELECT RESISTOR TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.

REFERENCE DRAWINGS			
COMP ASSY 54224101			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	D. G. TUTTLE	7-20-72
CHK	[illegible]	[illegible]
ENGR	D. [illegible]	9-29-72
MFG	[illegible]	[illegible]
APPR		

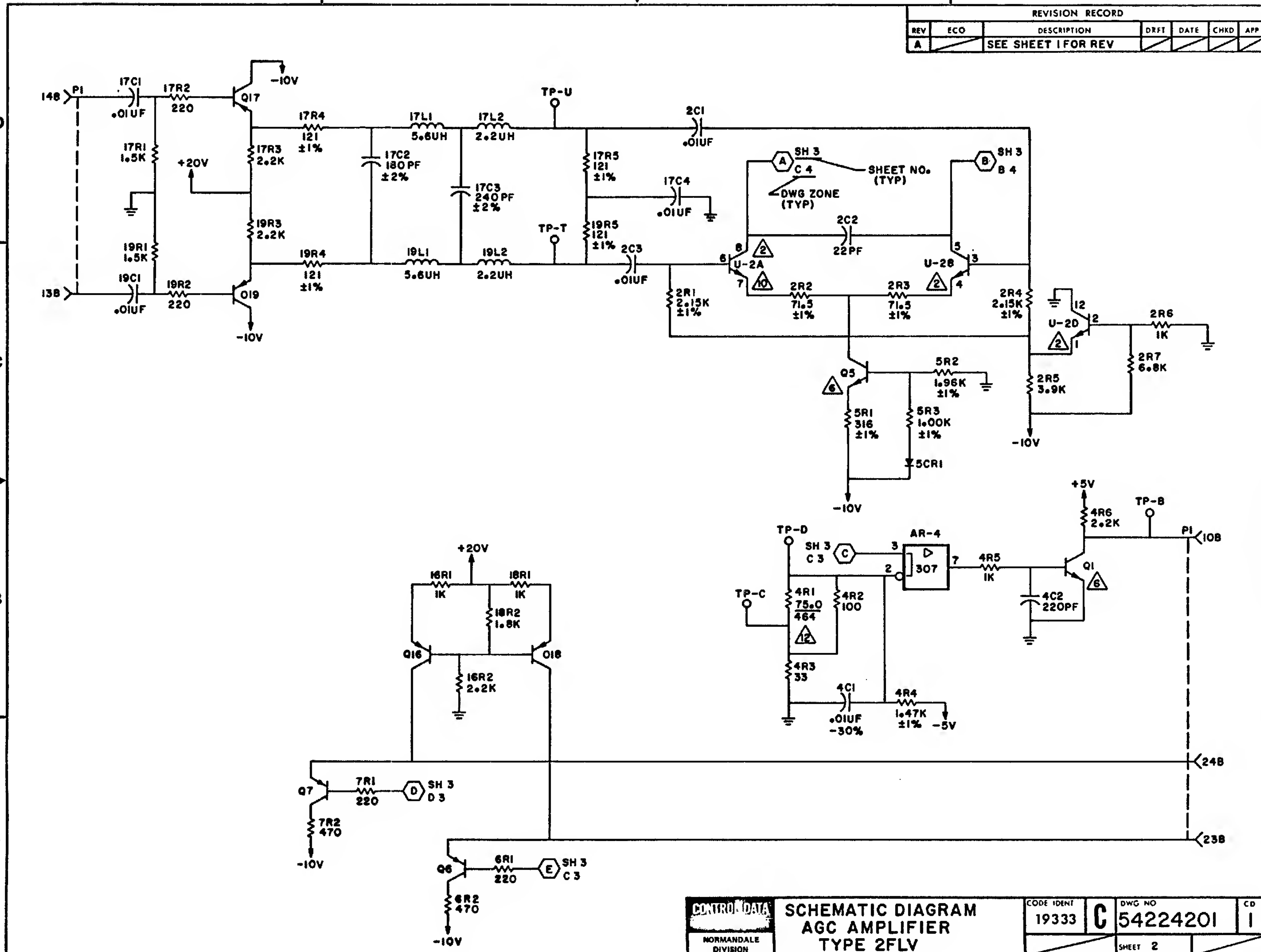
TITLE

SCHEMATIC DIAGRAM AGC AMPLIFIER TYPE 2FLV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54224201	1

SHEET 1 OF 3

54224201



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

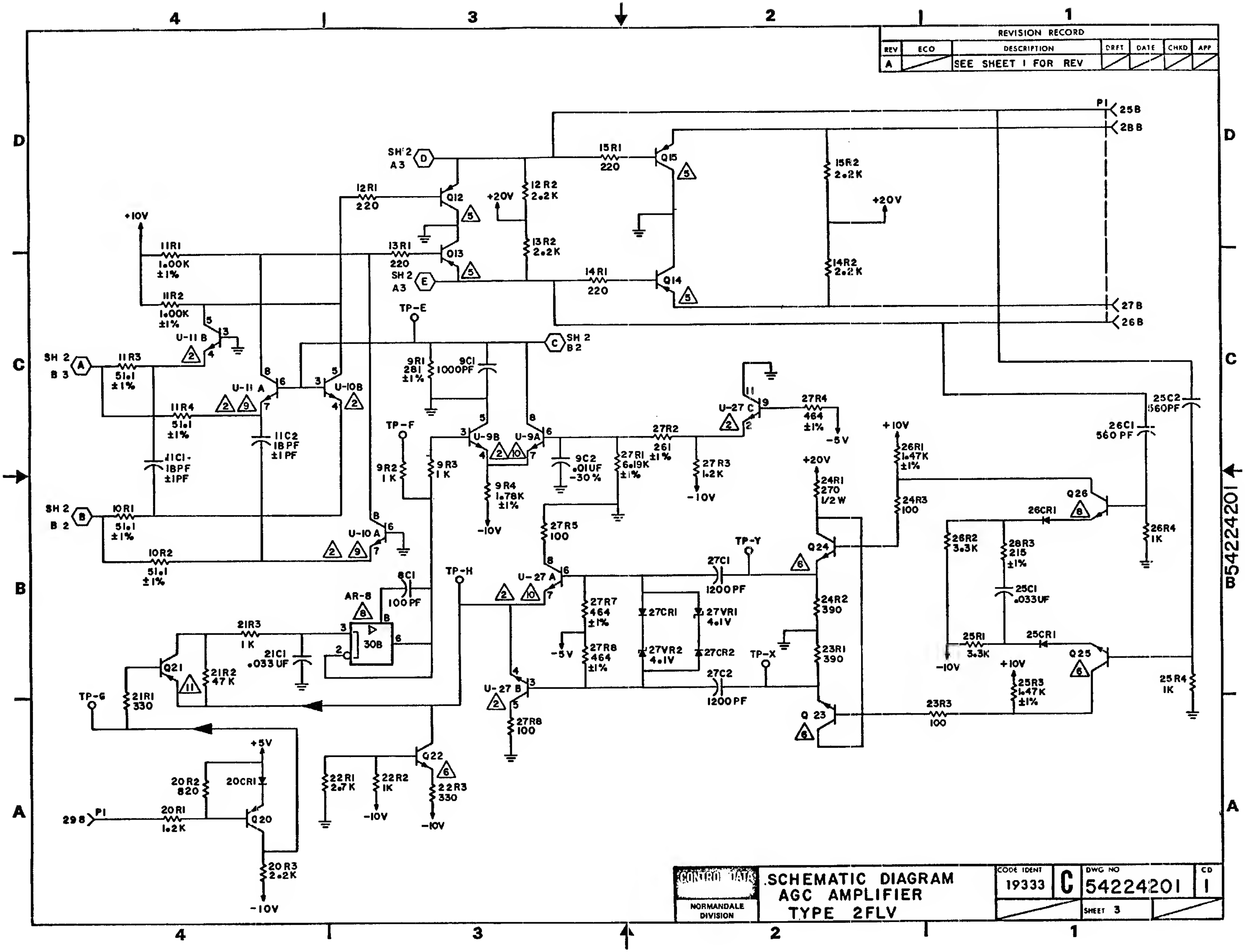
CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
AGC AMPLIFIER
TYPE 2FLV

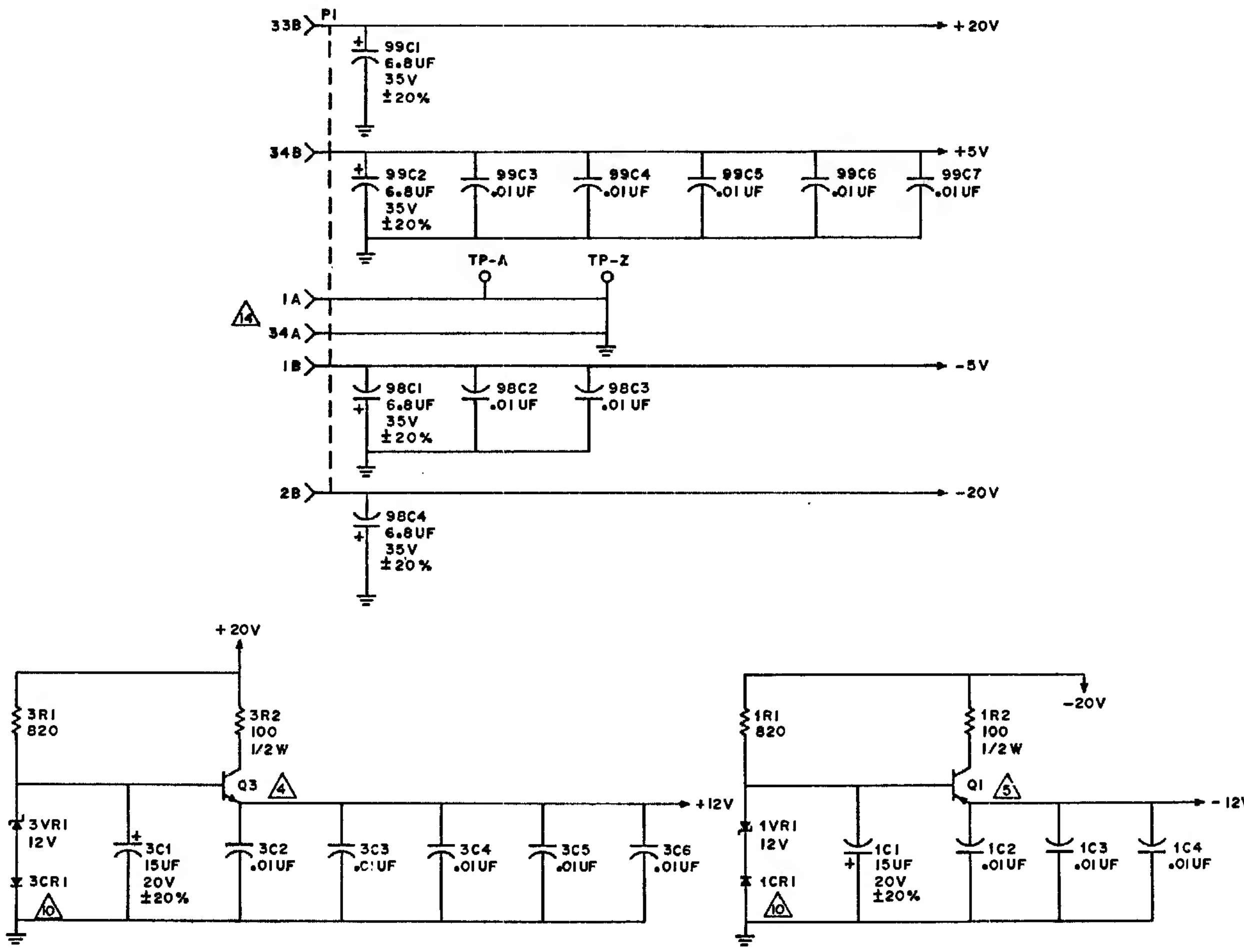
CODE IDENT 19333 | C | DWG NO 54224201 | CD 1

SHEET 2

54224201


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
AGC AMPLIFIER
TYPE 2FLV
CODE IDENT 19333
C
DWG NO 54224201
CD 1
SHEET 3
54224201
SH 2 A B 3
SH 2 B B 2
SH 2 D A3
SH 2 E A3
SH 2 C B 2
TP-E
TP-F
TP-H
TP-G
TP-Y
TP-X
P1 25B
28B
27B
26B
29B P1
U-11 A
U-11 B
U-10 A
U-10 B
U-9A
U-9B
U-27 A
U-27 B
U-27 C
AR-8
308
Q12
Q13
Q14
Q15
Q20
Q21
Q22
Q23
Q24
Q25
Q26
+10V
+20V
-10V
-5V
+5V

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		3-24-72		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, 92115021
   ALL ZENER DIODE VOLTAGE TOLERANCES ± 5%
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V.
2. TRANSISTOR, SNPN, 2N2221, 50210102.
3. TRANSISTOR, CA3018, QUAD, 50251100.
4. TRANSISTOR, SNPN, 2N3569, 50210811.
5. TRANSISTOR, SPNP, 2N3638, 50210610.
6. TRANSISTOR, SPNP, 2N3645, 50211210.
7. TRANSISTOR, SPNP, 2N4916, 50211610.
8. TIME DELAY FOR REFERENCE ONLY.
9. PINS 9 AND 10 OF U-11 ARE INTERCONNECTED.
10. DIODE, SILICON, 92115023.
11. COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
12. 8 PIN IC, TYPES 301 AND 308, HAVE PIN 7 CONNECTED TO +12V; PIN 4 TO -12V
13. 8 PIN IC, TYPE 307, HAS PIN 8 CONNECTED TO +12V; PIN 4 TO -5V.
14. CONNECTOR PINS 1A THRU 34A ARE CONNECTED TO GND.
15. PIN 10 OF U-8 IS CONNECTED TO GND.

REFERENCE DRAWINGS			
COMPONENT ASSY 54224501			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	8R3A1	
DWN	R. KONECNY	2-16-72
CHK	T. Hanson	2-22-72
ENGR	D. Young	2-22-72
MFG		2-23-72
APPR		2-23-72

TITLE: SCHEMATIC DIAGRAM LEVEL DETECTOR TYPE 2FMV

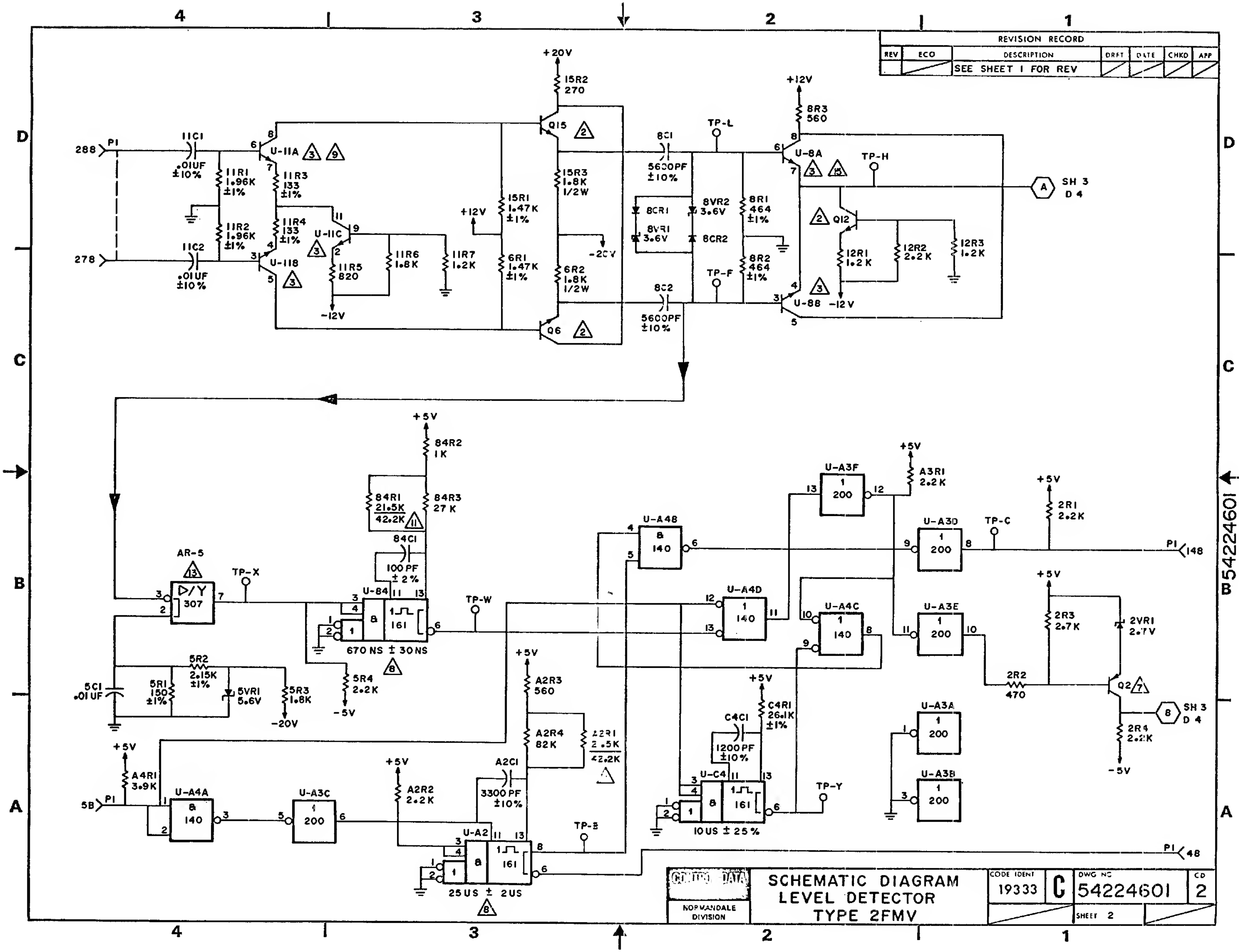
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54224601	2

SHEET 1 OF 3

HPD

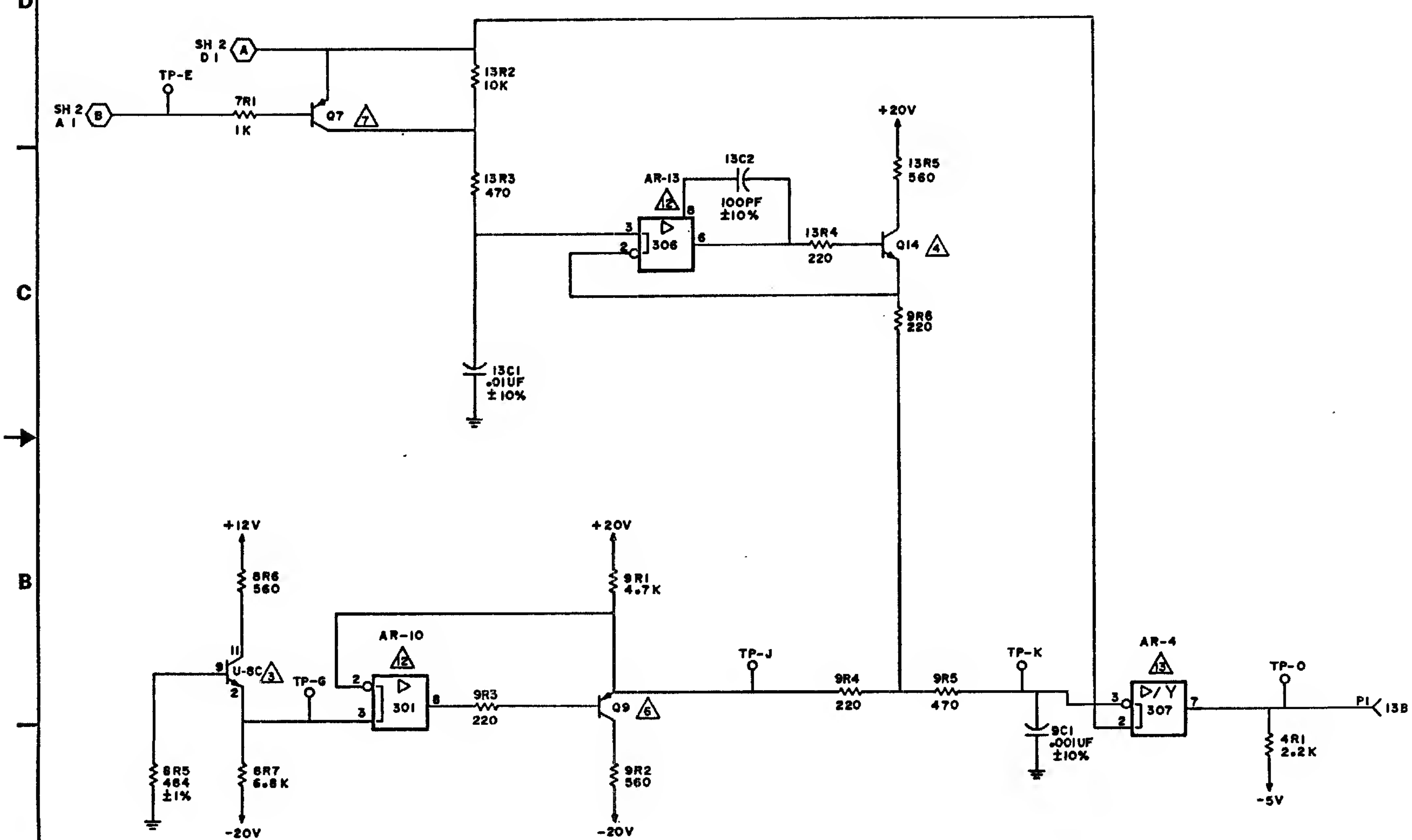
54224601

70629100 E



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
LEVEL DETECTOR
TYPE 2FMV
CODE IDENT 19333
C
DWG NO 54224601
CD 2
SHEET 2
54224601

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET I FOR REV				

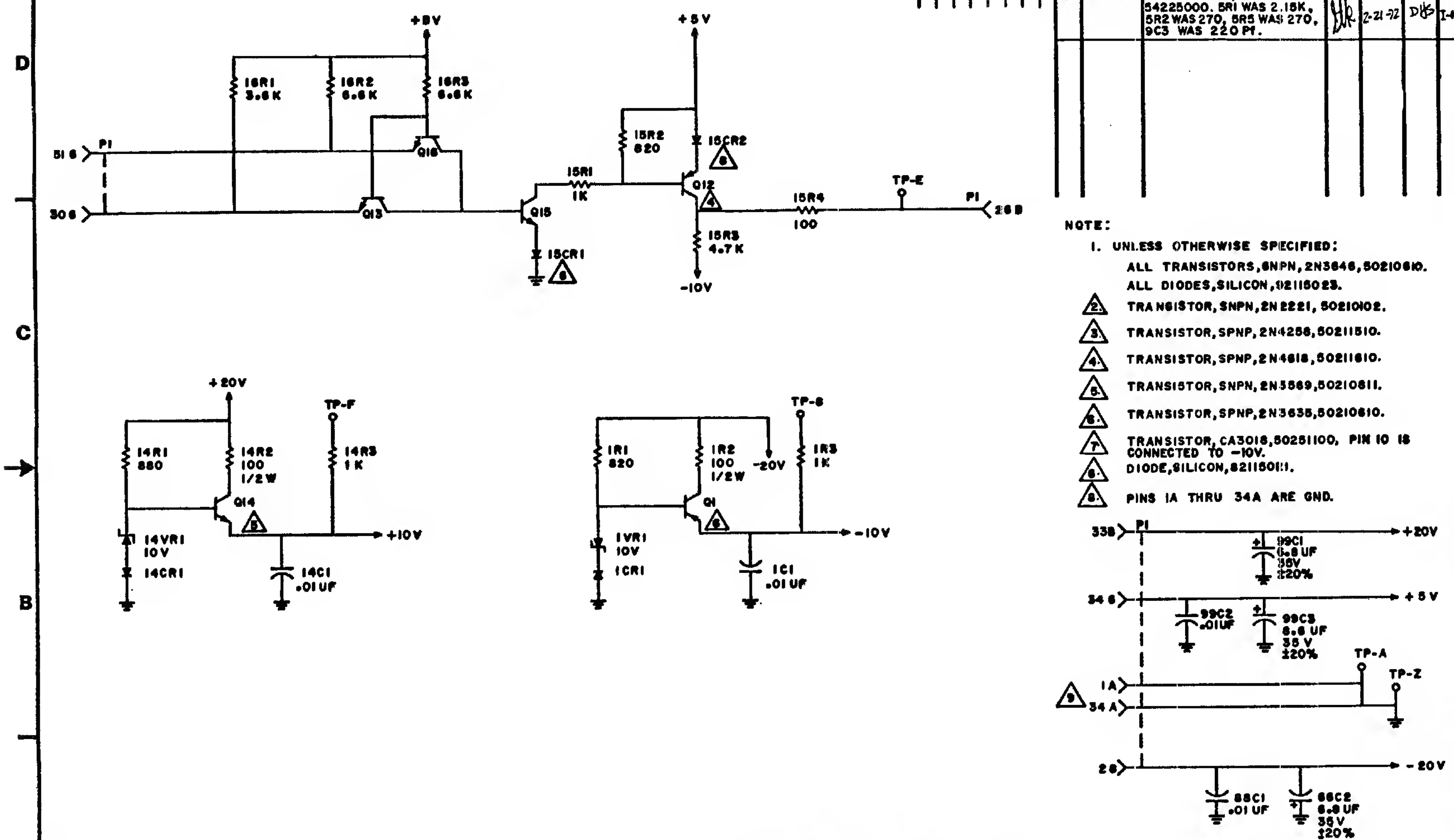


CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
LEVEL DETECTOR
TYPE 2FMV

CODE IDENT		DWG NO	CD
19333	C	54224601	2
		SHEET 3	

54224601



REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		12-17-71	.	RH
B	PE30500	DWG 54225001, DWG WAS 54225000. 5R1 WAS 2.15K, 5R2 WAS 270, 5R5 WAS 270, 9C3 WAS 220 PF.		2-21-72	DKS	

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210610.
   ALL DIODES, SILICON, 92115023.
   2. TRANSISTOR, SNPN, 2N2221, 50210102.
   3. TRANSISTOR, SPNP, 2N4258, 50211510.
   4. TRANSISTOR, SPNP, 2N4618, 50211610.
   5. TRANSISTOR, SNPN, 2N3569, 50210611.
   6. TRANSISTOR, SPNP, 2N3635, 50210610.
   7. TRANSISTOR, CA3018, 50251100, PIN 10 IS CONNECTED TO -10V.
   8. DIODE, SILICON, 82115011.
   9. PINS 1A THRU 34A ARE GND.

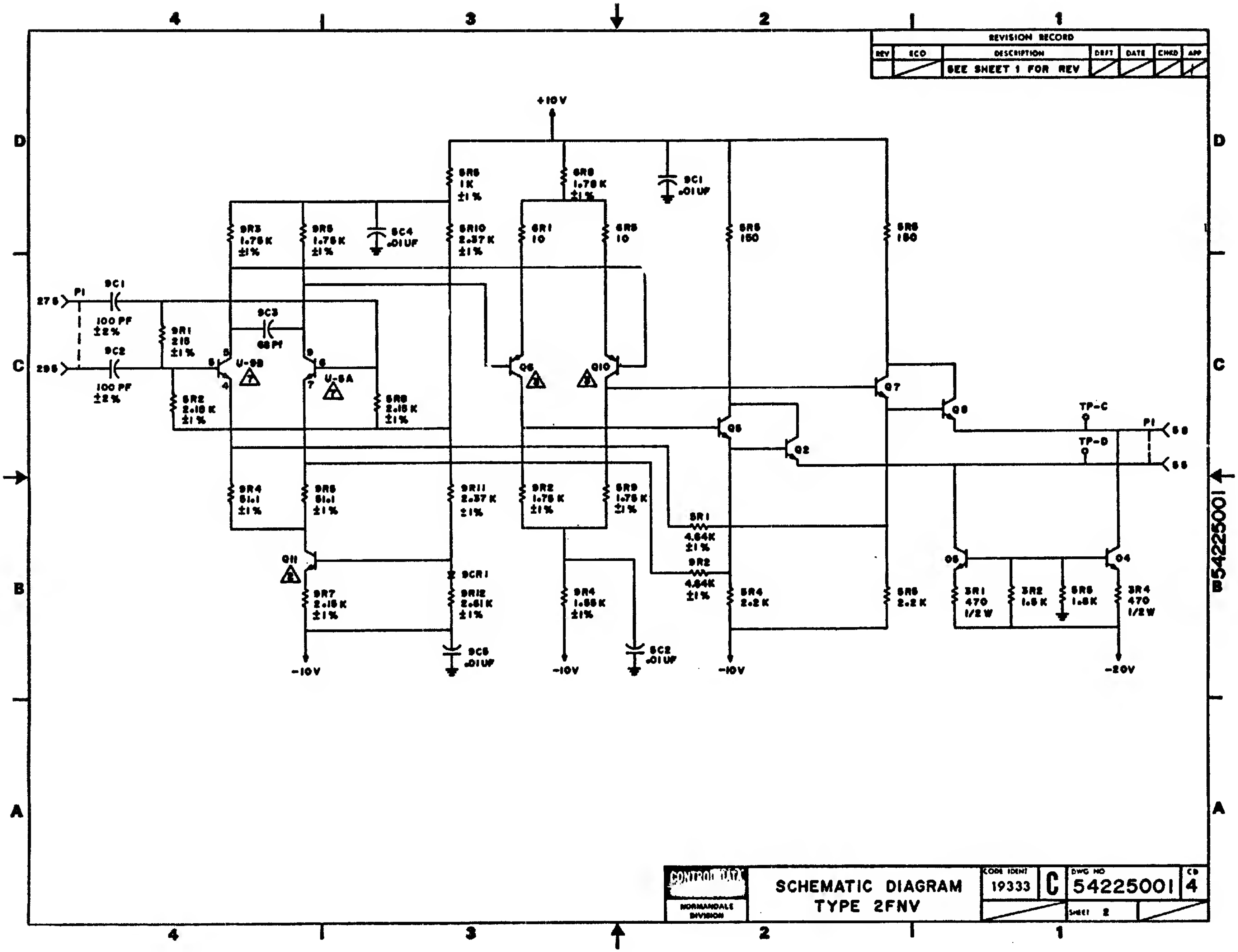
REFERENCE DRAWINGS	CONTROL DATA CORPORATION	NORMANDALE DIVISION
COMPONENT ASSY 54224900	FIRST USED ON	BR3A1
	DWN	R. KONECNY 10-18-71
	CHK	K. STRELTER 2-3-71
COMPONENTS, EXCEPT AS NOTED	ENGR	D. Young 12-15-71
TOLERANCE / VALUE / RATING	MFG	12-16-71
RES ±5 % / OHMS / 1/4 W	APPR	12-16-71
CAP -30%		

TITLE: SCHEMATIC DIAGRAM DIFFERENTIATOR & AMPLIFIER TYPE 2FNV

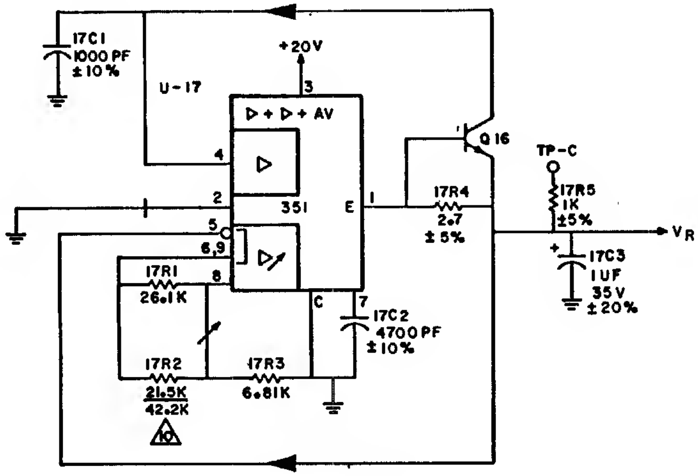
CODE IDENT 19333 | C | DRAWING NUMBER 54225001 | CO 4

SHEET 1 OF 2

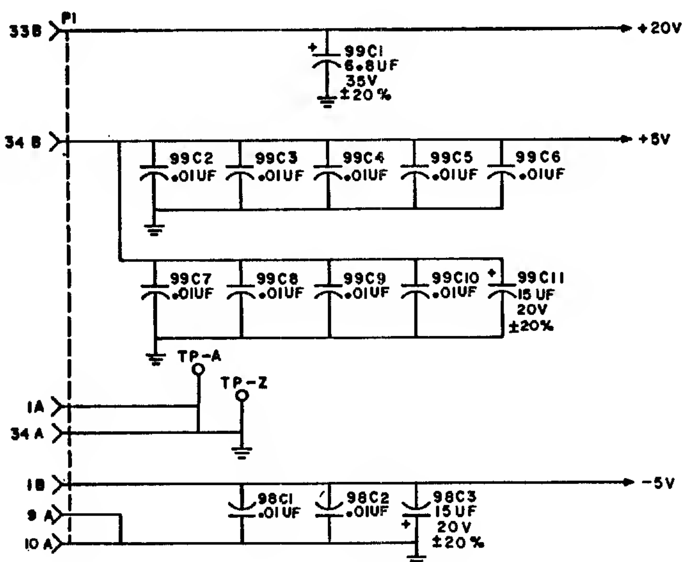
54225001


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2FNV
CODE IDENT 19333
C
DWG NO 54225001
CD 4
SHEET 2
54225001

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	FE23000	RELEASED				



V_R (<.20A) REGULATOR



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON PLANAR, 24551500
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. TRANSISTOR, SPNP, 2N3638, 50210610.
3. TRANSISTOR, SPNP, 2N3645, 50211210.
4. TRANSISTOR, SPNP, 2N4258, 50211510.
5. TRANSISTOR, SPNP, 2N4916, 50211610.
6. TRANSISTOR, SNPN, 2N4923, 50220902.
7. TRANSISTOR, SPNP, 2N5456, 50212100.
8. TRANSISTOR, SILICON, PLANAR, 24562100.
9. DIODE, GERMANIUM, 11801200.
10. COMPONENT VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
11. IC, TYPE 301, HAS PIN 7 CONNECTED TO +20V; PIN 4 TO -5V.
12. IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.
13. CONNECTOR PINS 15A, 15B, 16A AND 23B, AND TEST POINTS H, J, AND M ARE NOT USED.
14. DIODE, SCHOTKY BARRIER, 50241400.
15. DELAY TIME FOR REF ONLY.

REFERENCE DRAWINGS
COMP ASSY: 54225305

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR3A1 / BR3A3	
DWN	D. G. TUTTLE	8-7-72
CHK		8-15-72
ENGR		7-16-72
MFG		7-22-72
APPR		7-21-72

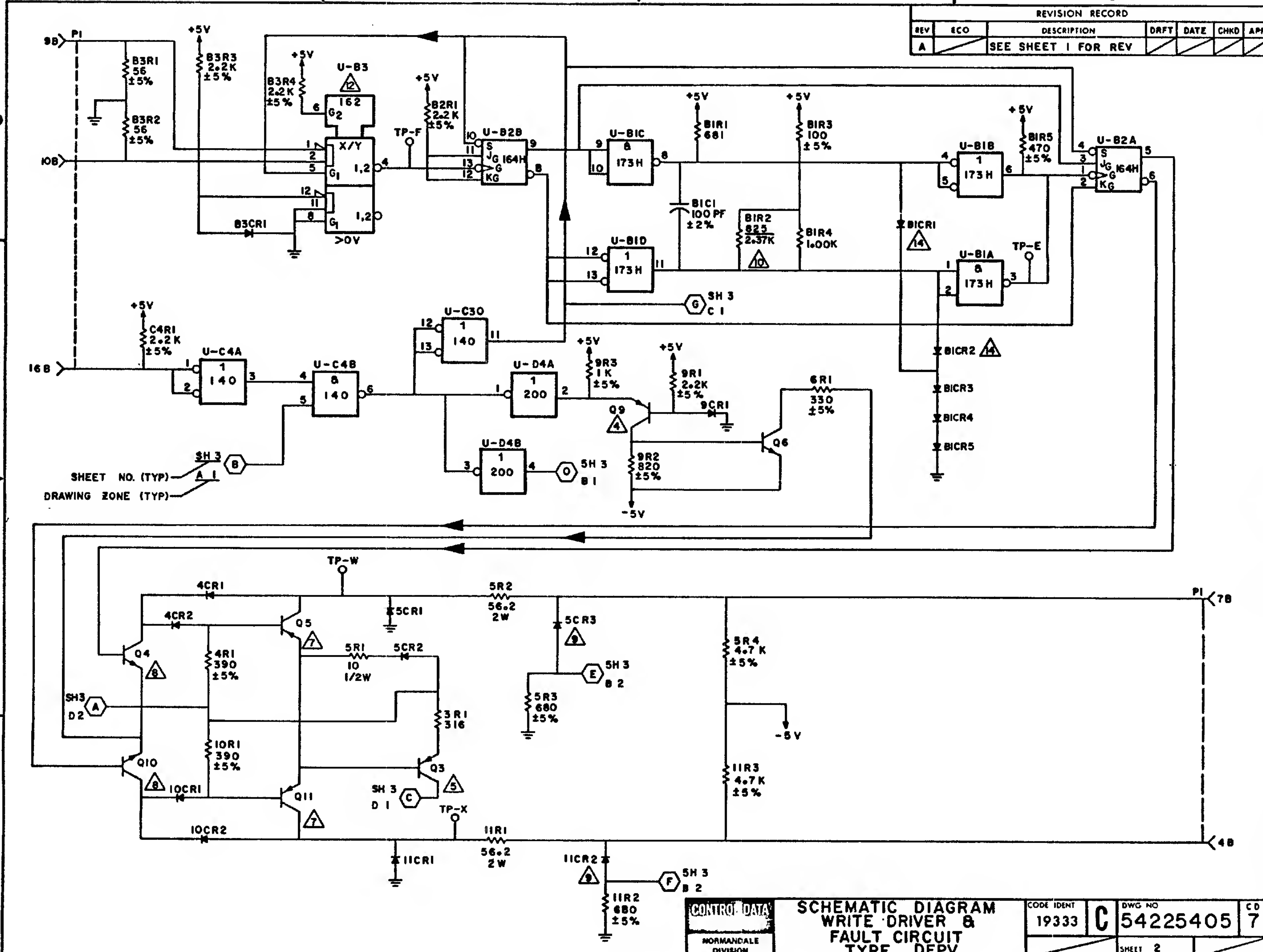
TITLE
SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE DFPV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54225405	7

SHEET 1 OF 3

54225405

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



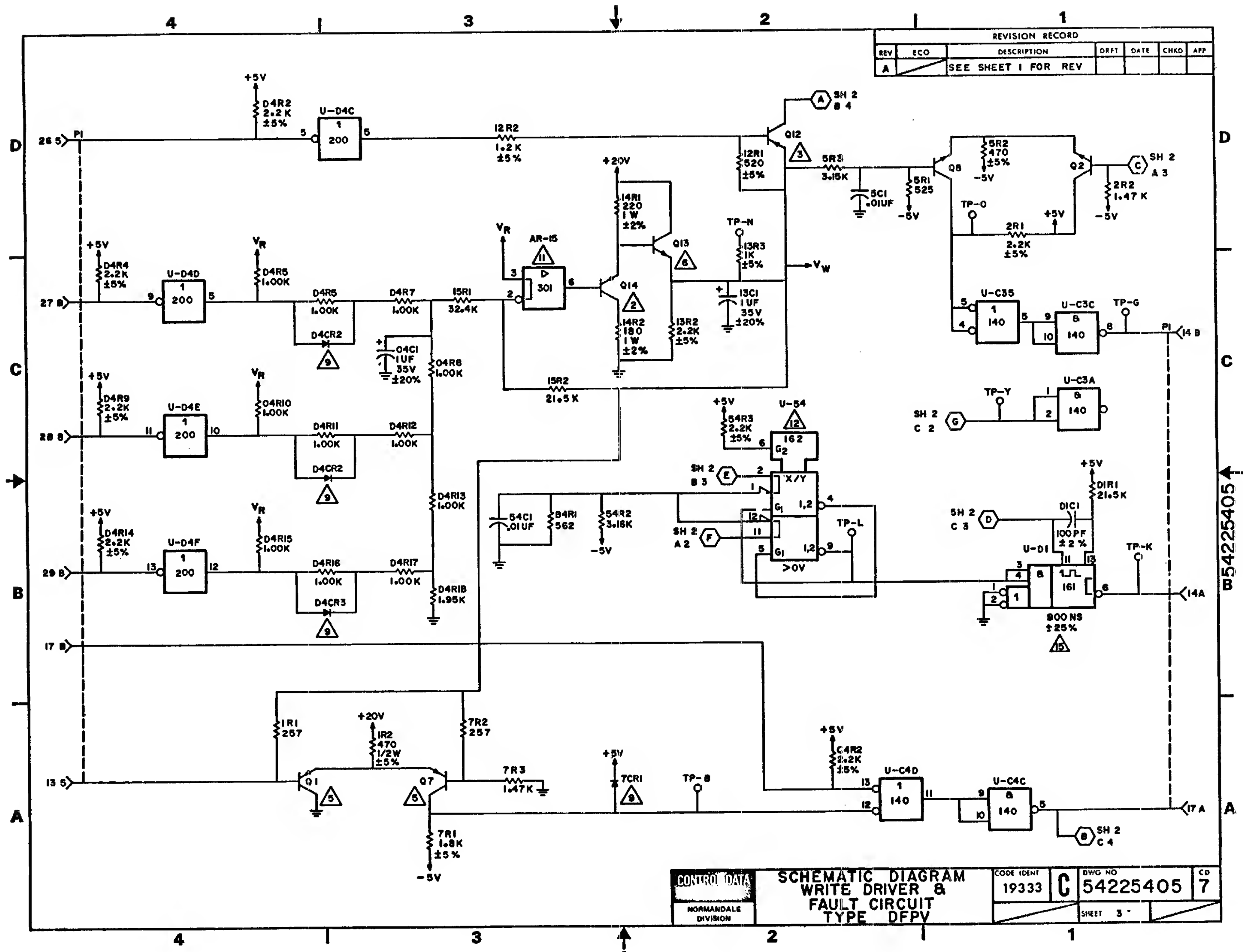
CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE DFPV

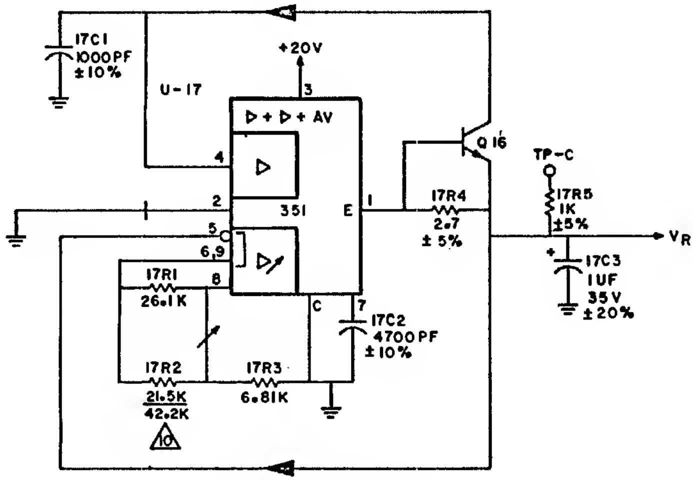
CODE IDENT		DWG NO	CD
19333	C	54225405	7
		SHEET 2	

54225405

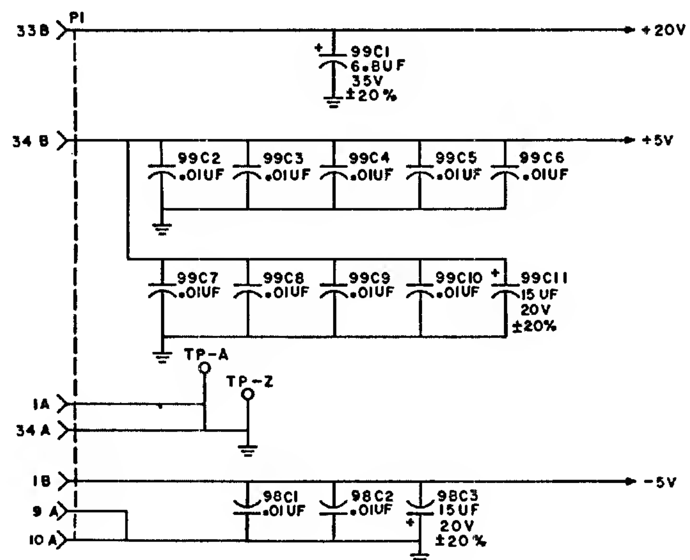
70629100 E


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
U-D4C
U-D4D
U-D4E
U-D4F
AR-15
301
Q12
Q13
Q14
Q8
Q2
Q1
Q7
U-C3S
U-C3C
U-C3A
U-54
162
U-D1
161
900 NS ±25%
U-C4D
U-C4C
TP-N
TP-O
TP-G
TP-Y
TP-L
TP-K
TP-B
+20V
+5V
-5V
V_R
V_W
12R2 1.2 K ±5%
15R1 32.4K
15R2 21.5 K
14R1 220 1 W ±2%
14R2 180 1 W ±2%
13R2 2.2K ±5%
13R3 1K ±5%
13C1 1 UF 35V ±20%
12R1 520 ±5%
5R3 3.16K
5C1 .01UF
5R1 525
5R2 470 ±5%
2R1 2.2K ±5%
2R2 1.47 K
D4C1 1UF 35V ±20%
D1C1 100 PF ±2 %
D1R1 21.5K
54C1 .01UF
54R1 562
54R2 3.16K
54R3 2.2K ±5%
1R1 257
1R2 470 1/2W ±5%
7R2 257
7R3 1.47K
7R1 1.8K ±5%
7CR1
C4R2 2.2K ±5%
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
WRITE DRIVER &
FAULT CIRCUIT
TYPE DFPV
CODE IDENT 19333
C
DWG NO 54225405
CD 7
SHEET 3
54225405

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED			[illegible]	[illegible]



V_R (<.20A) REGULATOR



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON PLANAR, 24553500
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. TRANSISTOR, SPNP, 2N3638, 50210610.
3. TRANSISTOR, SPNP, 2N3645, 50211210.
4. TRANSISTOR, SPNP, 2N4258, 50211510.
5. TRANSISTOR, SPNP, 2N4916, 50211610.
6. TRANSISTOR, SNPN, 2N4923, 50220902.
7. TRANSISTOR, SPNP, 2N5456, 50212100.
8. TRANSISTOR, SILICON, PLANAR, 24562100.
9. DIODE, GERMANIUM, 11801200.
10. COMPONENT VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
11. IC, TYPE 301, HAS PIN 7 CONNECTED TO +20V; PIN 4 TO -5V.
12. IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.
13. CONNECTOR PINS 15A, 15B, 16A AND 23B, AND TEST POINTS H, J, AND M ARE NOT USED.
14. DIODE, SCHOTKY BARRIER, 50241400.
15. DELAY TIME FOR REF ONLY.

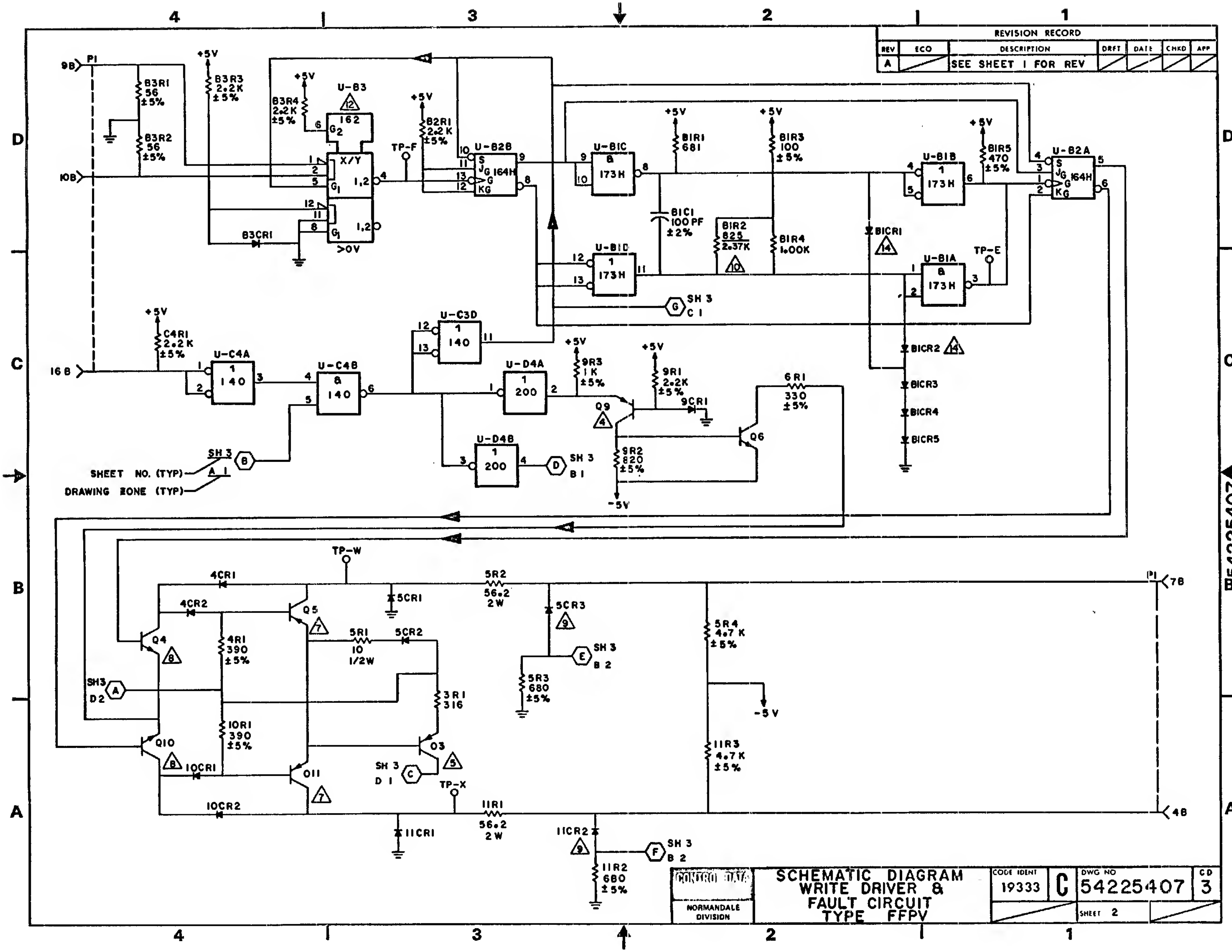
54225407

REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY: 54225307	USED ON	8R3A1/8R3A3	SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE FFPV
	DWN	D.G. TUTTLE	8-4-72
	CHK	[illegible]	[illegible]
COMPONENTS, EXCEPT AS NOTED	ENGR	[illegible]	[illegible]
TOLERANCE / VALUE / RATING	MFG	[illegible]	[illegible]
RES ±1% / OHMS / 1/4W	APPD	[illegible]	[illegible]
CAP -30%			

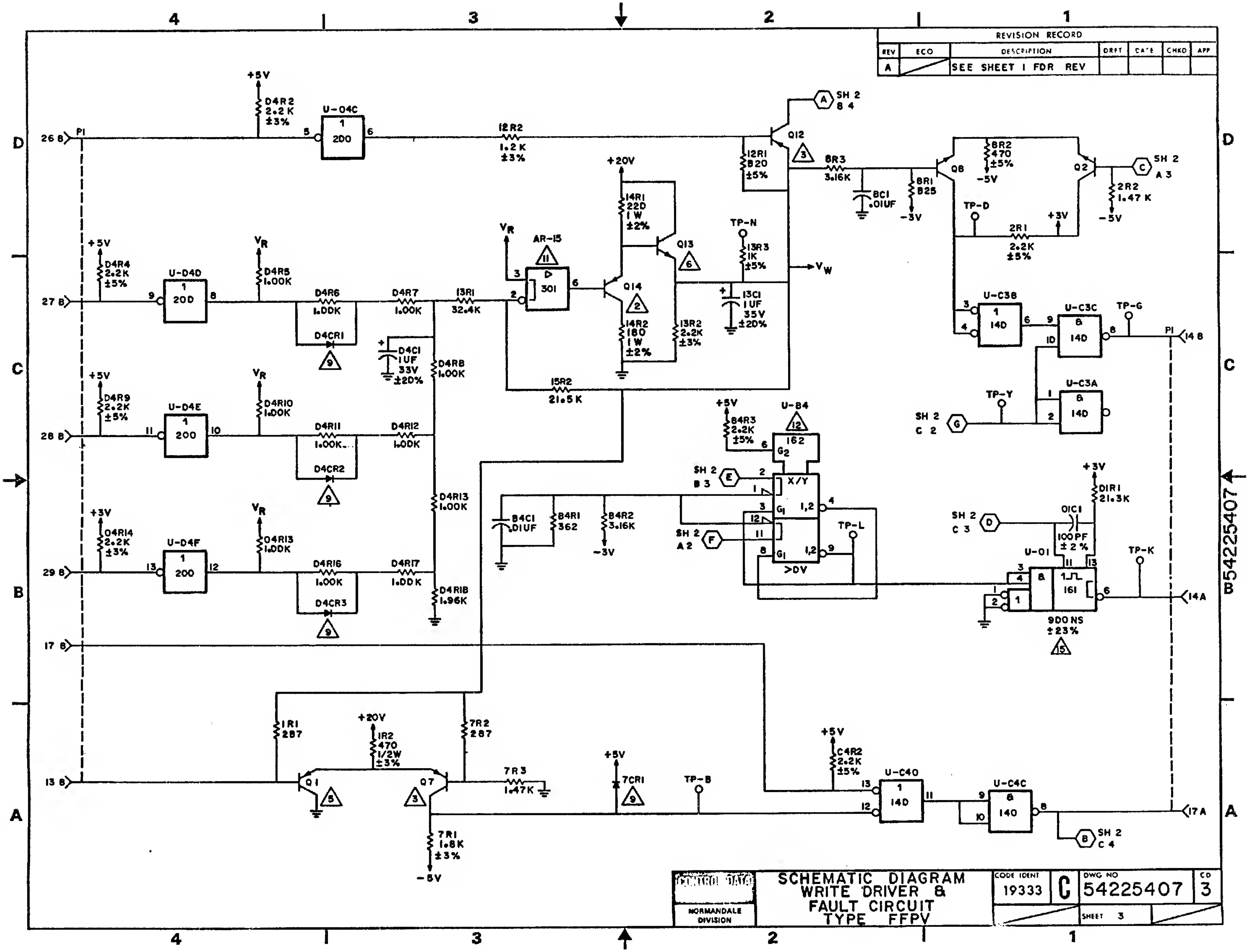
CODE IDENT 19333 | C | DRAWING NUMBER 54225407 | CD 3

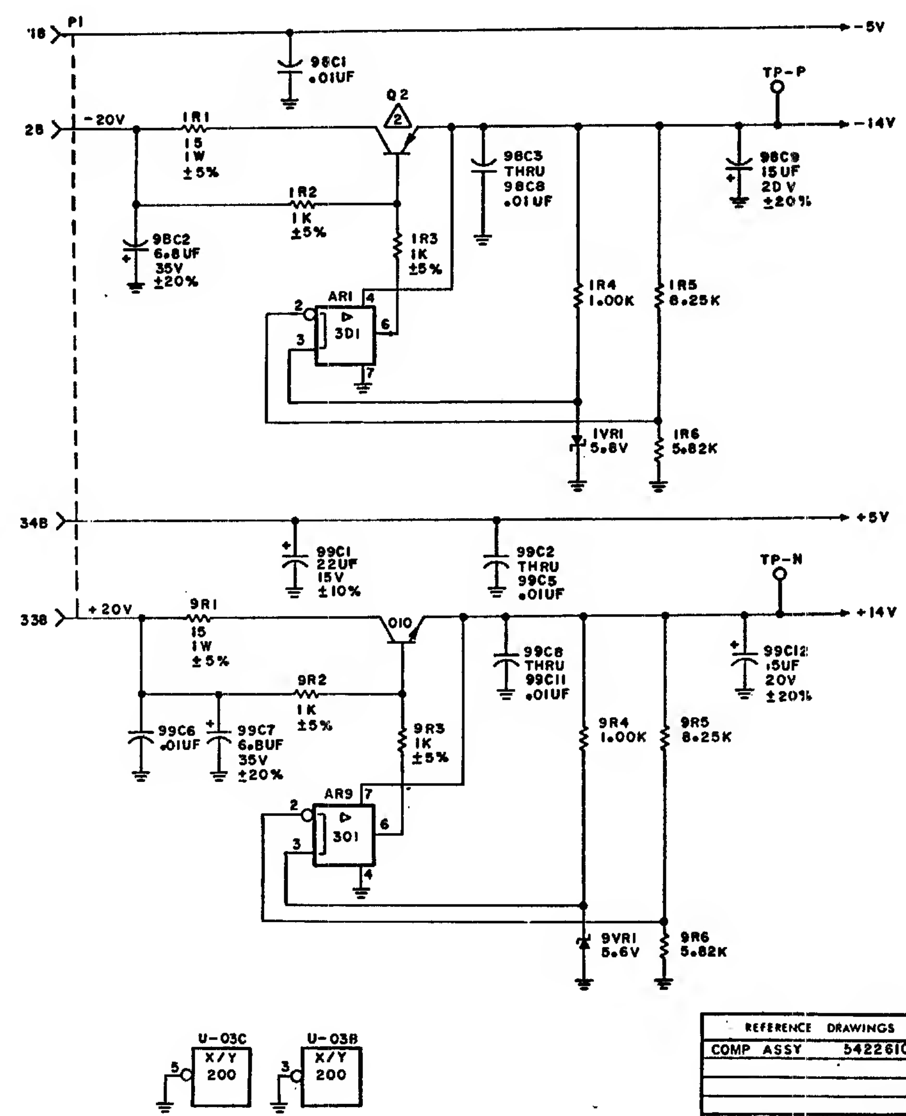
SHEET 1 OF 3

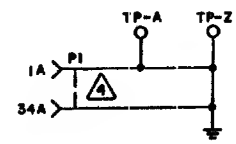
70629100 E



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
U-B3
U-B2B
U-B1C
U-B1D
U-B1B
U-B1A
U-B2A
U-C3D
U-C4A
U-C4B
U-D4A
U-D4B
TP-F
TP-E
TP-W
TP-X
SH 3 G C 1
SH 3 B
SH 3 D B 1
SH 3 E B 2
SH 3 F B 2
SH3 A D2
SH 3 C D 1
SHEET NO. (TYP)
DRAWING ZONE (TYP)
-5V
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE FFPV
CODE IDENT 19333
C
DWG NO 54225407
CD 3
SHEET 2
54225407


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
U-04C
U-D4D
U-D4E
U-D4F
AR-15
Q12
Q8
Q2
Q13
Q14
Q1
Q7
U-C3B
U-C3C
U-C3A
U-B4
U-01
U-C40
U-C4C
TP-N
TP-D
TP-G
TP-Y
TP-L
TP-K
TP-B
900 NS ±23%
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
WRITE DRIVER &
FAULT CIRCUIT
TYPE FFPV
CODE IDENT 19333
C
DWG NO 54225407
CD 3
SHEET 3
54225407





SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED				

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, TIP 29, 50221800
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL DIODES, SILICON, PLANAR, 24553500
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V
2. TRANSISTOR, SPNP, TIP 30, 50221900.
3. RESISTORS AIR1 THRU AIR3, C1R1 THRU C1R5, C2R1 THRU C2R4, E1R1 AND E1R2 TO BE SELECTED FROM DWG. 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
4. ALL UNUSED CONNECTOR PINS ARE CONNECTED TO GND, EXCEPT 28B, 29B, 30B AND 31B.
5. TRANSISTOR, N CHANNEL J FET, 50218302.
6. IC'S U-E1 AND U-E4, ELEMENT NO. 195, HAS PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
7. IC'S ARA1, ARC1 AND ARC2, ELEMENT NO. 306, HAS PIN 4 CONNECTED TO -14V AND PINS 9 AND 13 CONNECTED TO +14V.

REFERENCE DRAWINGS	
COMP ASSY	54226107

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR302	
DWN	SR WILSON	9-27-73
CHK		
ENGR		
MFG		
APPR		

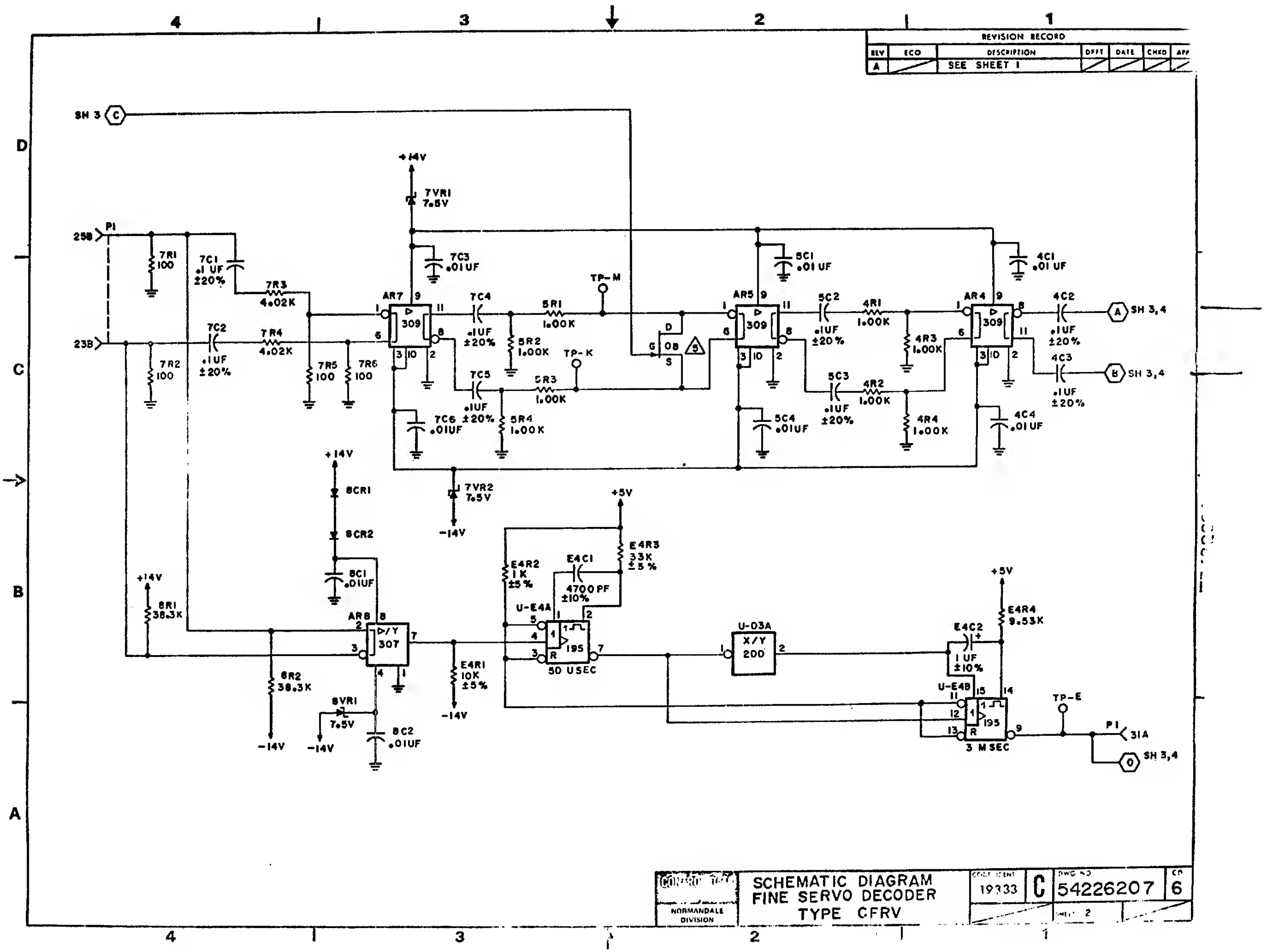
TITLE: SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE CFRV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54226207	6

SHEET 1 OF 4

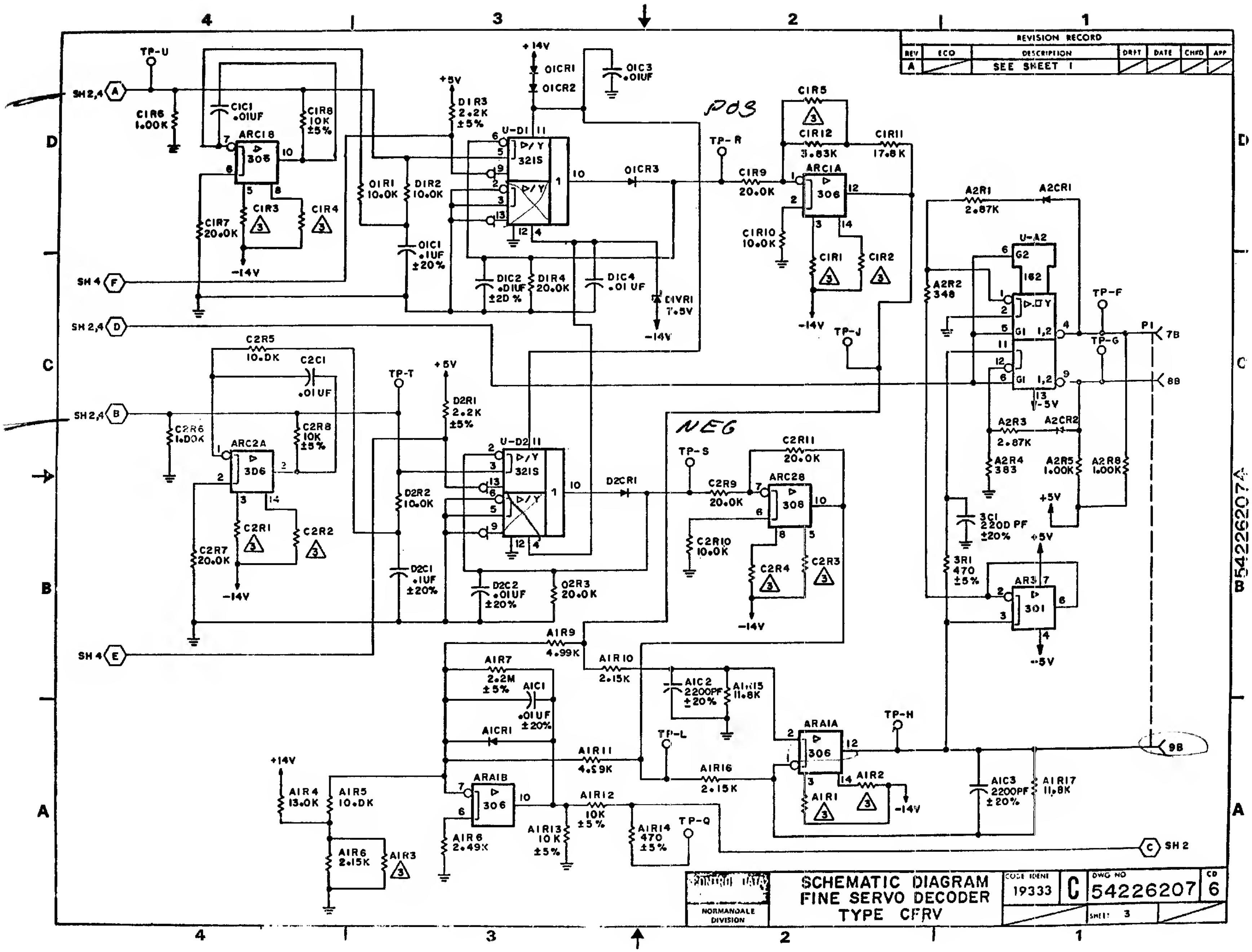
B54226207 A

4-92.2

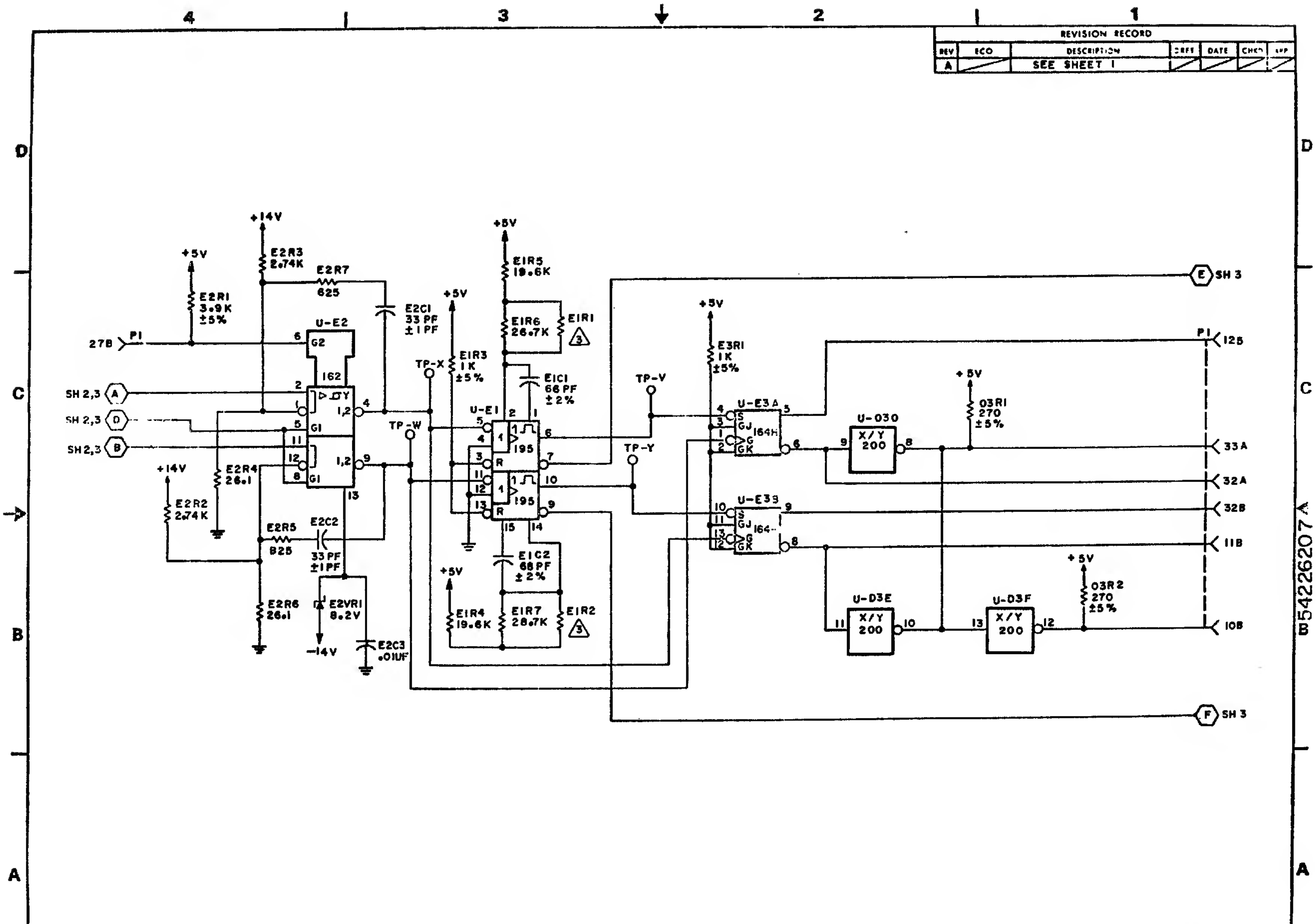


70629100 F

70629100 F



4-92.3

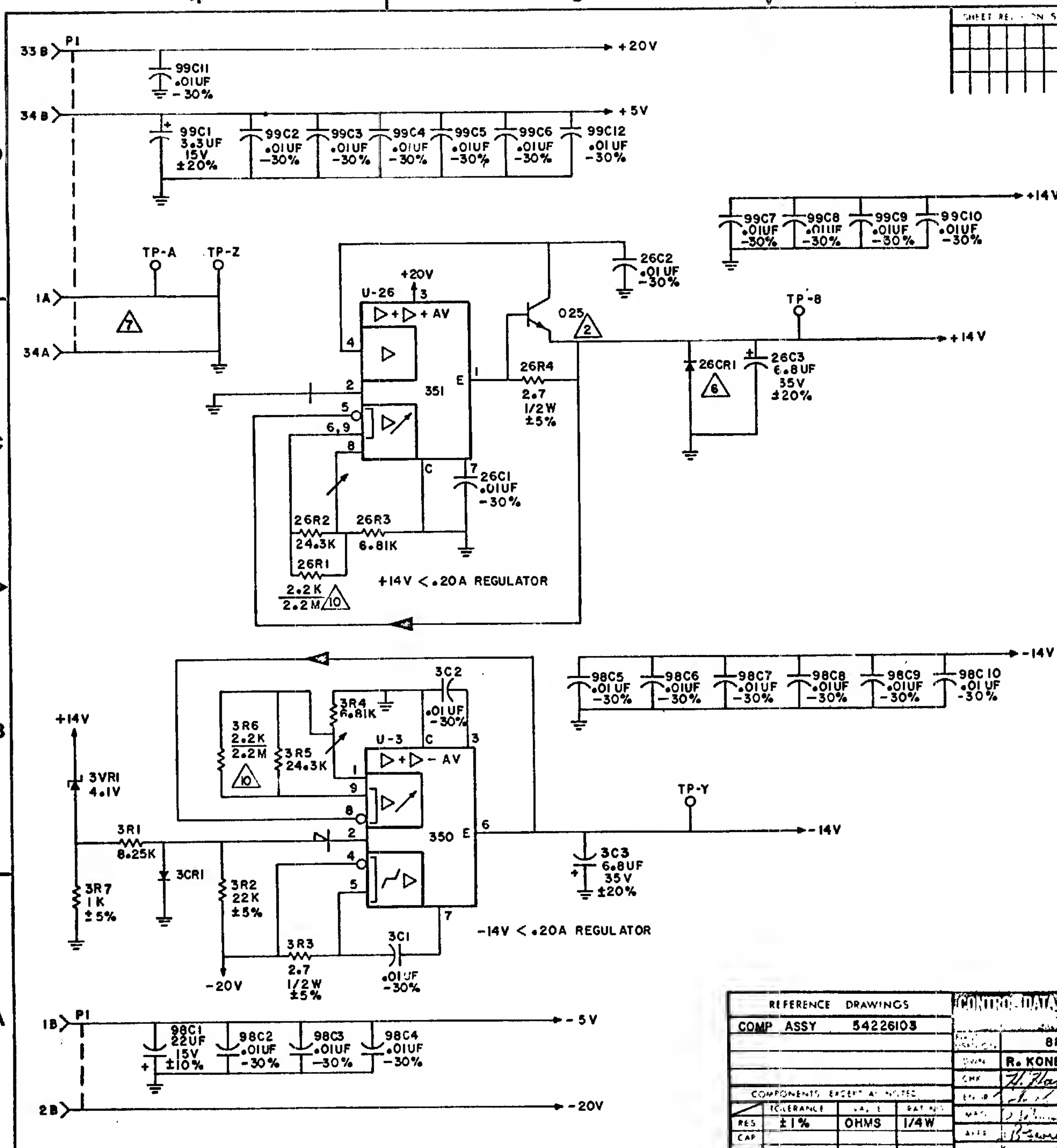


CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE CFRV

CODE IDENT 19333 | C | DWG NO 54226207 | CD 6
SHEET 4

70629100 E



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED		3-23-72		

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   - ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
   - ALL TRANSISTORS, SPNP, 2N3250, 50211100.
   - ALL DIODES SILICON, 24553500.
   - ALL ZENER DIODE VOLTAGE TOLERANCES ±5%

2. TRANSISTOR SNPN, 2N2221, 50210102.
3. TRANSISTOR SNPN, 2N3423, 50212000.
4. TRANSISTOR NFET 2N5434, 50218302.
5. TRANSISTOR SNPN, 2N2060, 50210900.
6. DIODE, GERMANIUM, 11801200.
7. ALL CONNECTOR PINS NOT OTHERWISE DESIGNATED ARE GND.
8. IC PACKAGE U-A1 HAS PIN 13 CONNECTED TO -5V.
9. IC PACKAGE AR1,2,6,7,9,10,19 AND 23 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
10. RESISTORS 26R1 AND 3R6 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
11. RESISTOR 1R2 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
12. IC PACKAGES U-21 AND U-24 HAVE PIN 5 CONNECTED TO -5V.
13. DELAY TIMES FOR REFERANCE ONLY.

54226203 A

REFERENCE DRAWINGS	
COMP ASSY	54226103

COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4W
CAP			

CONTROL DATA — NORMANDALE DIVISION

8R3A3

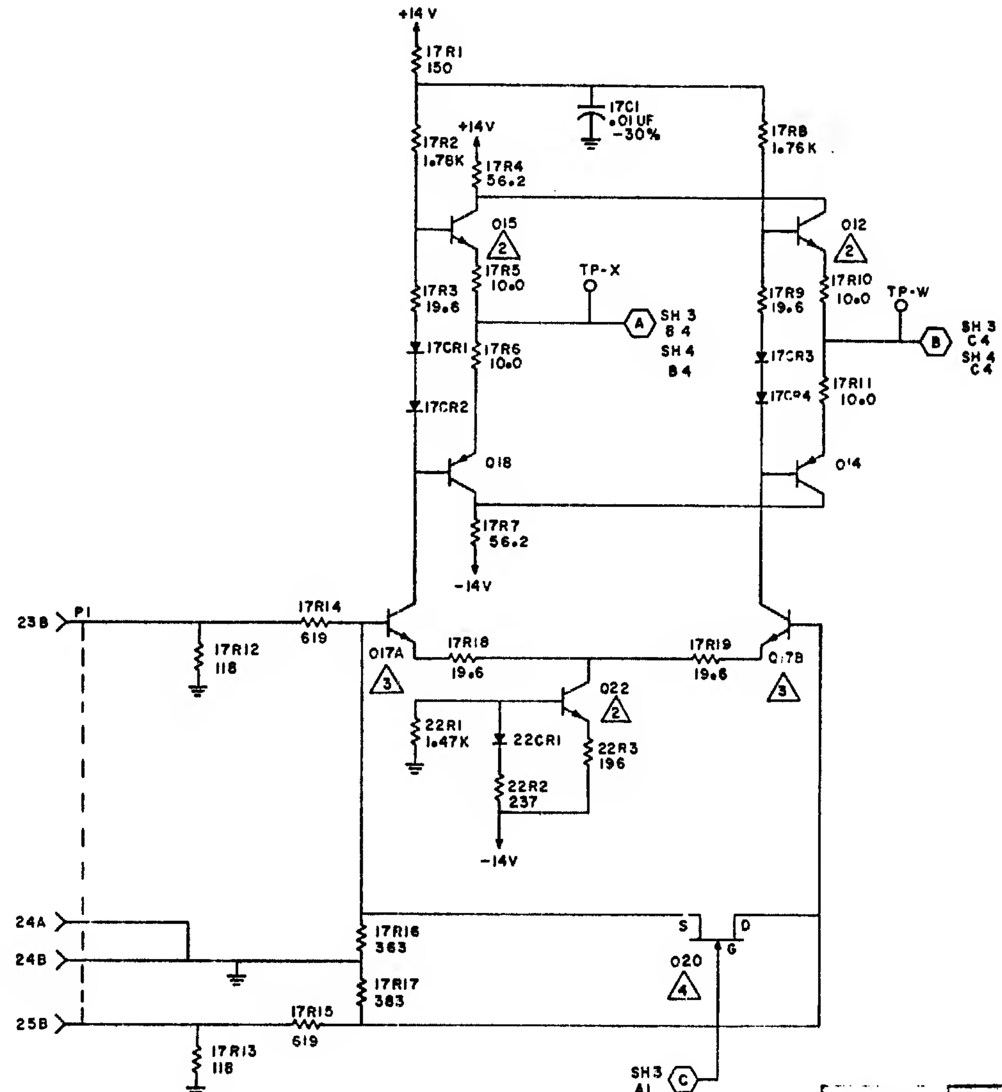
DWN	R. KONECNY	3-6-72
CHK	H. Hanson	3-22-72
ENGR		2-22-72
MFG		3-22-72
APPD		3-22-72

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 2FRV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54226203	5

SHEET 1 OF 4

HPD



REVISION RECORD						
		SEE SHT 1 FOR REV				

NORMANDALE DIVISION

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 2FRV

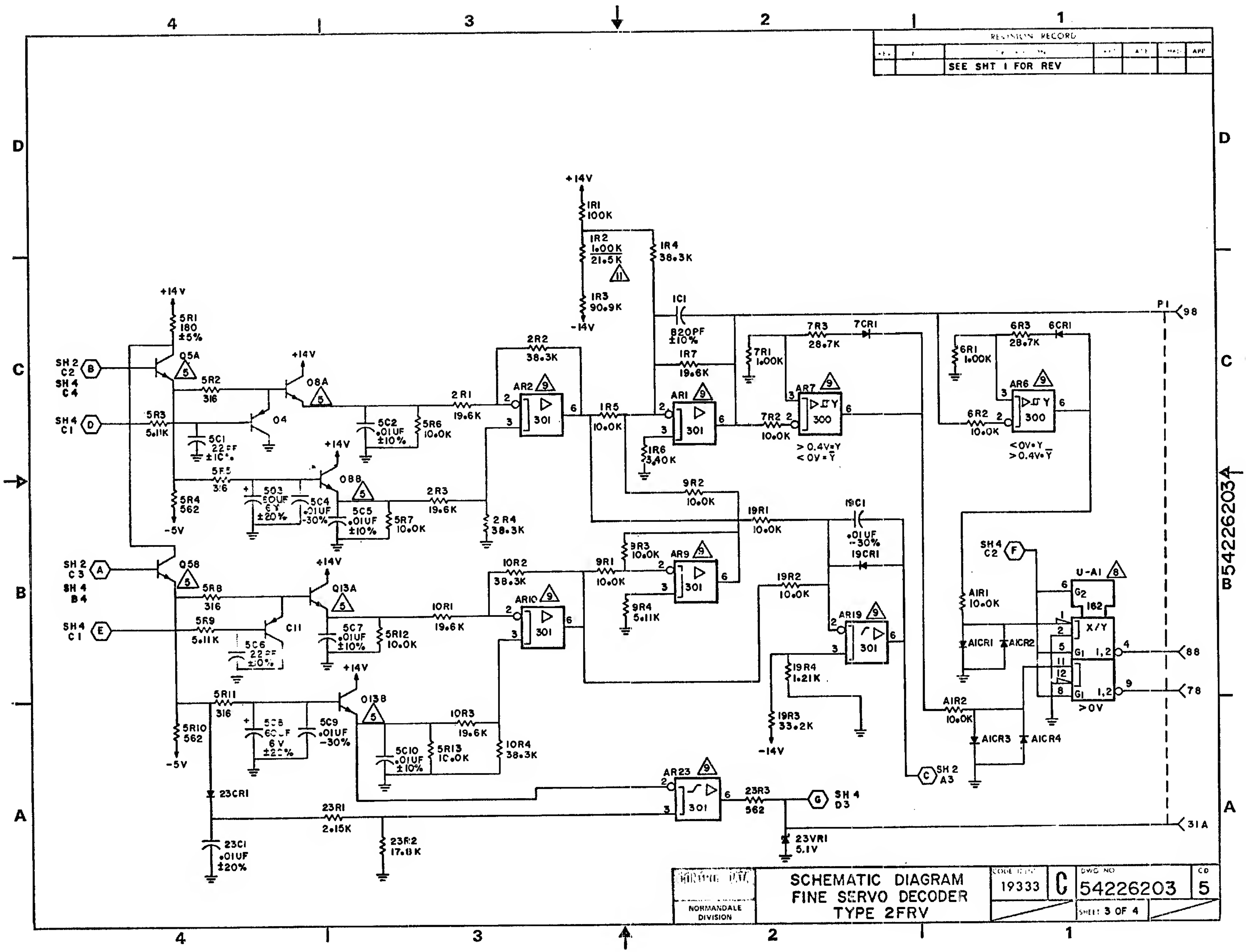
CODE IDENT 19333 | C | DWG NO 54226203 | ED 5

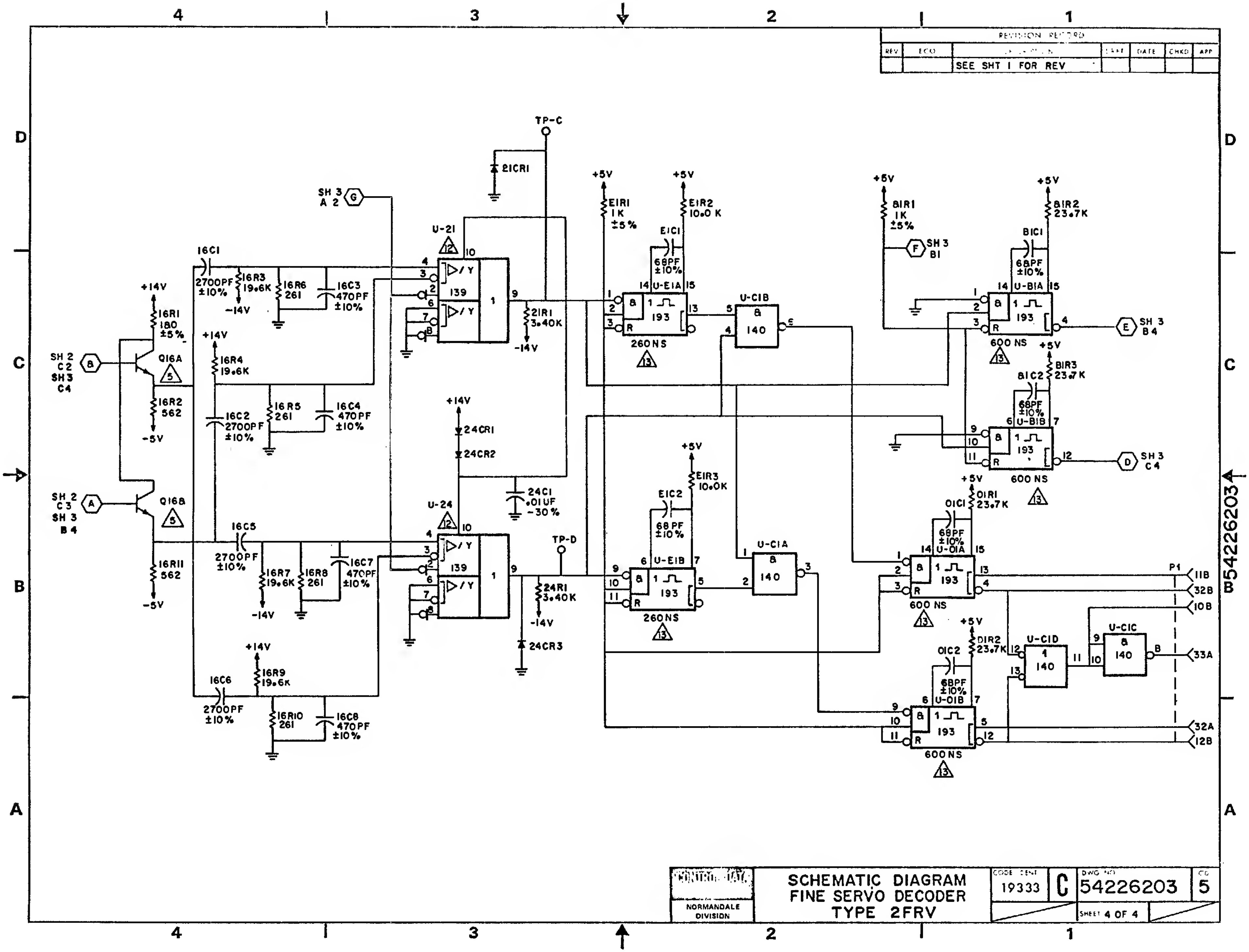
SHEET 2 OF 4

54226203

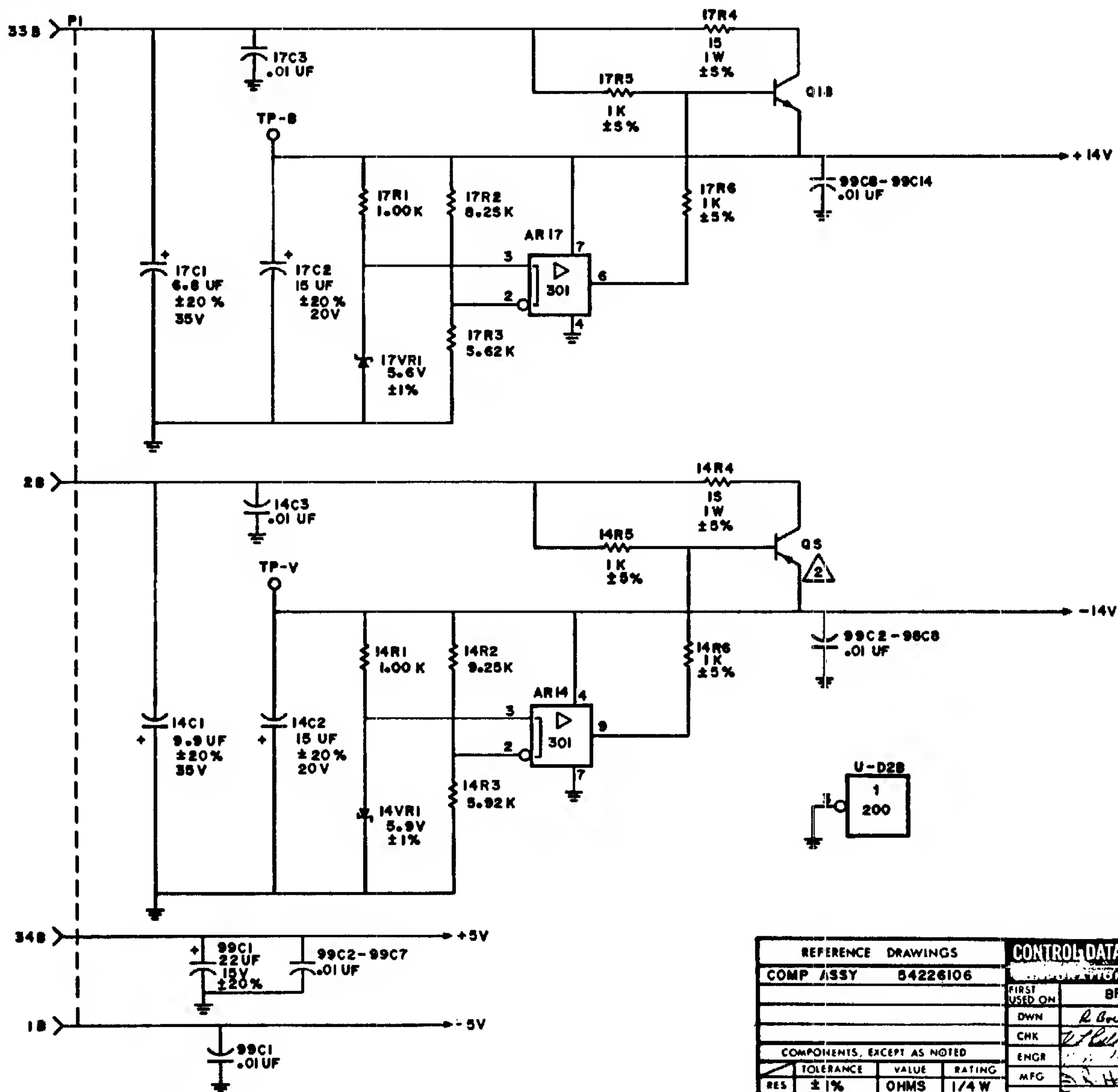
70629100 E

70629100 E


REVISION RECORD
SEE SHT 1 FOR REV
+14V
1R1 100K
1R2 1.00K 21.5K
1R3 90.9K
-14V
1R4 38.3K
1C1 820PF ±10%
1R7 19.6K
1R5 10.0K
1R6 3.40K
AR1
2R1 19.6K
2R2 38.3K
2R3 19.6K
2R4 38.3K
AR2
301
300
7R1 1.00K
7R2 10.0K
7R3 28.7K
7CR1
AR7
> 0.4V=Y
< 0V=Ȳ
6R1 1.00K
6R2 10.0K
6R3 28.7K
6CR1
AR6
<0V=Y
>0.4V=Ȳ
P1 98
SH 2 C2
SH 4 C4
SH 4 C1
5R1 180 ±5%
Q5A
5R2 316
Q8A
Q4
5R3 5.11K
5C1 22PF ±10%
5C2 .01UF ±10%
5R6 10.0K
5R5 316
5C3 60UF 6V ±20%
5C4 .01UF -30%
Q8B
5C5 .01UF ±10%
5R7 10.0K
5R4 562
-5V
9R2 10.0K
19R1 10.0K
19C1 .01UF -30%
19CR1
9R3 10.0K
9R1 10.0K
AR9
9R4 5.11K
19R2 10.0K
AR19
19R4 1.21K
19R3 33.2K
SH 4 C2
U-A1
G2
162
X/Y
G1
1,2
>0V
A1R1 10.0K
A1CR1
A1CR2
A1R2 10.0K
A1CR3
A1CR4
88
78
SH 2 C3
SH 4 B4
Q5B
5R8 316
Q13A
10R1 19.6K
10R2 38.3K
AR10
5R9 5.11K
C11
5C6 22PF ±10%
5C7 .01UF ±10%
5R12 10.0K
5R11 316
Q13B
5C8 60UF 6V ±20%
5C9 .01UF -30%
5R10 562
10R3 19.6K
10R4 38.3K
5C10 .01UF ±10%
5R13 10.0K
SH 2 A3
23CR1
AR23
23R1 2.15K
23R2 17.8K
23C1 .01UF ±20%
23R3 562
SH 4 D3
23VR1 5.1V
31A
54226203A
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 2FRV
19333
C
54226203
5
SHEET 3 OF 4

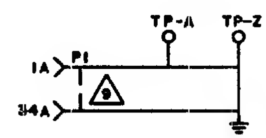

REVISION RECORD
SEE SHT 1 FOR REV
TP-C
TP-D
U-21
U-24
139
U-E1A
U-E1B
U-C1A
U-C1B
U-C1C
U-C1D
U-B1A
U-B1B
U-01A
U-01B
193
140
260 NS
600 NS
Q16A
Q16B
2700PF ±10%
470PF ±10%
68PF ±10%
+14V
-14V
+5V
-5V
P1
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 2FRV
CODE IDENT 19333
C
DWG NO 54226203
5
SHEET 4 OF 4
54226203

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, TIP 29, 50221800.
   ALL DIODES SILICON PLANAR, 24553500.
   ALL ZENER DIODE VOLTAGE TOLERANCES ±5%
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. TRANSISTOR, SPNP, TIP 30, 50221900.
3. DELAY TIME FOR REF ONLY
4. IC, TYPE 139, HAS PIN 1 CONNECTED TO GND.
5. TRANSISTOR, N CHANNEL J FET, 2N5434, 50218302.
6. IC, TYPE 162 HAS PIN 13 CONNECTED TO -5V.
7. IC, TYPE 321S HAS PIN 12 CONNECTED TO GND.
8. IC'S, AR1, AR2, AR3, AR4, AR6, AR7 AND AR10 HAVE PIN 7 CONNECTED TO +14V AND PIN 4 CONNECTED TO -14V.
9. ALL UNUSED CONNECTOR PINS ARE GROUNDED.
10. TEST SELECT RESISTOR TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.



REFERENCE DRAWINGS		
COMP ASSY	54226106	
COMPONENTS, EXCEPT AS NOTED		
TOLERANCE	VALUE	RATING
RES ±1%	OHMS	1/4 W
CAP ±30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A6
DWN	R Burke 5-3-73
CHK	5-9-73
ENGR	5-9-73
MFG	5-9-73
APPR	

TITLE: SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 3FRV

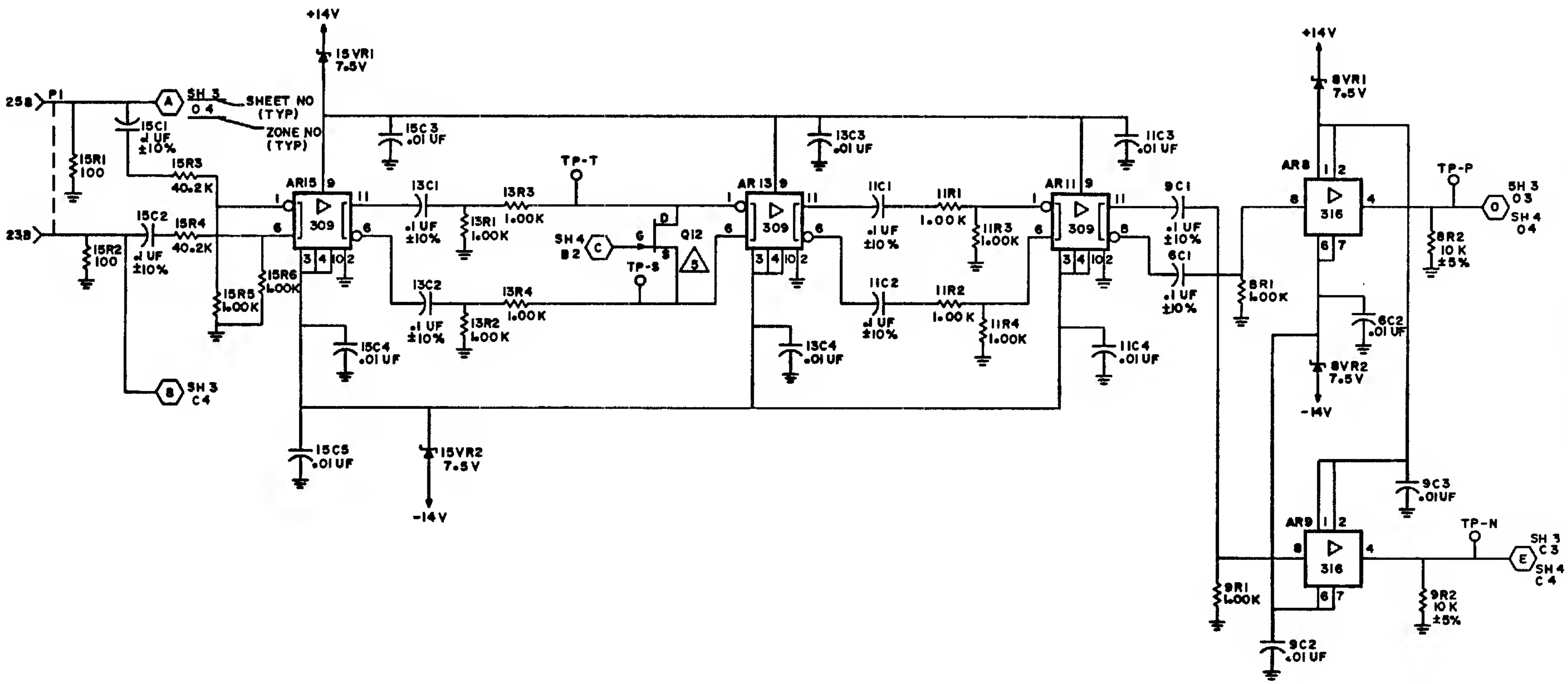
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54226206	8

SHEET 1 OF 4

54226206

HPD-E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

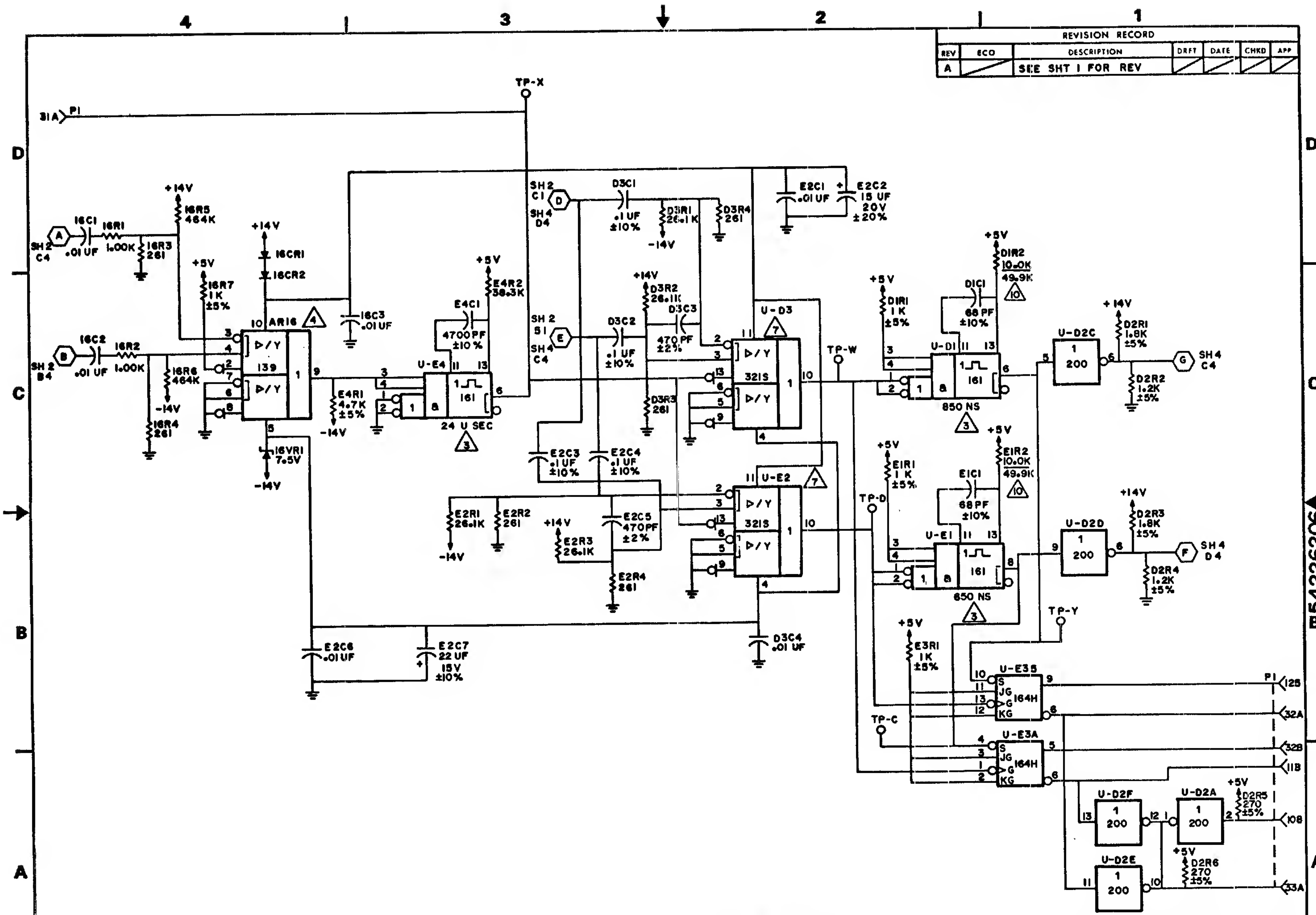


CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 3FRV	CODE IDENT 19333	C	DWG NO 54226206	CD 8
				SHEET 2	

54226206

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

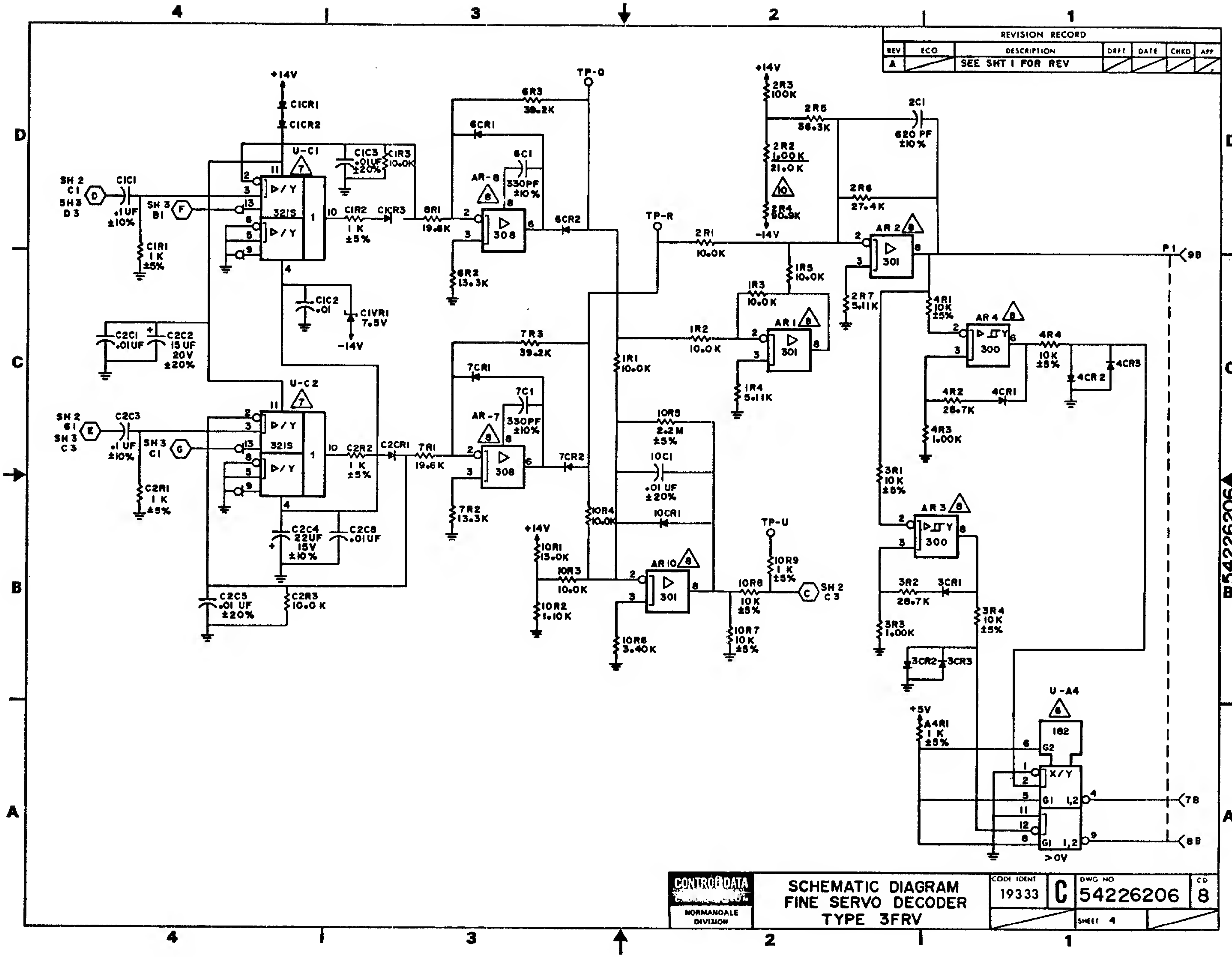


CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 3FRV

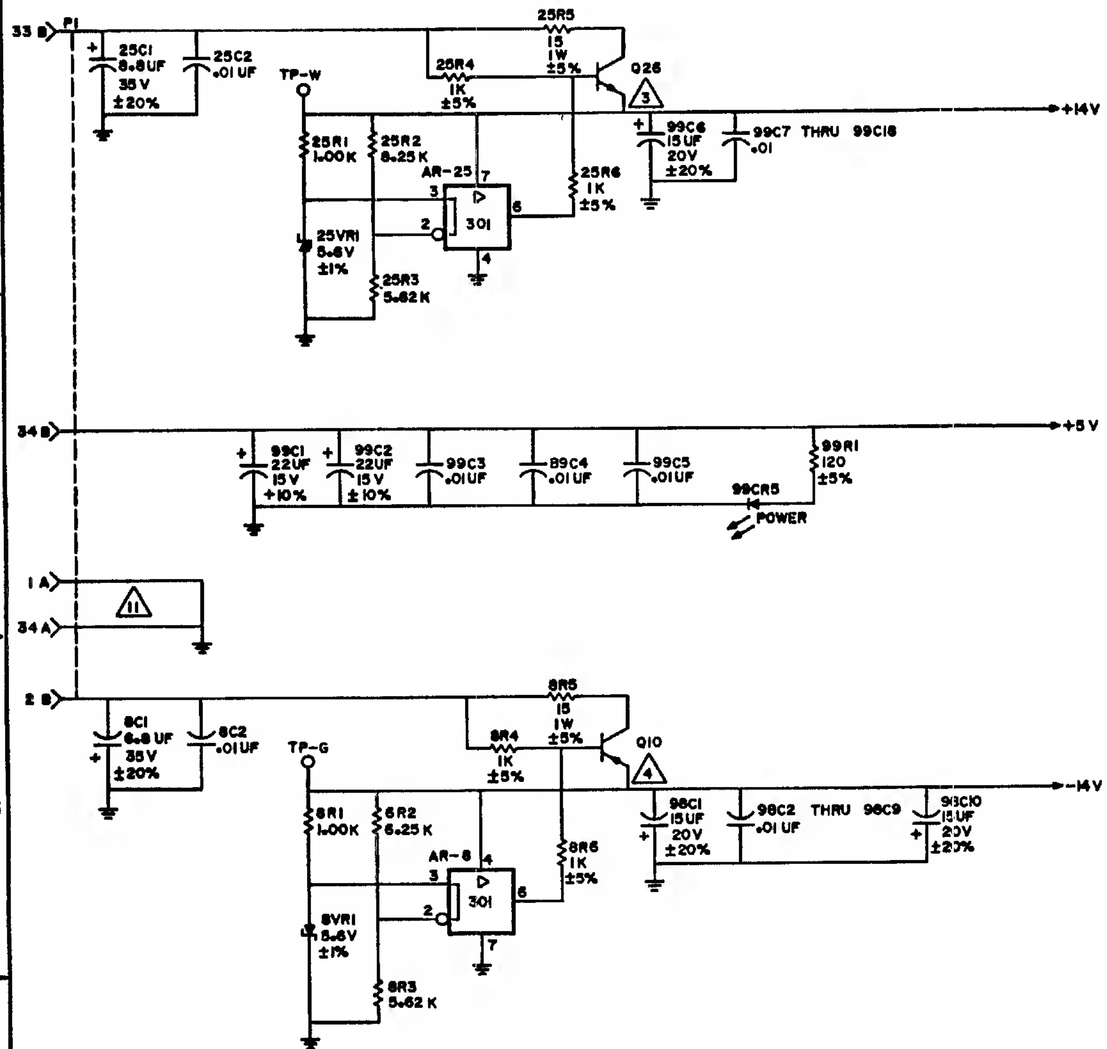
CODE IDENT	SIZE	DWG NO	CD
19333	C	54226206	8
		SHEET 3	

54226206


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHT 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 3FRV
CODE IDENT 19333
C
DWG NO 54226206
CD 8
SHEET 4
54226206
+14V
-14V
+5V
TP-Q
TP-R
TP-U
U-C1
U-C2
U-A4
321S
308
301
300
182
AR-8
AR-7
AR 1
AR 2
AR 3
AR 4
AR 10
SH 2 C1
SH 3 D3
SH 3 B1
SH 2 G1
SH 3 C3
SH 3 C1
SH 2 C3
P1
9B
7B
8B
C1C1 .1UF ±10%
C1R1 1K ±5%
C1R2 1K ±5%
C1R3 10.0K
C1C3 .01UF ±20%
C1C2 .01
C1VR1 7.5V
C2C1 .01UF
C2C2 15UF 20V ±20%
C2C3 .1UF ±10%
C2R1 1K ±5%
C2R2 1K ±5%
C2C4 22UF 15V ±10%
C2C8 .01UF
C2C5 .01UF ±20%
C2R3 10.0K
8R1 19.6K
6R3 39.2K
6C1 330PF ±10%
6R2 13.3K
7R1 19.6K
7R3 39.2K
7C1 330PF ±10%
7R2 13.3K
1R1 10.0K
1R2 10.0K
1R3 10.0K
1R4 5.11K
1R5 10.0K
2R1 10.0K
2R3 100K
2R5 36.3K
2R2 1.00K 21.0K
2R4 90.9K
2R6 27.4K
2R7 5.11K
2C1 620PF ±10%
4R1 10K ±5%
4R2 28.7K
4R3 1.00K
4R4 10K ±5%
3R1 10K ±5%
3R2 28.7K
3R3 1.00K
3R4 10K ±5%
10R1 13.0K
10R2 1.10K
10R3 10.0K
10R4 10.0K
10R5 2.2M ±5%
10C1 .01UF ±20%
10R6 3.40K
10R7 10K ±5%
10R8 10K ±5%
10R9 1K ±5%
A4R1 1K ±5%

70629100 E

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23500	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL TRANSISTORS, NFET, 2N5434, 50218302.
   ALL DIODES SILICON, 24553500.
2. TRANSISTOR, SNPN, 2N2221, 50210102.
3. TRANSISTOR, SNPN, POWER, 50221800.
4. TRANSISTOR, SPNP, POWER, 50221900.
5. DELAY TIMES FOR REFERENCE ONLY.
6. IC PACKAGE AR 3, 4, 5, 6, 16, 17, AND 18 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14 V.
7. TERMINAL NUMBERING FOR RELAY K11 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.
8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 1.00K TO 1.00M.
10. SPDT SWITCH.
11. CONNECTOR PINS 7B, 10B, 21B, 23B, 25B, AND 27B SHALL NOT BE USED. ALL OTHER PINS NOT OTHERWISE DESIGNATED ARE GND.

REFERENCE DRAWINGS			
COMP ASSY 54226502			
COMPONENTS EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

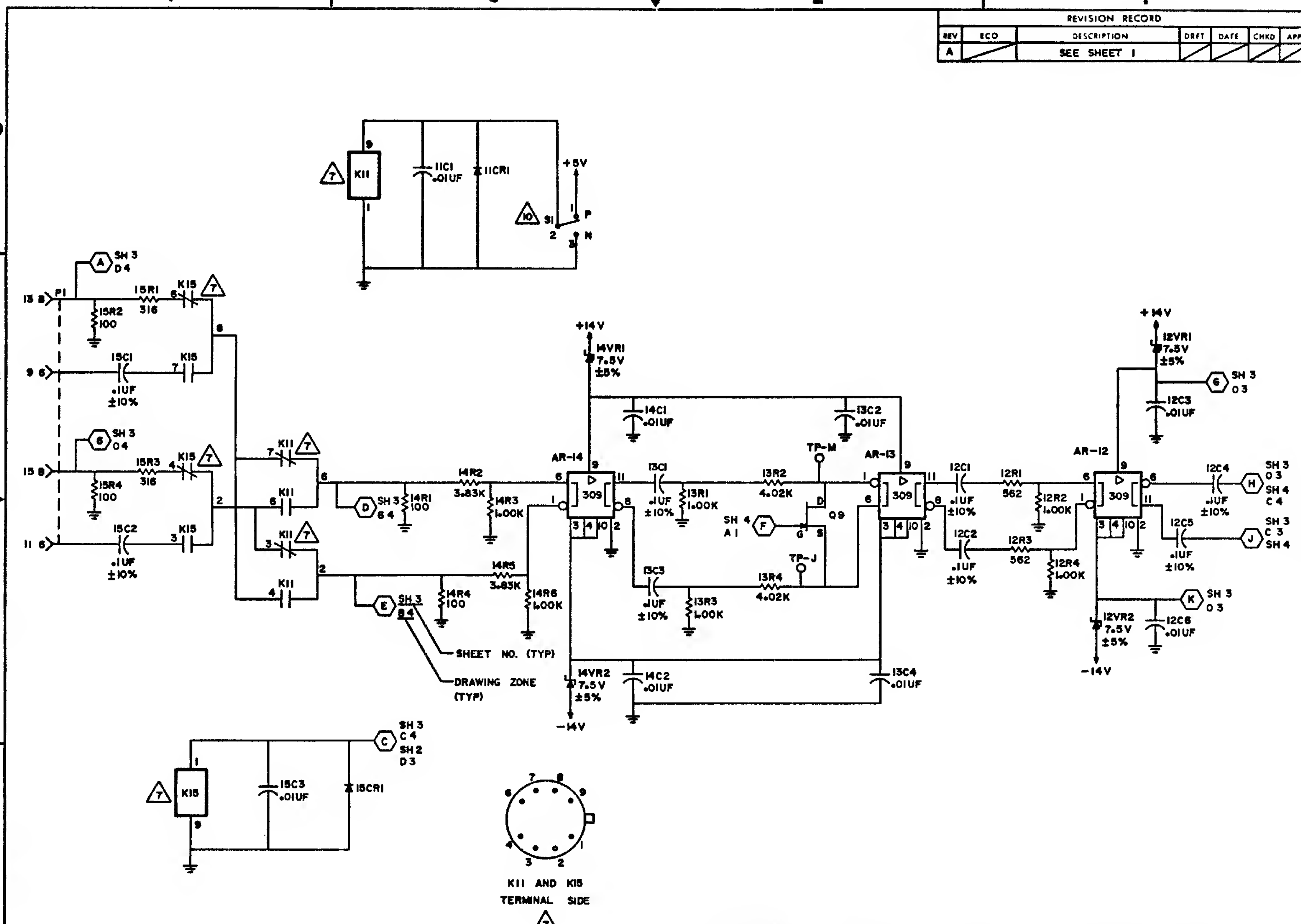
FIRST USED ON	BR3A3	
DWN	D. G. TUTTLE	9-9-72
CHK		
ENGR		9-27-72
MFG		9-9-72
APPR		

TITLE: SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE BFSV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54226602	8

SHEET 1 OF 4

4-100.2



CONTROL DATA
NORMANDALE DIVISION

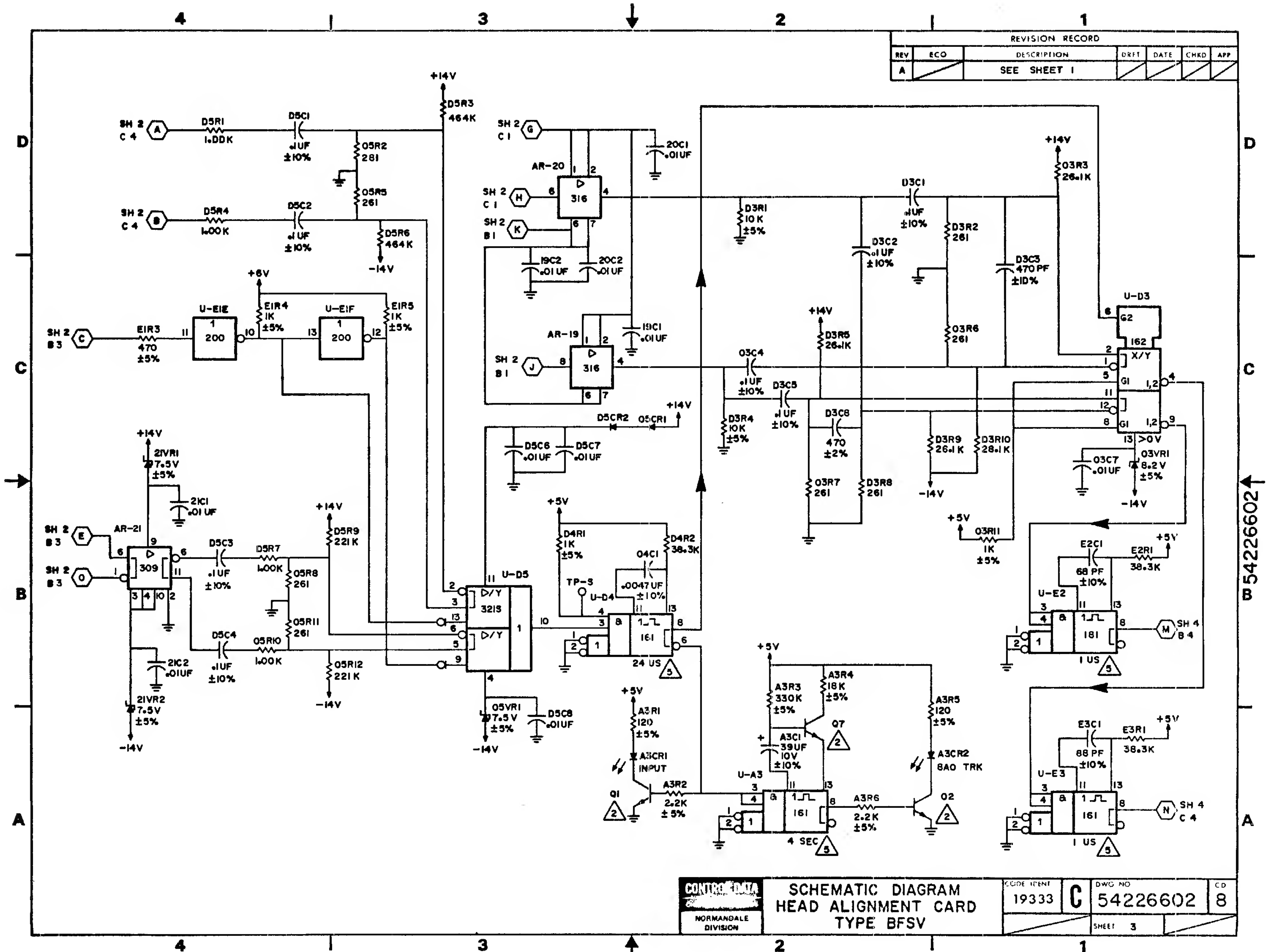
SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE BFSV

CODE IDENT		DWG NO	CD
19333	C	54226602	8
		SHEET 2	

54226602

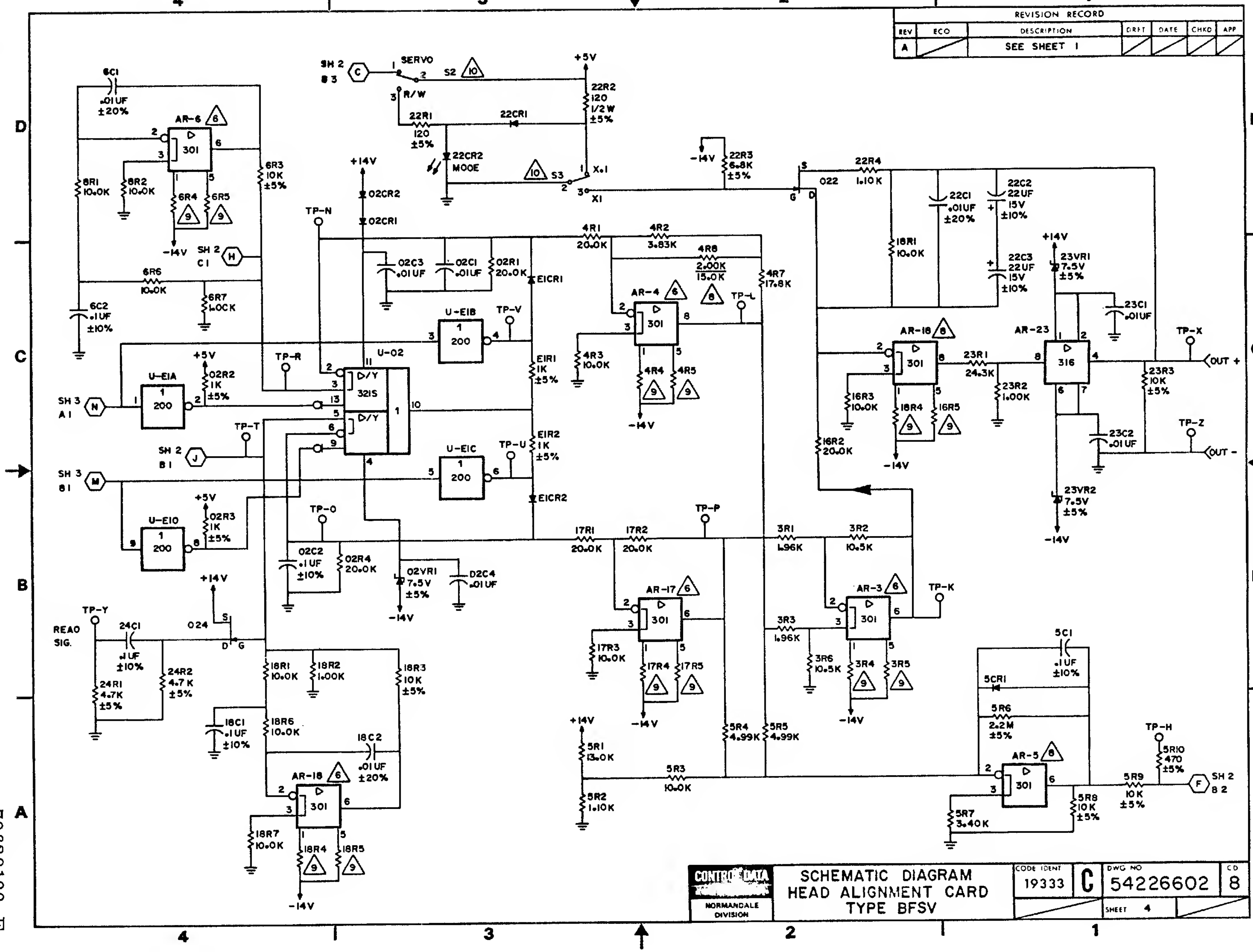
70629100 E

70629100 E



4-100.3

4-100.4



CONTROL DATA CORPORATION
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE BFSV

CODE IDENT		DWG NO	CD
19333	C	54226602	8
		SHEET 4	

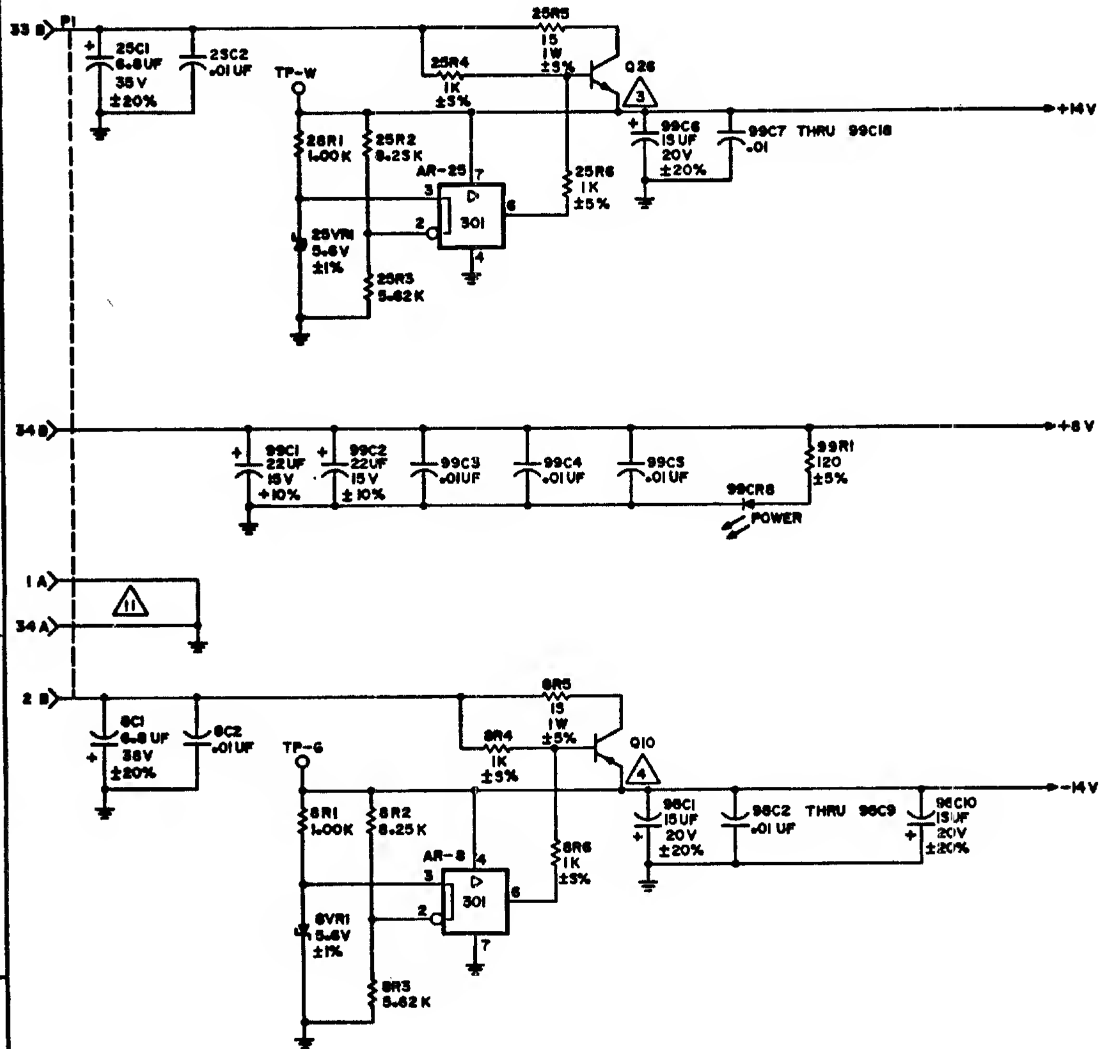
54226602

70629100 E

70629100 E

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	23030	RELEASED		[illegible]	[illegible]	[illegible]

SHEET REVISION STATUS



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL TRANSISTORS, NFET, 2N5434, 50218302.
   ALL DIODES SILICON, 24553500.

2. TRANSISTOR, SNPN, 2N2221, 50210102.

3. TRANSISTOR, SNPN, POWER, 50221800.

4. TRANSISTOR, SPNP, POWER, 50221900.

5. DELAY TIMES FOR REFERENCE ONLY.

6. IC PACKAGE AR 3, 4, 5, 6, 18, 17, AND 18 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14 V.

7. TERMINAL NUMBERING FOR RELAY K11 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.

8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.

9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 1.00K TO 1.00M.

10. SPDT SWITCH.

11. CONNECTOR PINS 7B, 10B, 21B, 23B, 25B, AND 27B SHALL NOT BE USED. ALL OTHER PINS NOT OTHERWISE DESIGNATED ARE GND

12. NO CONNECTIONS.

54226604

REFERENCE DRAWINGS			
COMP ASSY 54228604			
COMPONENTS EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

APPLICATION	BR3A3	
DWN	V.B. WILSON	7-16-73
CHK	[illegible]	7-19-73
ENG	[illegible]	7-19-73
MFG	[illegible]	7-27-73
APPR	[illegible]	7-25-73

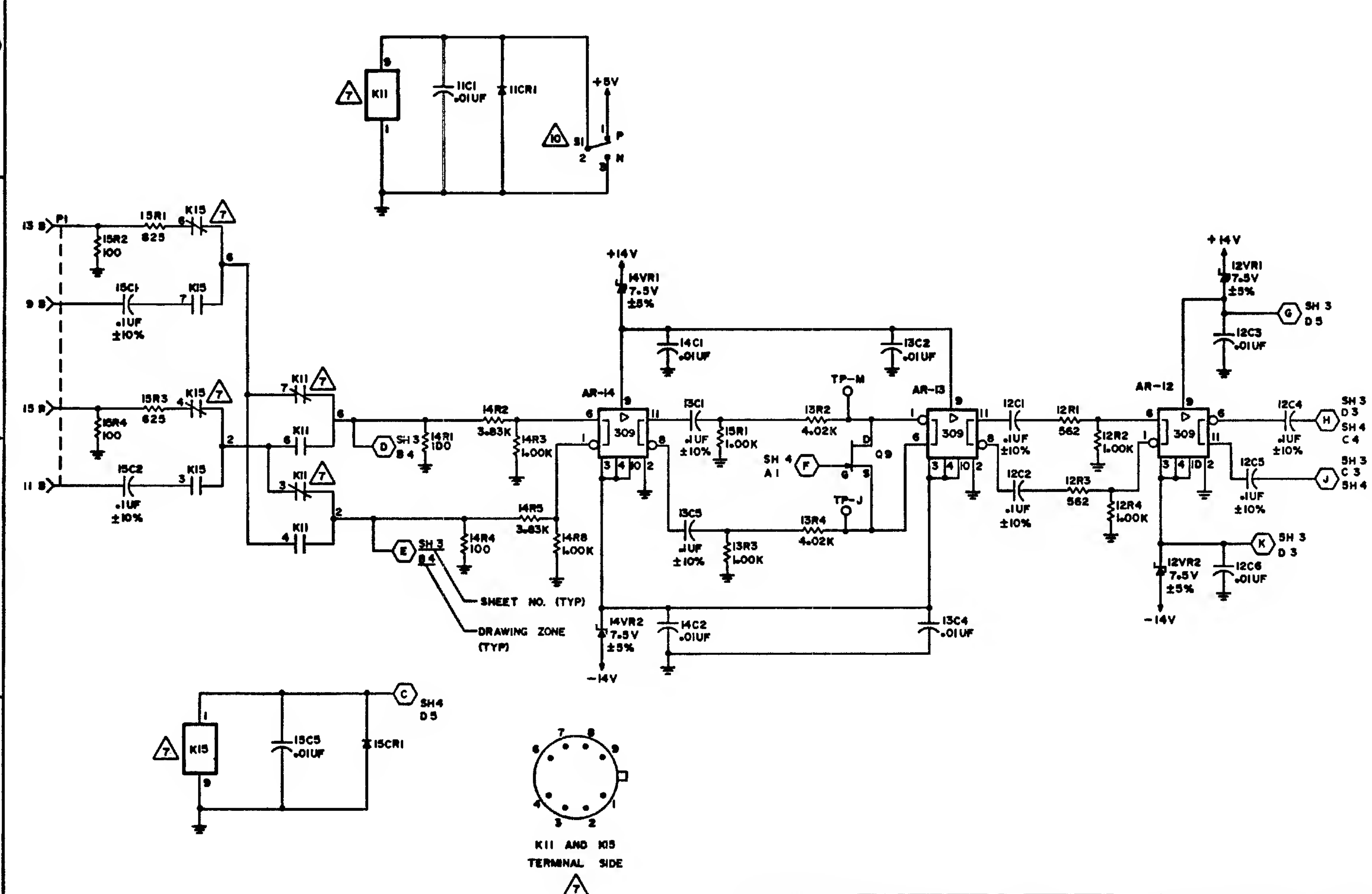
TITLE: SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE CFSV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54226604	4

SHEET 1 OF 4

HPD-E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

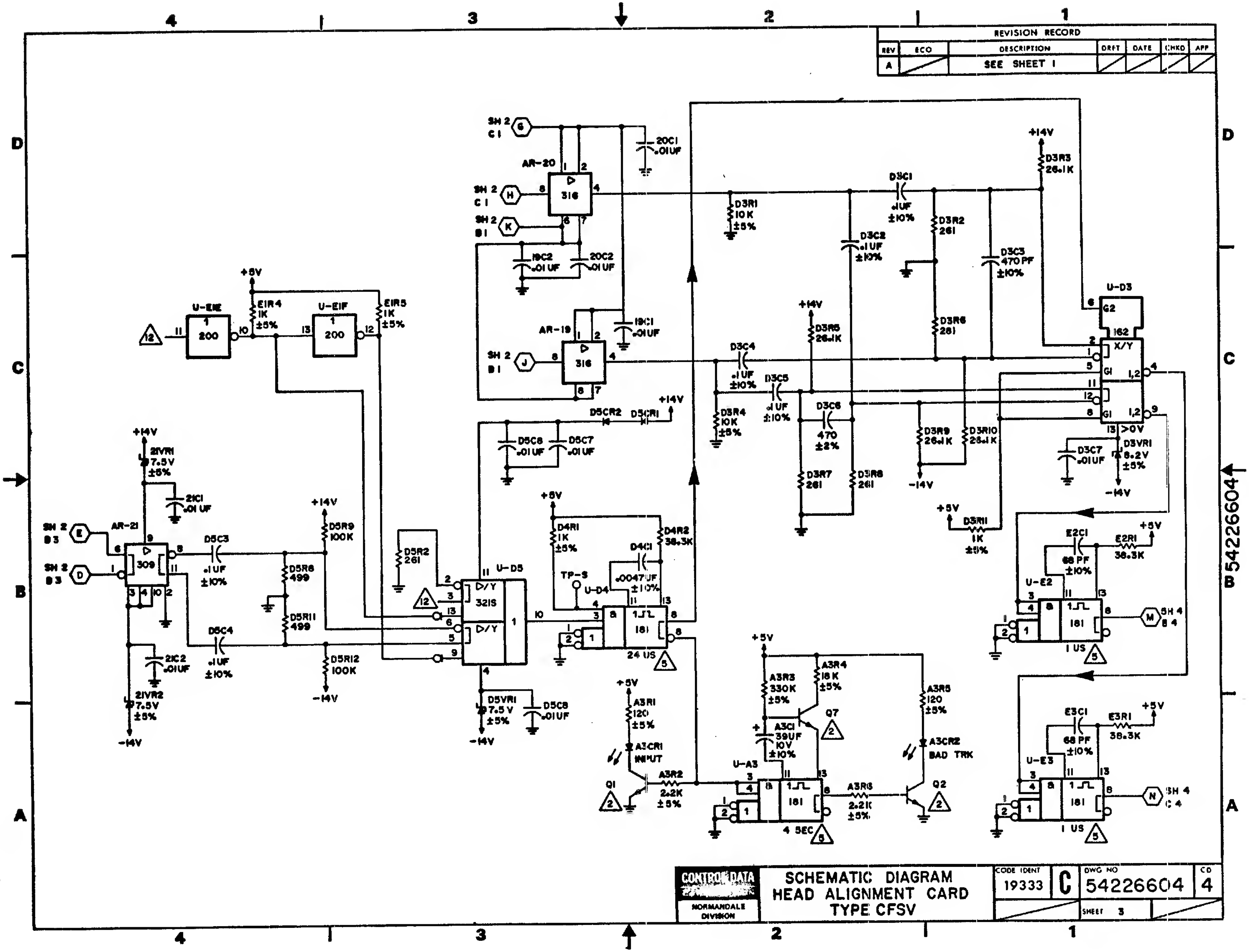


CONTROL DATA NORMANDALE DIVISION

SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE CFSV

CODE IDENT		DWG NO	CD
19333	C	54226604	4
		SHEET 2	

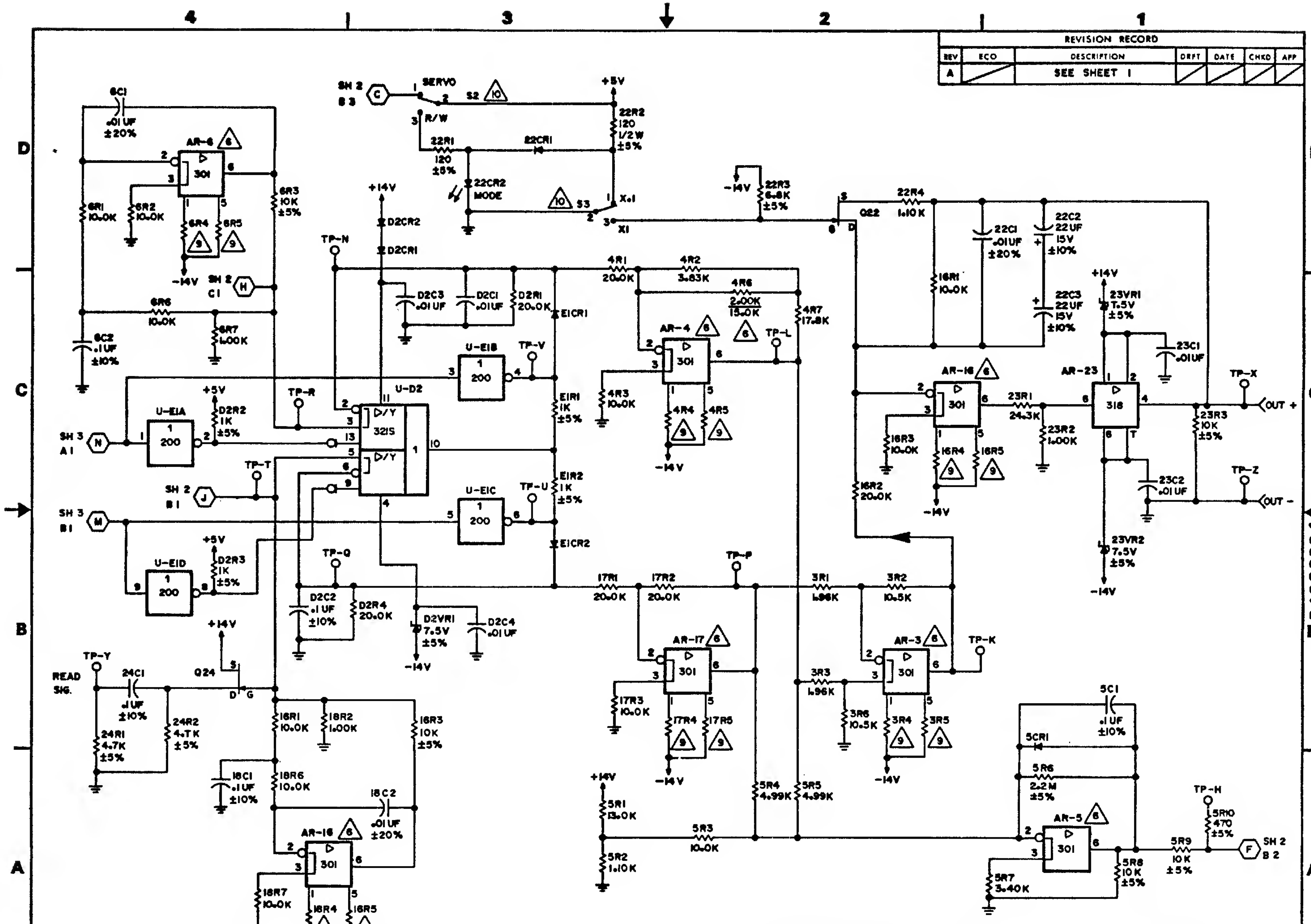
70629100 E



4-100.7

4-100.8

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

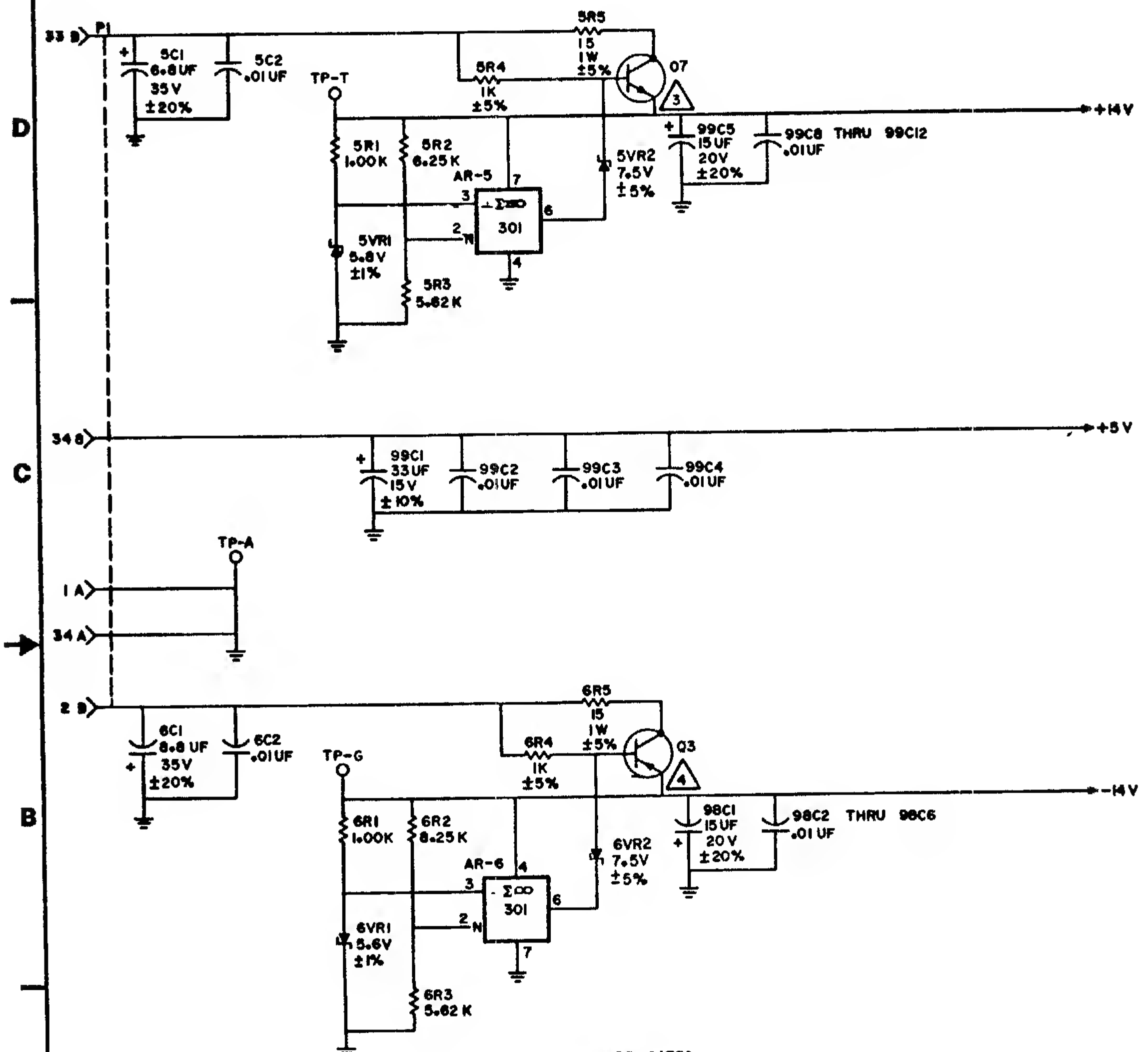


CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE CFSV	CODE IDENT 19333	C	DWG NO 54226604	CD 4
				SHEET 4	

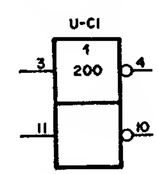
54226604

70629100 E

70629100 G



SPARE GATES



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A		RELEASED				

REVISION RECORD

NOTE.

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V EXCEPT U-B1.
   ALL TRANSISTORS, JFET, 50218302.
   ALL DIODES SILICON, 24553500.

2. TRANSISTOR, JFET, 50218100.
3. TRANSISTOR, SNPN, POWER, 50221800.
4. TRANSISTOR, SPNP, POWER, 50221900.
5. DELAY TIMES FOR REFERENCE ONLY.
6. IC PACKAGE U-A1, U-A3, AND U-A5 HAVE PIN 4 CONNECTED TO -14V AND PINS 9 AND 13 CONNECTED TO +14V.
7. TERMINAL NUMBERING FOR RELAY K14 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.
8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 2.00K TO 100K.
10. TOGGLE SWITCH, 94263907.
11. TRANSISTOR, SPNP, 2N4916, 50211610.
12. IC PACKAGE AR-1 HAS PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
13. IC PACKAGE U-C3 HAS PIN 6 CONNECTED TO -14V AND PIN 11 CONNECTED TO +14V.
14. TRANSISTOR, SNPN, 2N3569, 50210811.

54226606

REFERENCE DRAWINGS
COMP ASSY 54226506

COMPONENTS EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON: BR3B9A/B

DWN 3-7-74 · CHK · ENGR · MFG · APPR

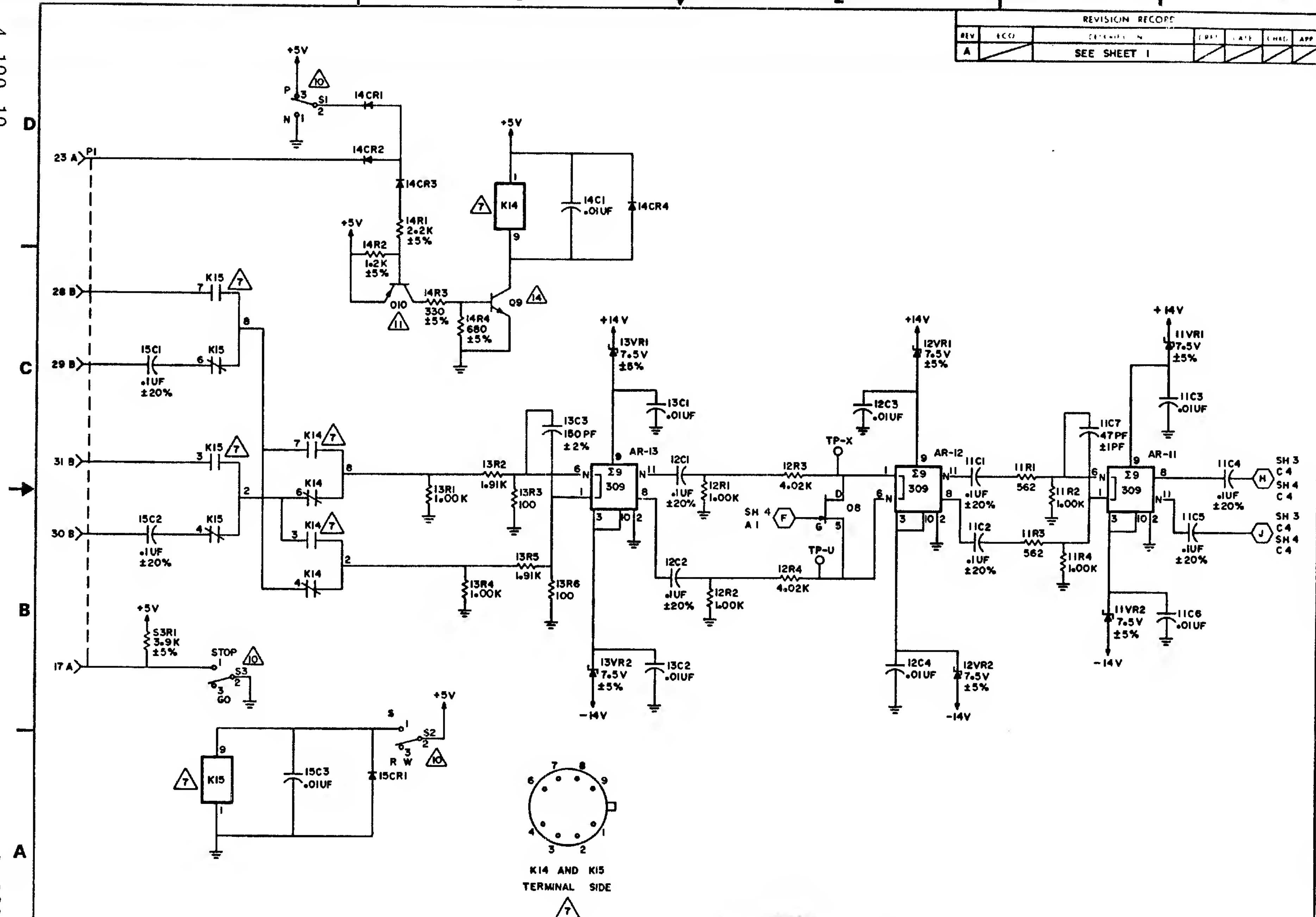
TITLE

SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54226606	9

SHEET 1 OF 4

4-100.10



54226606

NORMANDALE DIVISION

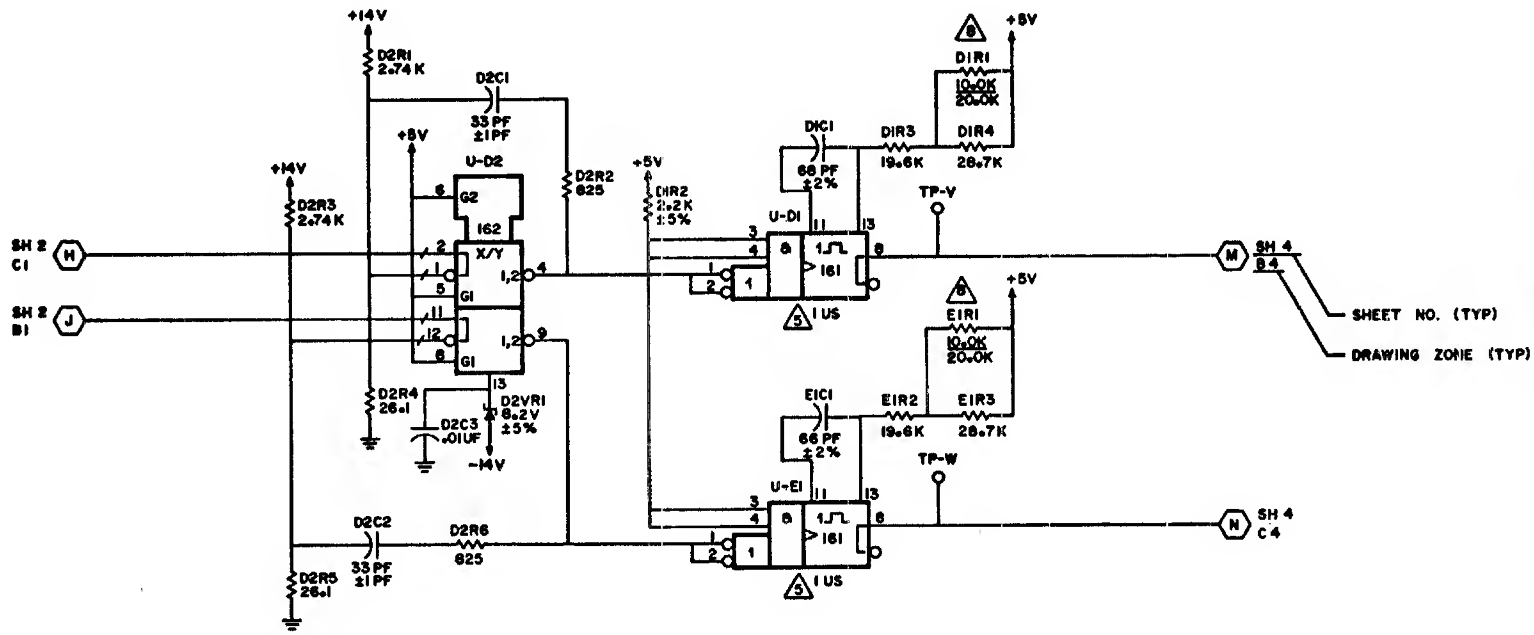
SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE EFSV

CODE IDENT		DWG NO	CD
19333	C	54226606	9
		SHEET 2	

70629100 G

70629100 G

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

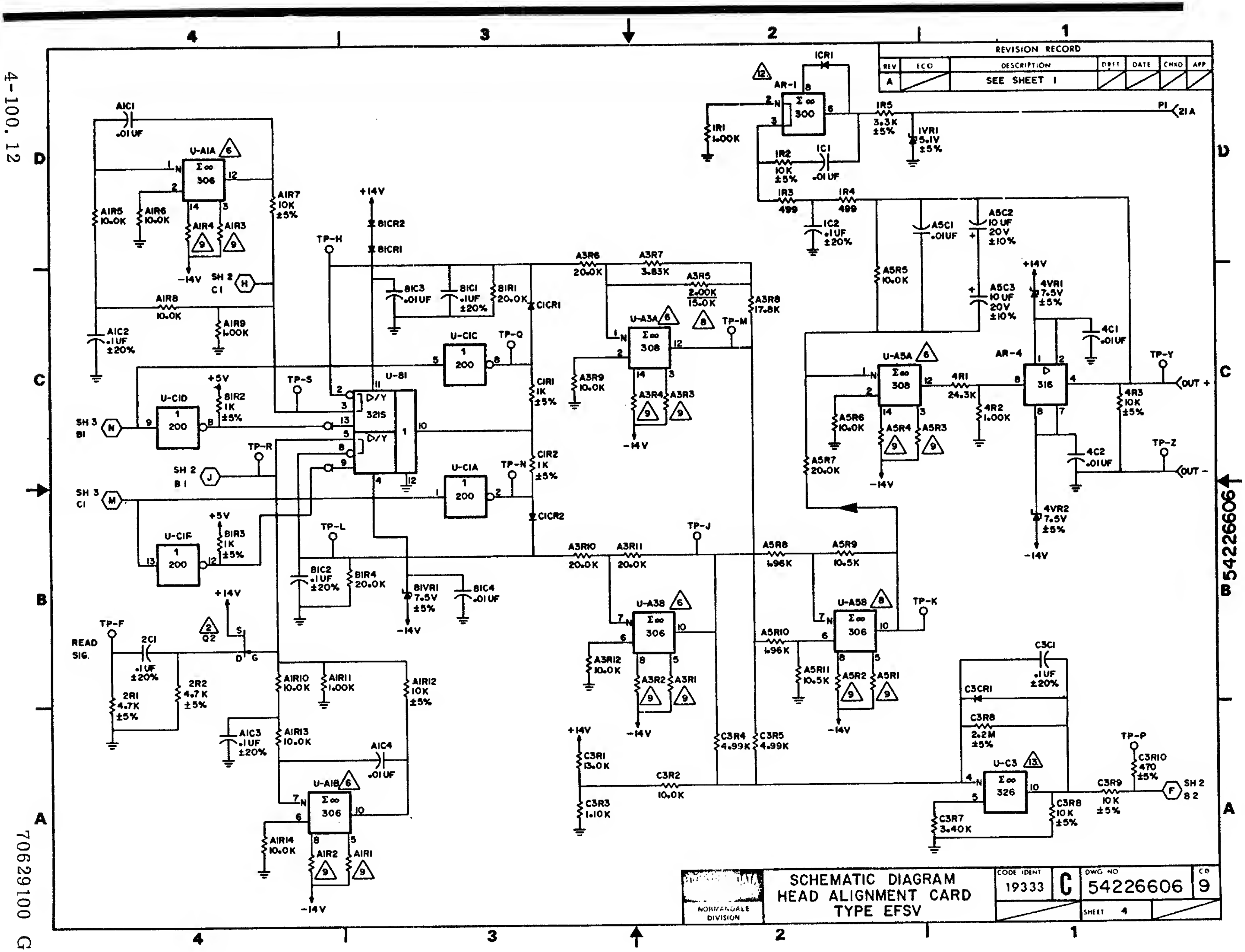


54226606

NORMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV	CODE IDENT 19333	C	DWG NO 54226606 · CD 9 · SHEET 3

4-100.11

4-100.12



NORMANDALE DIVISION

SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE EFSV

CODE IDENT		DWG NO	CD
19333	C	54226606	9

SHEET 4

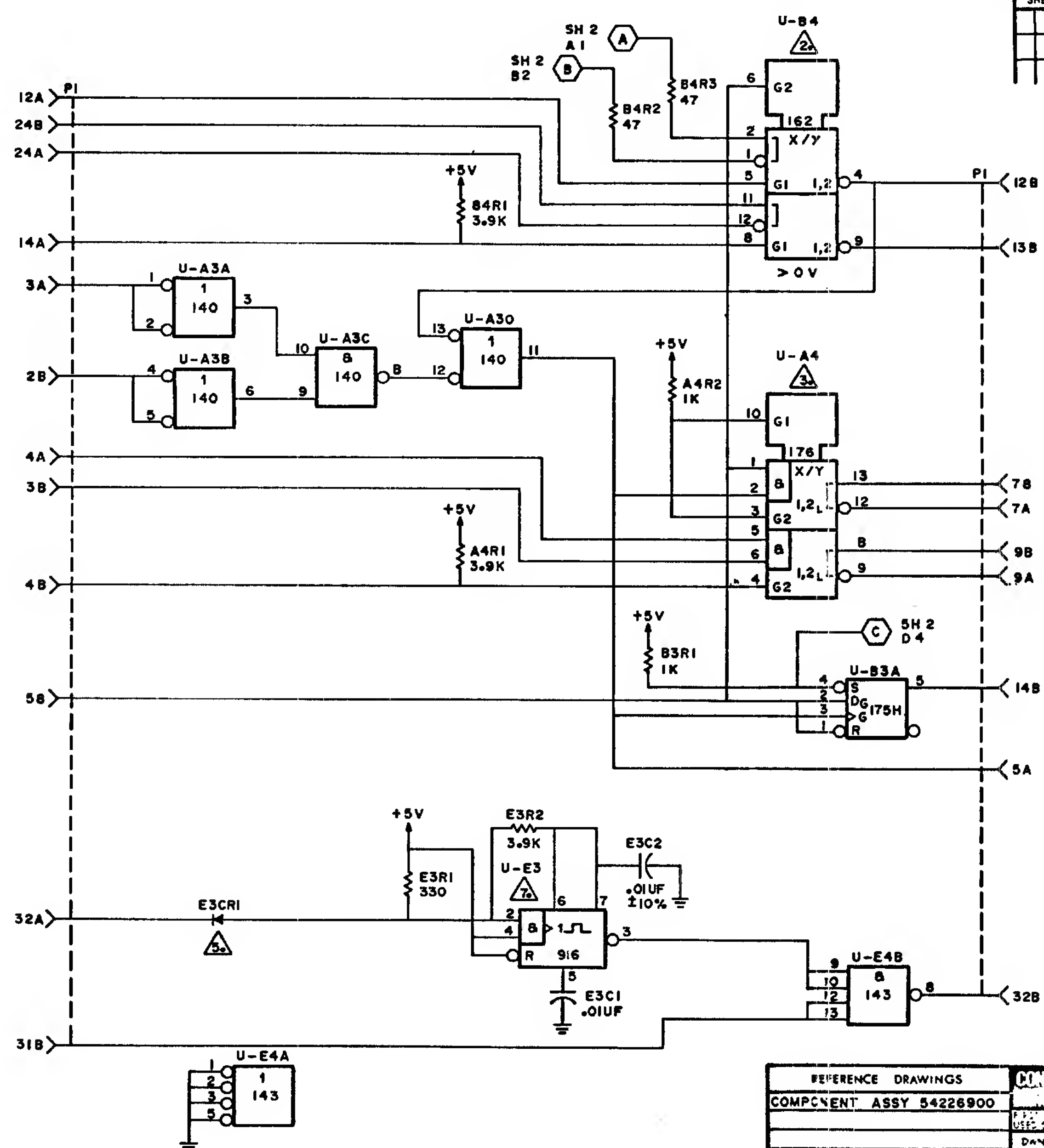
54226606

70629100 G

SHEET REVISION STATUS									

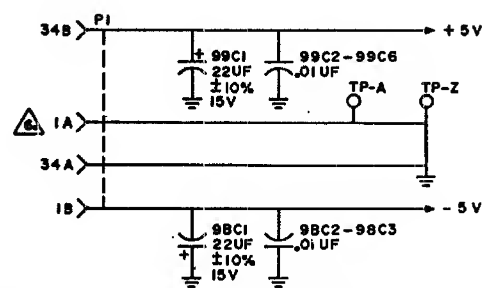
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23066	RELEASED		2-27-73		
B	PE34180	CHANGE NOTE 6	RB	3-22-73		



NOTES:

1. UNLESS OTHERWISE SPECIFIED;
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
   ALL TRANSISTOR'S ARE SPNP, 2N4258, 50211510.
   ALL DIODES, SILICON, 92115021.
2. IC B4 HAS PIN 13 CONNECTED TO -5V.
3. IC A4 HAS PIN 11 CONNECTED TO -5V.
4. TRANSISTORS, SNPN, 2N3646, 50210310.
5. DIODE, GERMANIUM, 11801200.
6. CONNECTOR PINS 8A, 8B, 10A, 10B, 27A, 27B, 30A, AND 31A ARE GROUNDED.
7. IC E3 HAS PIN 1 CONNECTED TO GND AND PIN 8 CONNECTED TO +5V.



54227000

REFERENCE DRAWINGS
COMPONENT ASSY 54226900

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHM	1/4 W
CAP	±30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

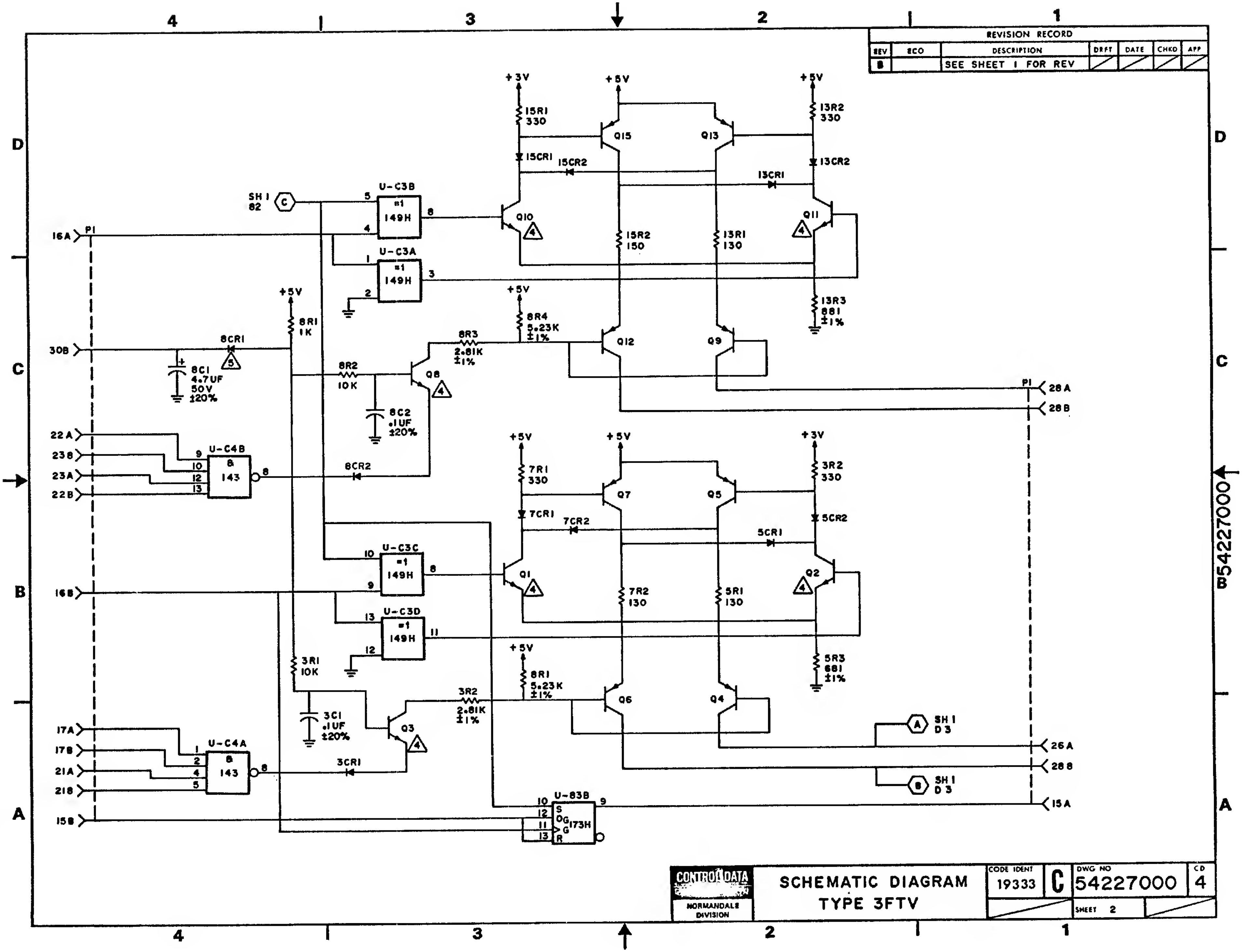
USED ON	BR501	
DRN	R. KONECNY	2-16-73
CHK		
ENGR		2-22-73
MFG		2-23-73
APPR		

TITLE: SCHEMATIC DIAGRAM DATA, CLOCK-XMITR & RCVR TYPE 3FTV

CODE IDENT	SIZE	DRAWING NUMBER	CO
19333	C	54227000	4

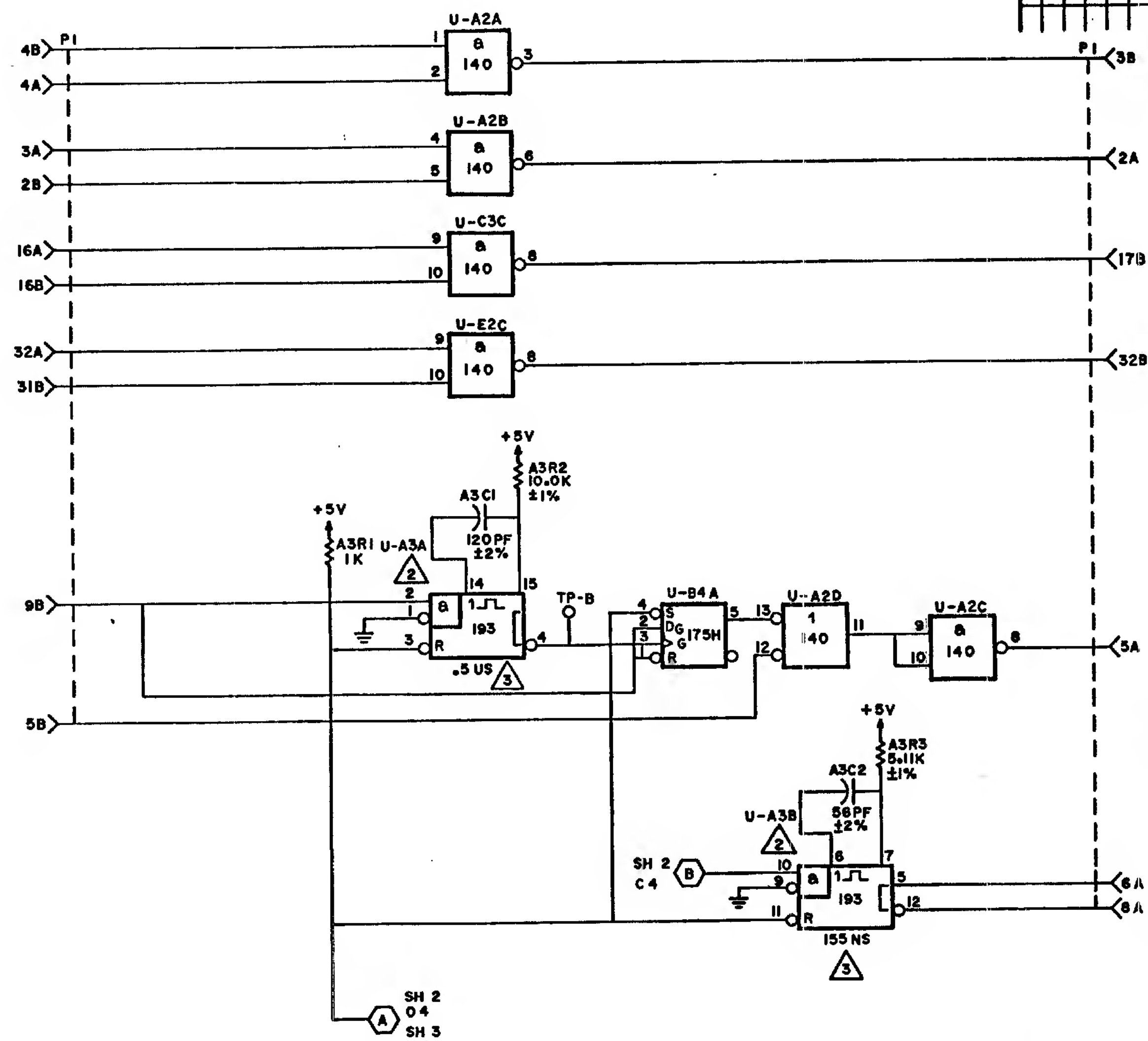
SHEET 1 OF 2

HPD-E



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
B | SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 3FTV
CODE IDENT 19333
C
DWG NO 54227000
CD 4
SHEET 2
54227000

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	FE23000	RELEASED		6-1-72		RTR

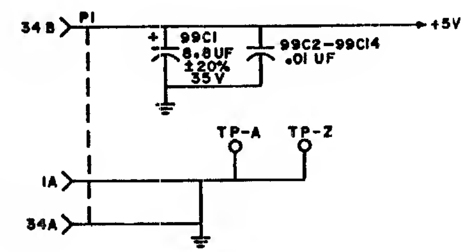


NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.

3. DELAY TIME FOR REFERENCE.



54227402

REFERENCE DRAWINGS	
COMP ASSY 54227302	

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

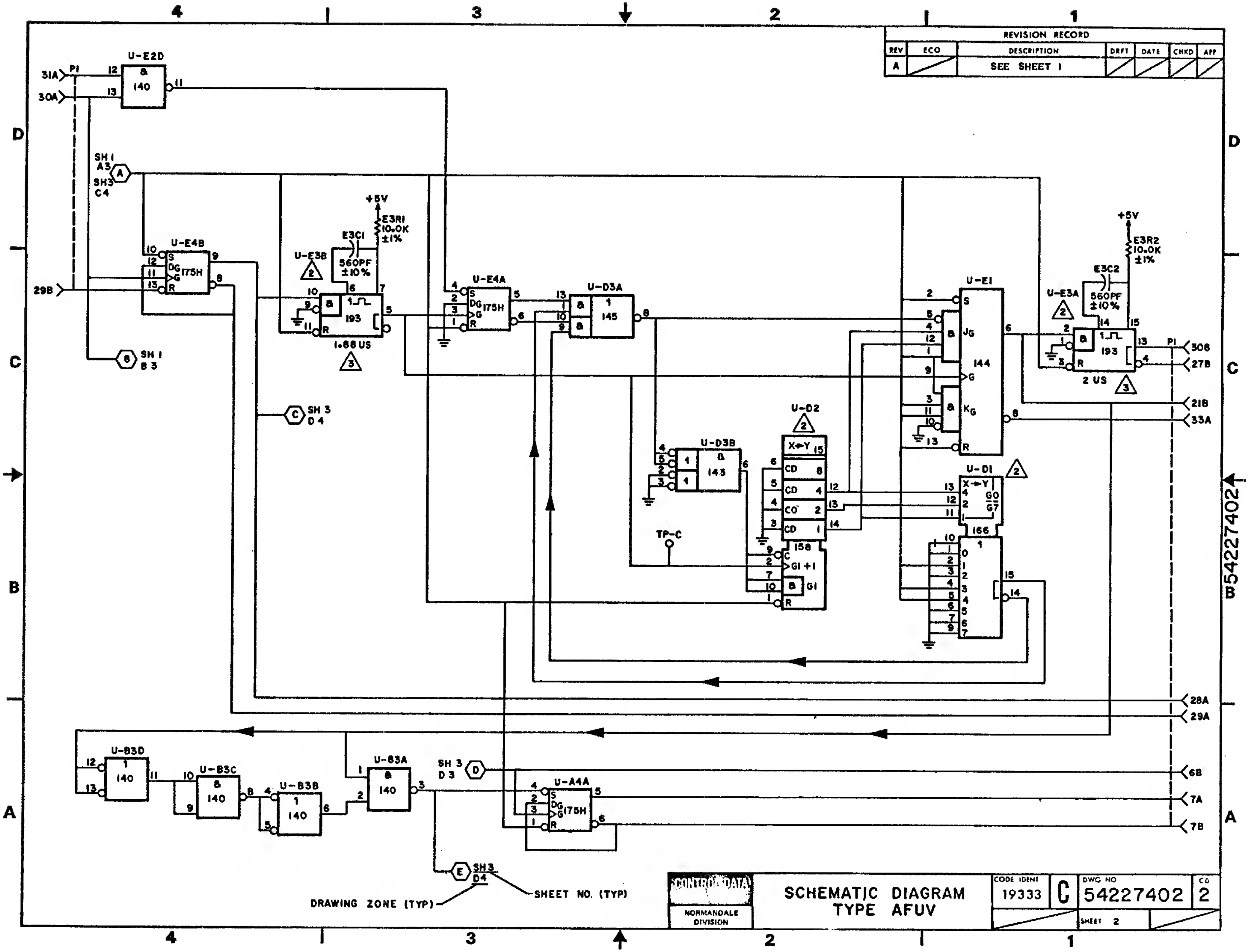
FIRST USED ON	BR3A4	
DWN	O. G. TUTTLE	3-30-72
CHK		5-9-72
ENGR		5-12-72
MFG		
APPR		5/1/72

TITLE
SCHEMATIC DIAGRAM
INDEX DETECT
& SECTOR GENERATOR
TYPE AFUV

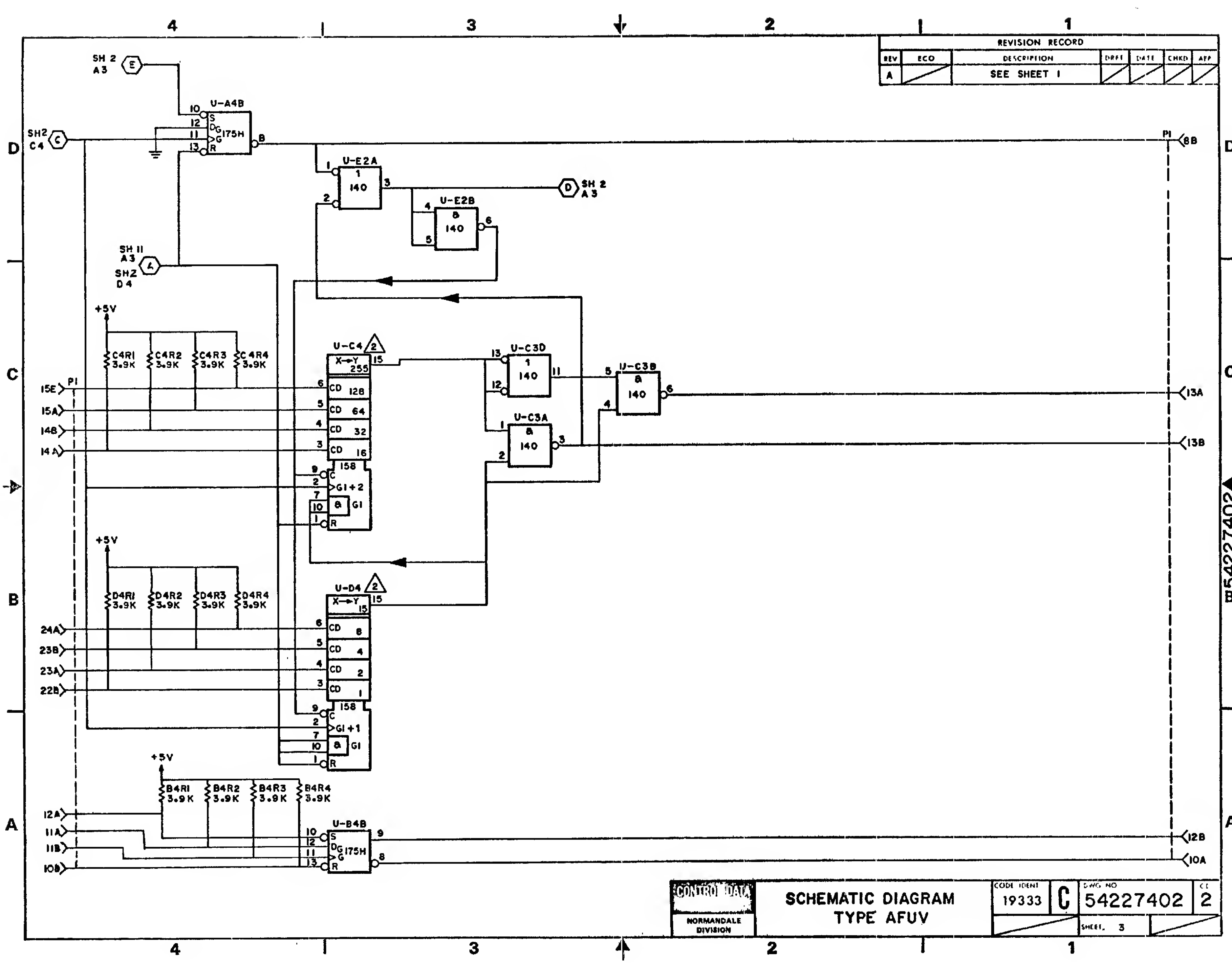
CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54227402	2

SHEET 1 OF 3

HPD

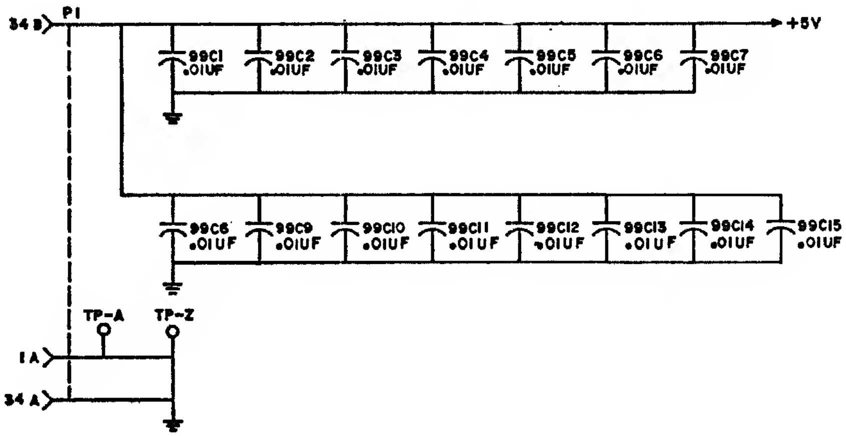

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
U-E2D
U-E4B
U-E3B
U-E4A
U-D3A
U-E1
U-E3A
U-D3B
U-D2
U-D1
U-B3D
U-B3C
U-B3B
U-B3A
U-A4A
E3C1 560PF ±10%
E3R1 10.0K ±1%
E3C2 560PF ±10%
E3R2 10.0K ±1%
+5V
1.88 US
2 US
TP-C
SH 1 A3
SH3 C4
SH 1 B 3
SH 3 D 4
SH 3 D 3
SH3 D4
31A
30A
29B
30B
27B
21B
33A
28A
29A
6B
7A
7B
DRAWING ZONE (TYP)
SHEET NO. (TYP)
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM TYPE AFUV
CODE IDENT 19333
C
DWG NO 54227402
CD 2
SHEET 2

54227402



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
SH 2 A3
SH2 C4
U-A4B
175H
U-E2A
140
U-E2B
SH 2 A3
SH 11 A3
SH2 D4
+5V
C4R1 3.9K
C4R2 3.9K
C4R3 3.9K
C4R4 3.9K
U-C4
X→Y 255
CD 128
CD 64
CD 32
CD 16
158
G1+2
G1
U-C3D
U-C3A
U-C3B
15E
15A
14B
14A
P1
13A
13B
8B
D4R1 3.9K
D4R2 3.9K
D4R3 3.9K
D4R4 3.9K
U-D4
X→Y
CD 8
CD 4
CD 2
CD 1
G1+1
24A
23B
23A
22B
B4R1 3.9K
B4R2 3.9K
B4R3 3.9K
B4R4 3.9K
U-B4B
175H
12A
11A
11B
10B
12B
10A
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE AFUV
CODE IDENT 19333
C
DWG NO 54227402
2
SHEET 3
54227402

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
3. DELAY TIME FOR REFERENCE.

54227404

REFERENCE DRAWINGS	
COMP ASSY 54227304	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	−30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	D. G. TUTTLE	10-5-72
CHK		
ENGR		
MFG		
APPR		

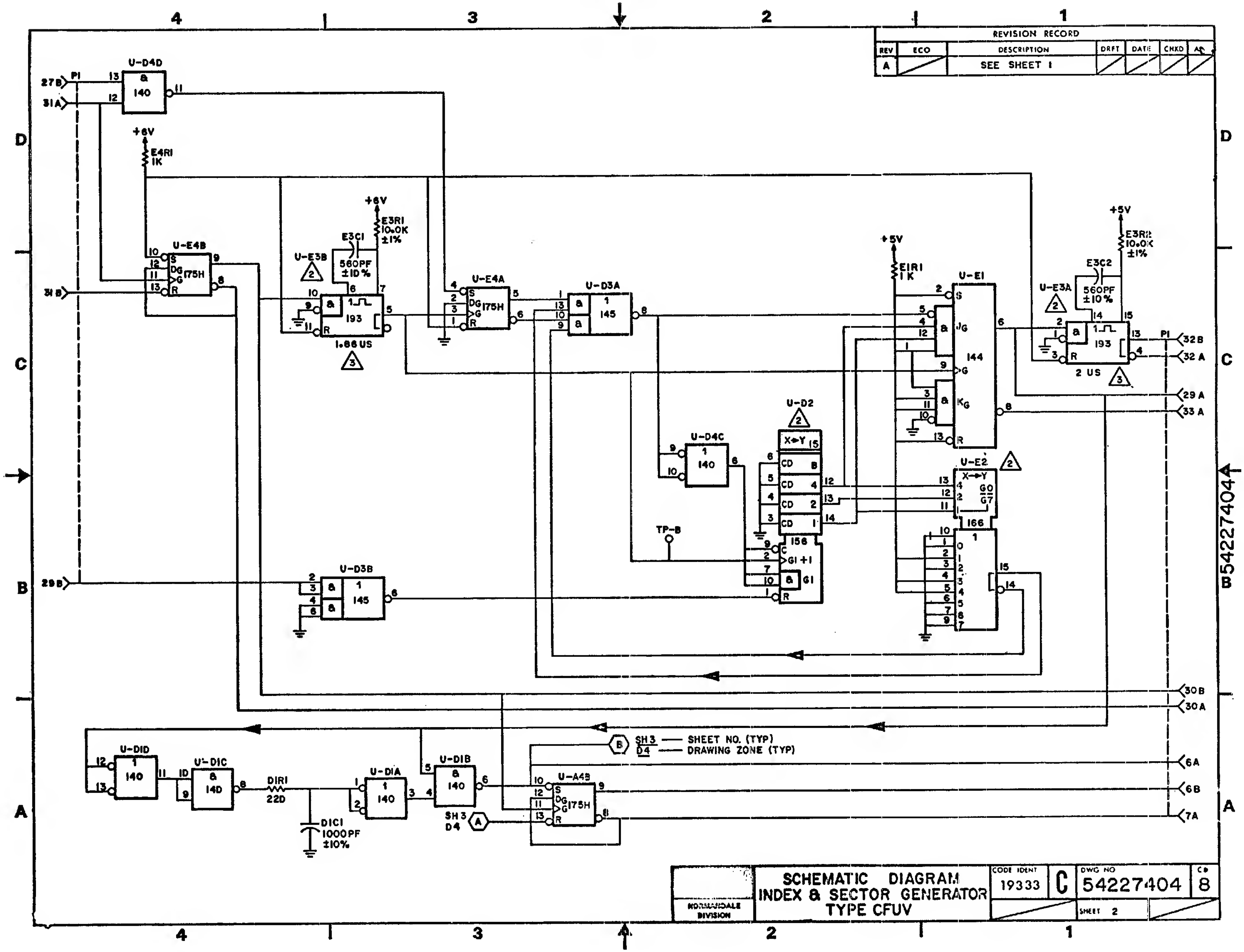
TITLE
SCHEMATIC DIAGRAM INDEX & SECTOR GENERATOR TYPE CFUV

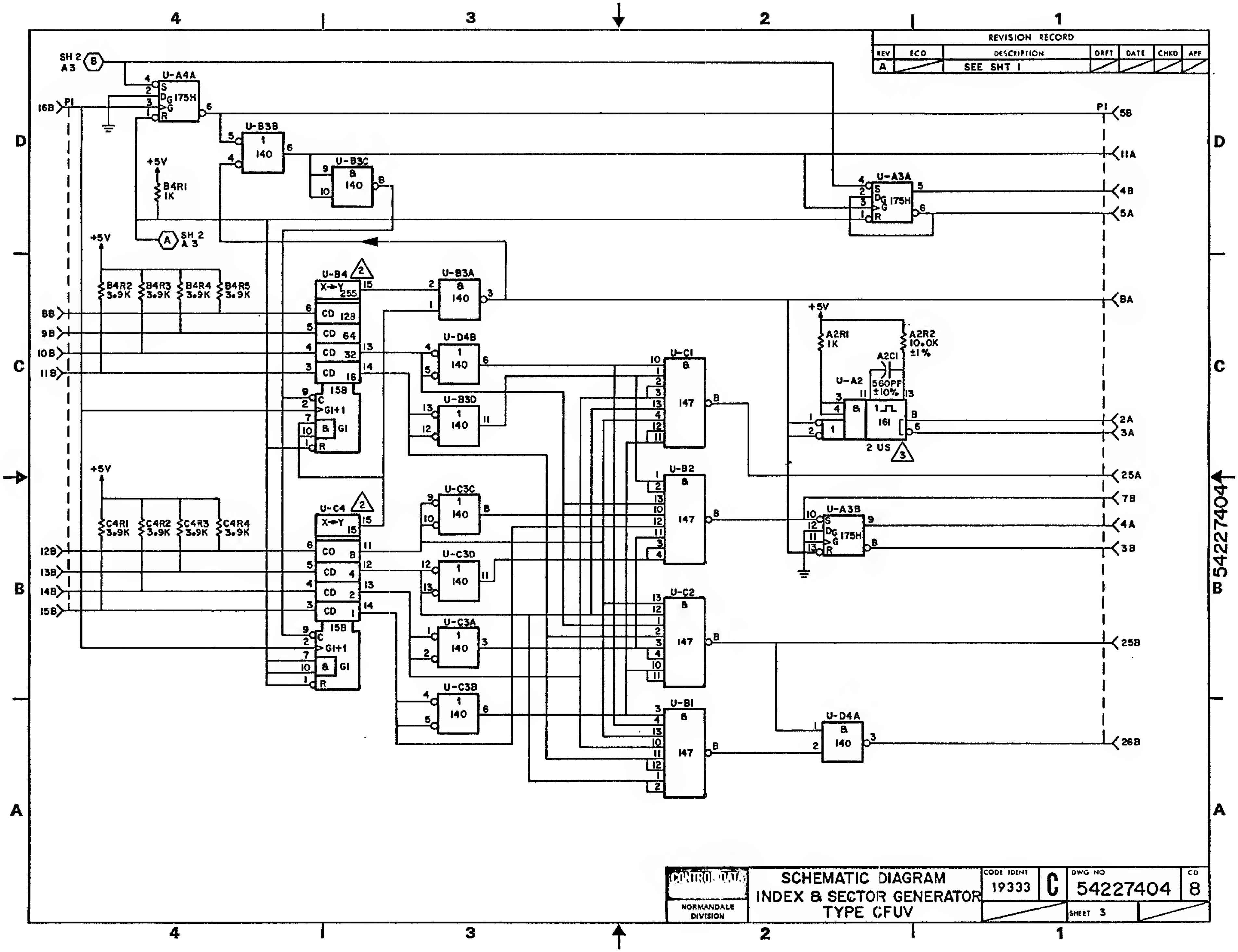
CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54227404	8

SHEET 1 OF 3

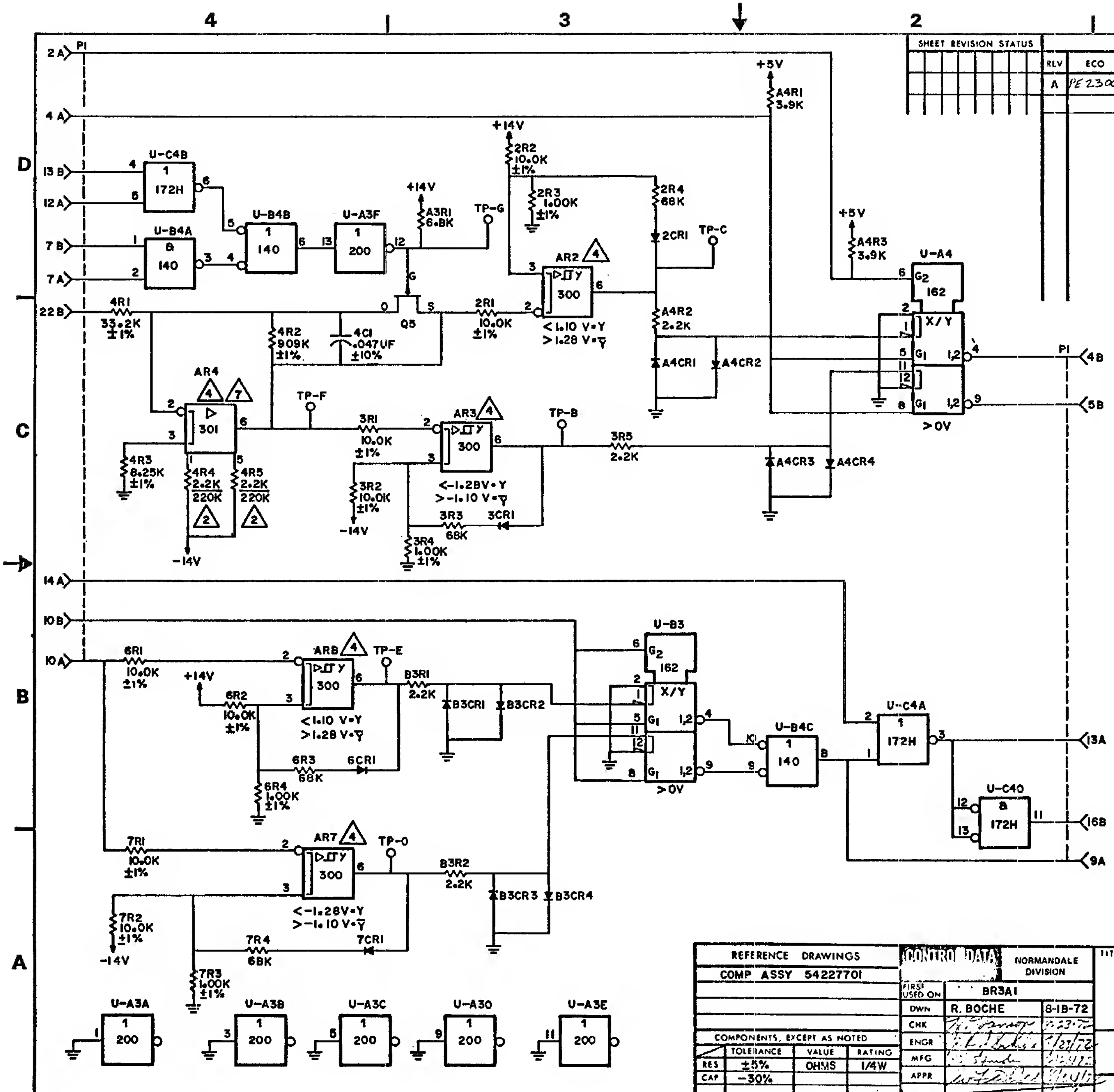
HPD

70629100 E


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1
SH 3 — SHEET NO. (TYP)
D4 — DRAWING ZONE (TYP)
SCHEMATIC DIAGRAM
INDEX & SECTOR GENERATOR
TYPE CFUV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54227404
8
SHEET 2
54227404


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHT 1
SH 2 A3
U-A4A 175H
U-B3B 140
U-B3C 140
B4R1 1K
SH 2 A 3
U-A3A 175H
U-B4
U-B3A 140
U-D4B 140
U-B3D 140
U-C1 147
U-B2 147
U-C2 147
U-B1 147
U-A2 161
A2R1 1K
A2R2 10.0K ±1%
A2C1 560PF ±10%
2 US
U-A3B 175H
U-C4
U-C3C 140
U-C3D 140
U-C3A 140
U-C3B 140
U-D4A 140
B4R2 3.9K B4R3 3.9K B4R4 3.9K B4R5 3.9K
C4R1 3.9K C4R2 3.9K C4R3 3.9K C4R4 3.9K
+5V
16B 8B 9B 10B 11B 12B 13B 14B 15B
5B 11A 4B 5A 8A 2A 3A 25A 7B 4A 3B 25B 26B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
INDEX & SECTOR GENERATOR
TYPE CFUV
CODE IDENT 19333
C
DWG NO 54227404
CD 8
SHEET 3
54227404

70629100 E



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED				

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, FET'S 50218200
   ALL DIODES, SILICON, 92115021
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. FOR VALUES OF RESISTORS 9R1, 1R1, 4R4 AND 4R5 SEE ENGINEERING TEST PROCEDURE.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. IC'S AR2, AR3, AR4, AR6, AND AR7 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14 V
5. DIODE, GERMANIUM, 11801200.
6. DELAY TIME FOR REFERENCE ONLY.
7. ONLY ONE TRIM RESISTOR, 4R4 OR 4R5 TO BE USED WITH OPERATIONAL AMP. AR4 PER ENGINEERING PROCEDURE.

54227801

REFERENCE DRAWINGS	
COMP ASSY 54227701	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

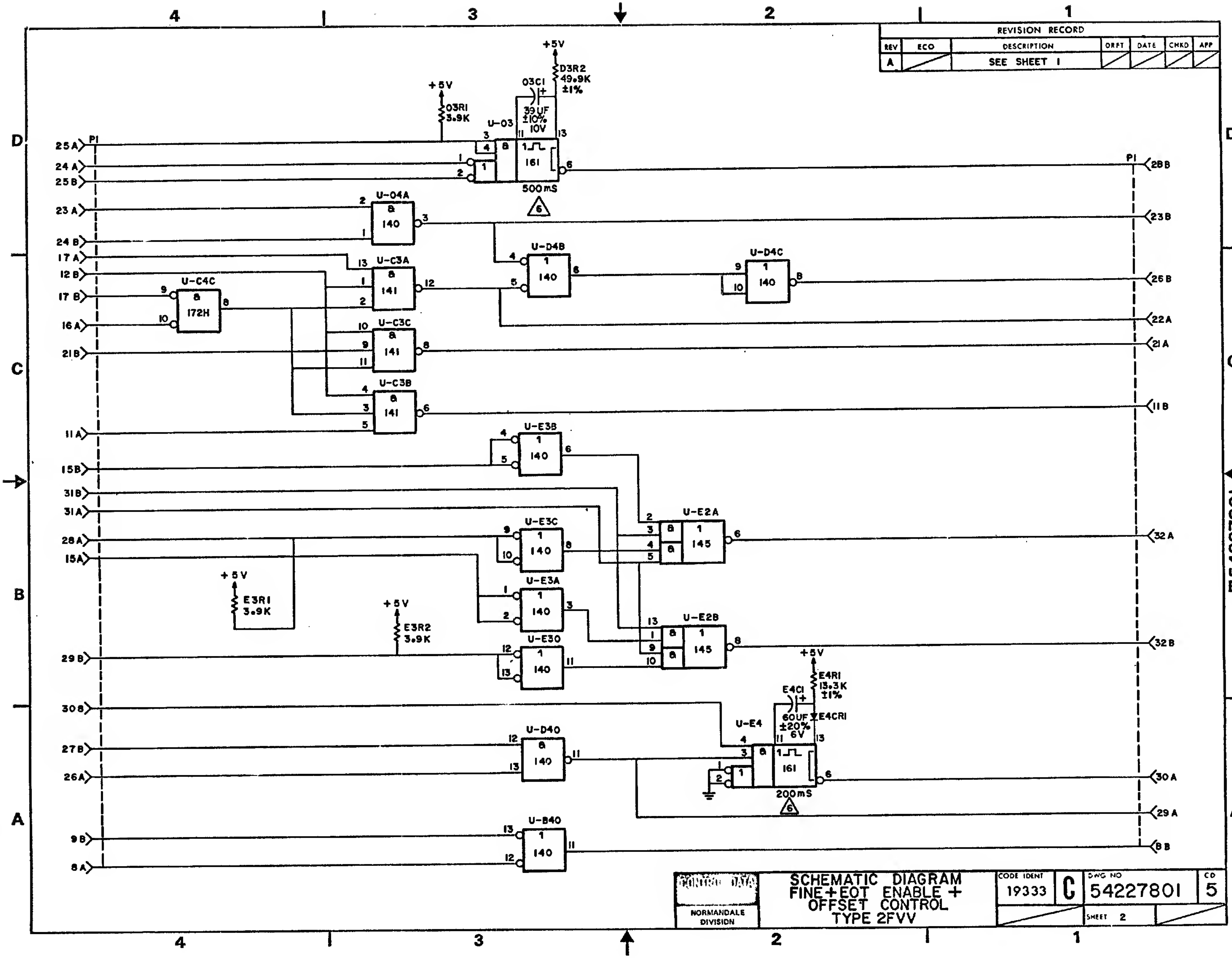
FIRST USED ON	BR3A1	
DWN	R. BOCHE	8-18-72
CHK		
ENGR		
MFG		
APPR		

SCHEMATIC DIAGRAM
FINE + EOT ENABLE + OFFSET CONTROL
TYPE 2FVV

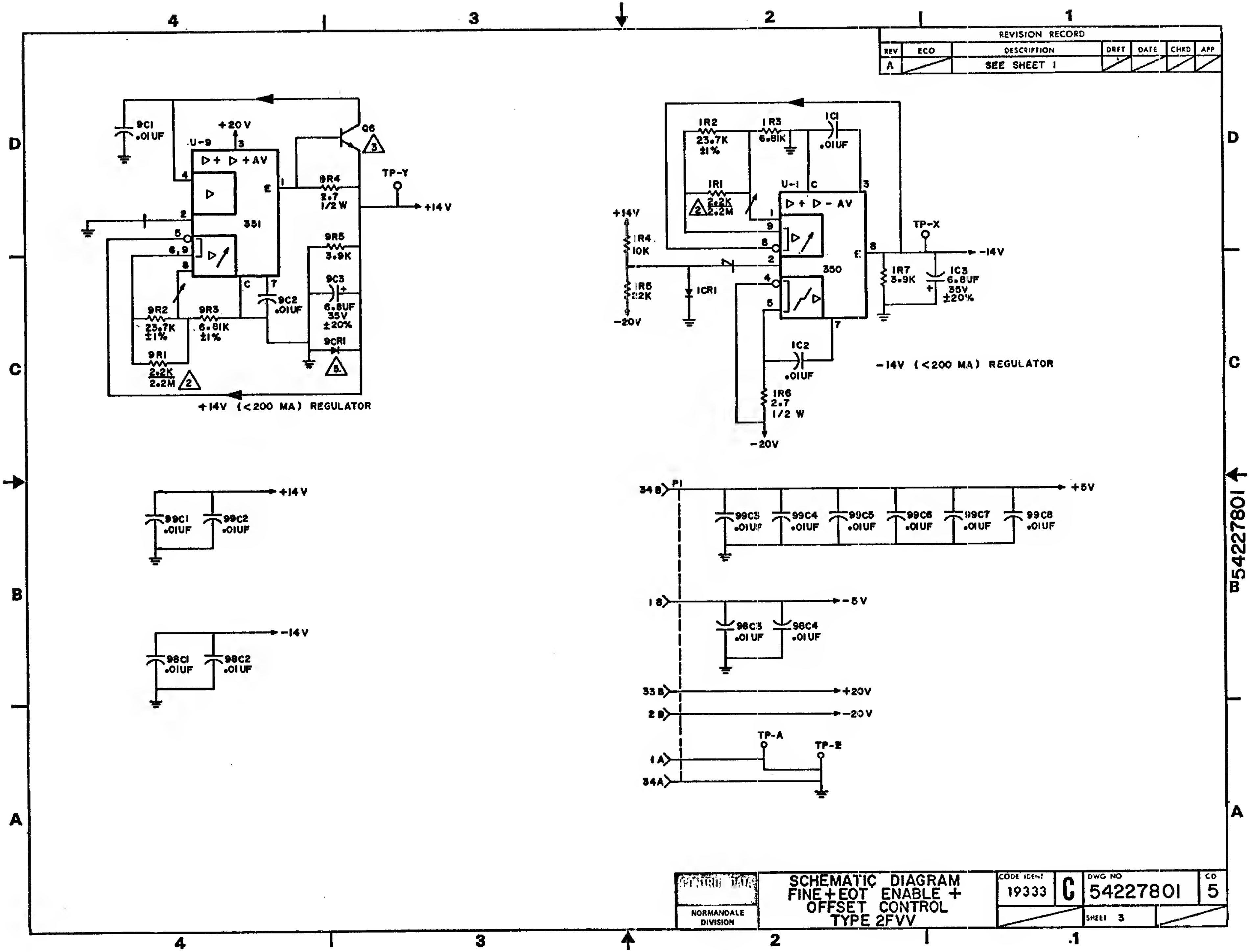
CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54227801	5

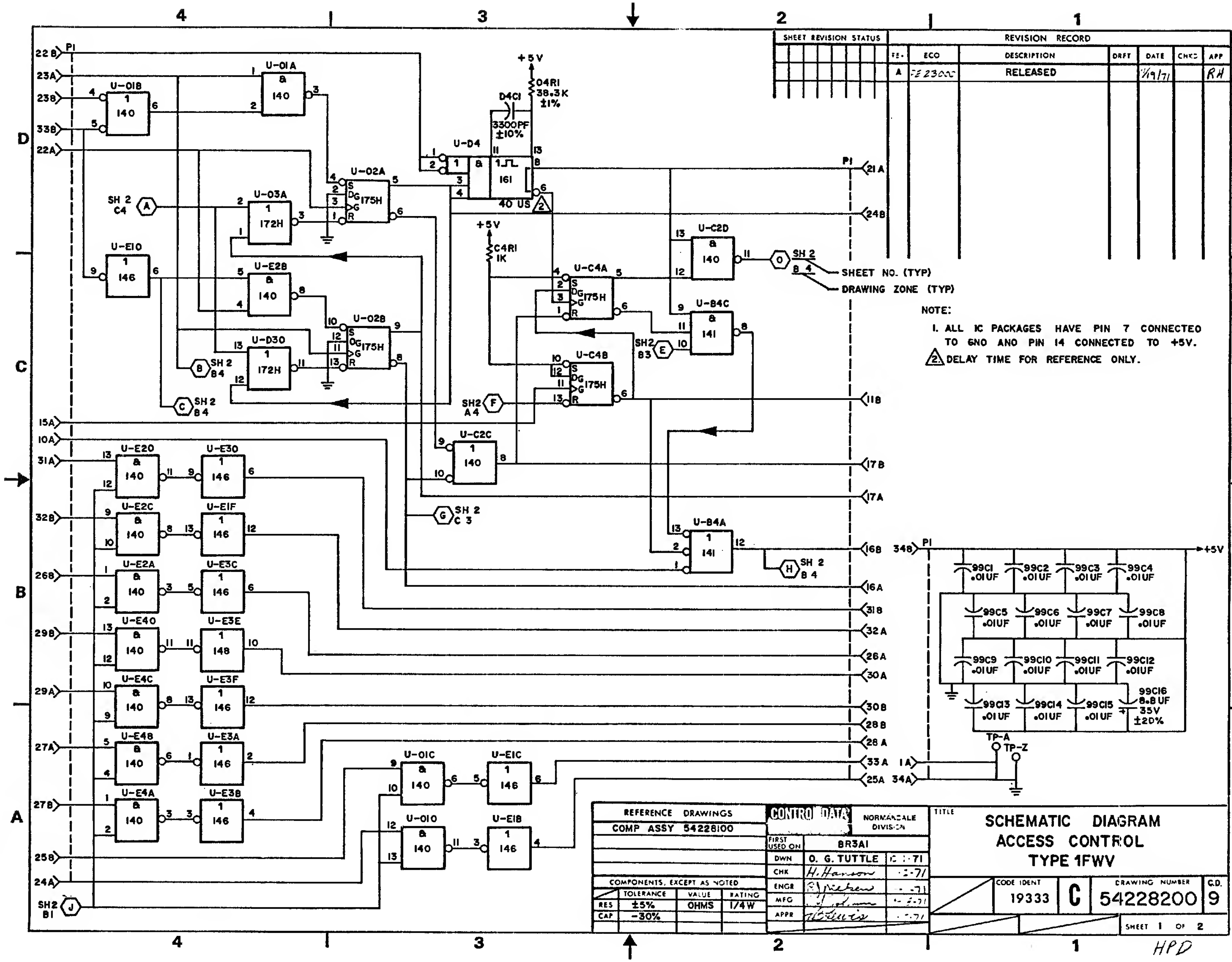
SHEET 1 OF 3

HPD



REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
P1
25A
24A
25B
23A
24B
17A
12B
17B
16A
21B
11A
15B
31B
31A
28A
15A
29B
30B
27B
26A
9B
8A
+5V
03R1 3.9K
D3R2 49.9K ±1%
03C1
39UF ±10% 10V
U-03
161
500mS
U-04A
140
U-D4B
140
U-D4C
140
U-C3A
141
U-C4C
172H
U-C3C
141
U-C3B
141
U-E3B
140
U-E2A
145
U-E3C
140
E3R1 3.9K
E3R2 3.9K
U-E3A
140
U-E2B
145
U-E30
140
E4R1 13.3K ±1%
E4C1
60UF ±20% 6V
E4CR1
U-E4
161
200mS
U-D40
140
U-B40
140
28B
23B
26B
22A
21A
11B
32A
32B
30A
29A
8B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FINE + EOT ENABLE +
OFFSET CONTROL
TYPE 2FVV
CODE IDENT 19333
C
DWG NO 54227801
CD 5
SHEET 2
54227801


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1
+14V (<200 MA) REGULATOR
-14V (<200 MA) REGULATOR
U-9
U-1
351
350
Q6
TP-Y
TP-X
TP-A
TP-Z
P1
+14V
-14V
+5V
-5V
+20V
-20V
9C1 .01UF
9R4 2.7 1/2 W
9R5 3.9K
9C3 6.8UF 35V ±20%
9C2 .01UF
9R2 23.7K ±1%
9R3 6.81K ±1%
9R1 2.2K 2.2M
9CR1
1R2 23.7K ±1%
1R3 6.81K
1C1 .01UF
1R1 2.2K 2.2M
1R4 10K
1R5 2.2K
1CR1
1R7 3.9K
1C3 6.8UF 35V ±20%
1C2 .01UF
1R6 2.7 1/2 W
99C1 .01UF
99C2 .01UF
98C1 .01UF
98C2 .01UF
99C3 .01UF
99C4 .01UF
99C5 .01UF
99C6 .01UF
99C7 .01UF
99C8 .01UF
98C3 .01 UF
98C4 .01 UF
34 B
1 B
33 B
2 B
1 A
34 A
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FINE + EOT ENABLE +
OFFSET CONTROL
TYPE 2FVV
CODE IDENT 19333
C
DWG NO 54227801
CD 5
SHEET 3
54227801



SHEET REVISION STATUS	REVISION RECORD					
RE-	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	FE 23000	RELEASED		1/19/71		RH

NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS	
COMP ASSY 54228100	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR3A1
DWN	O. G. TUTTLE
CHK	H. Hanson
ENGR	
MFG	
APPR	

TITLE

SCHEMATIC DIAGRAM ACCESS CONTROL TYPE 1FWV

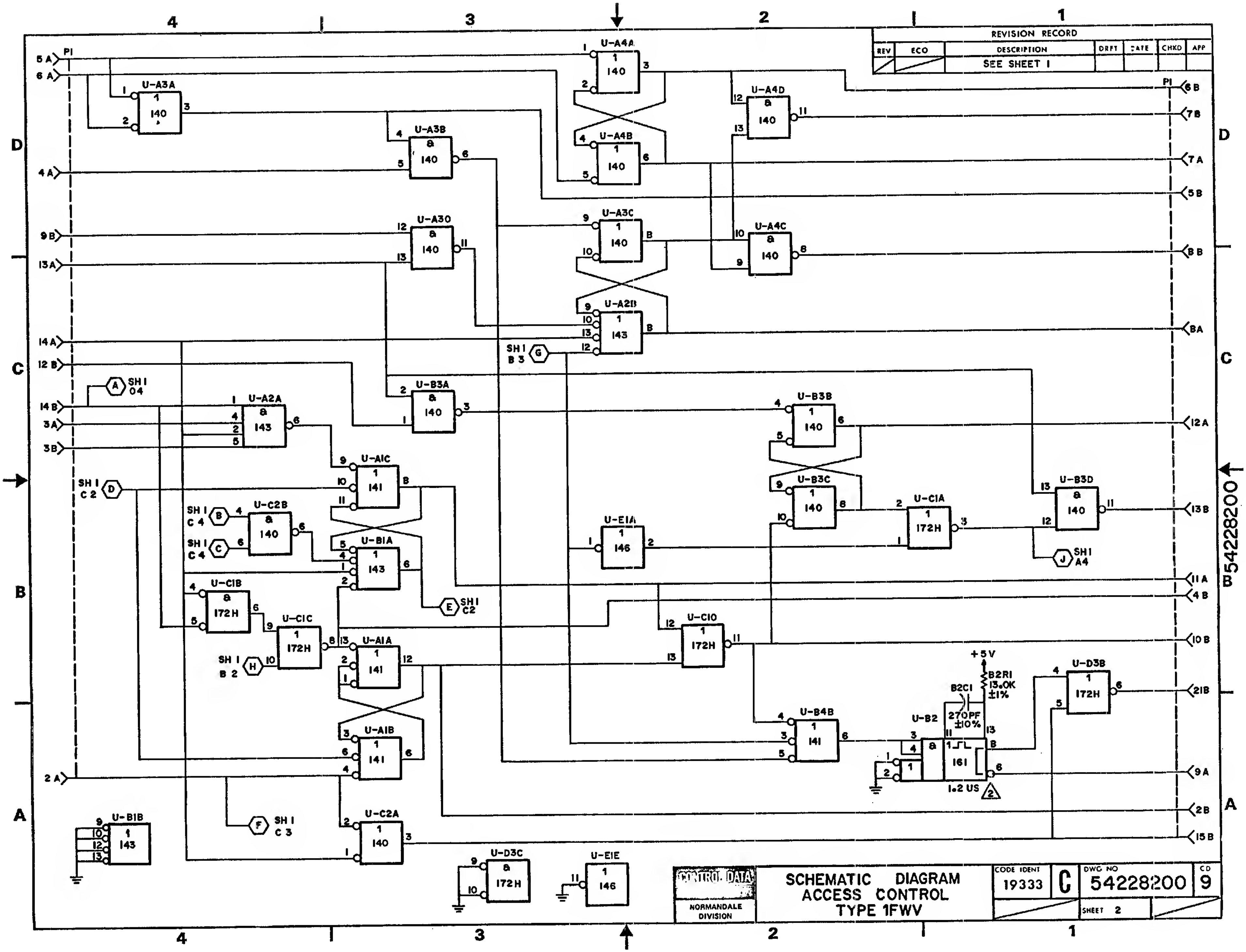
CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54228200	9

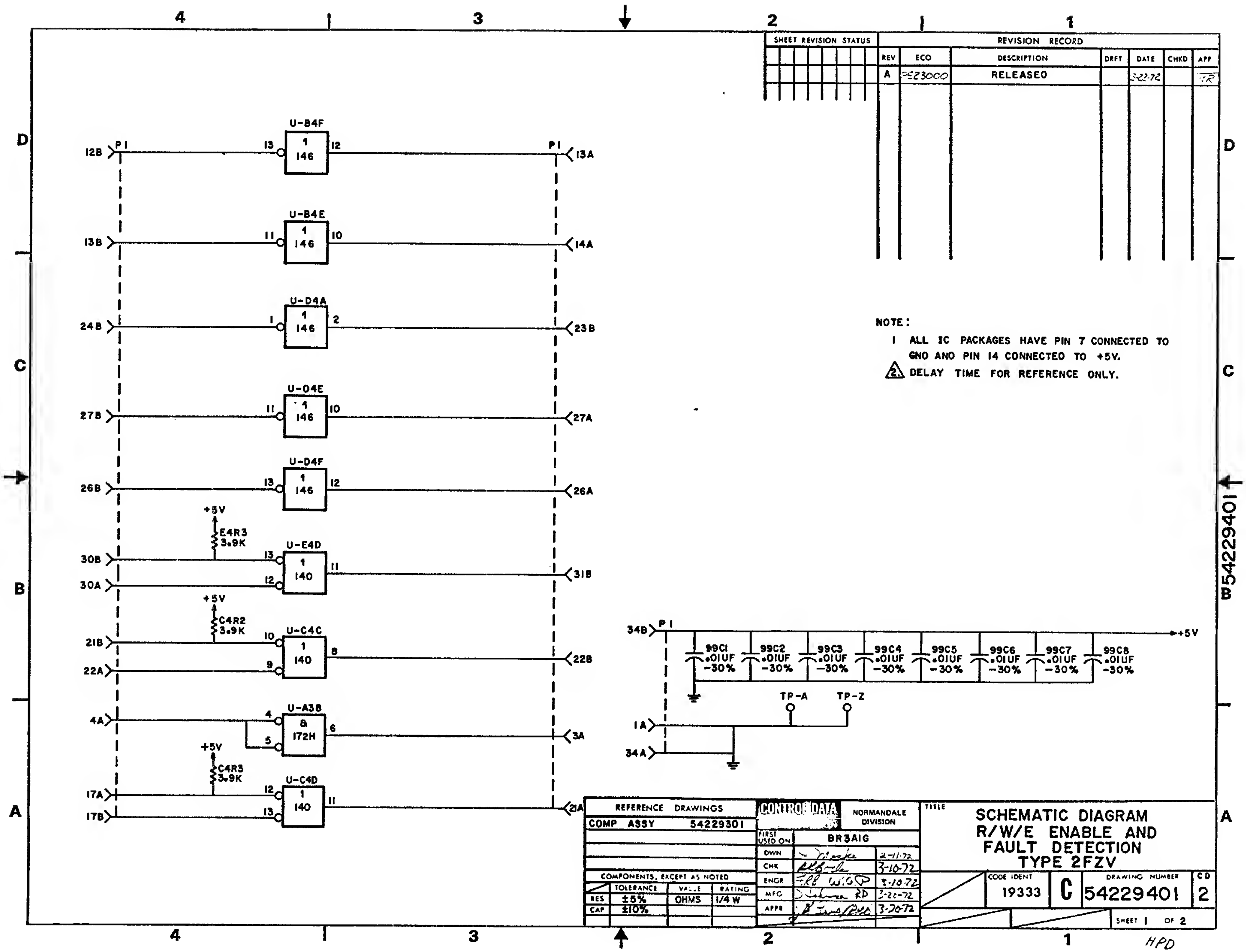
SHEET 1 OF 2

HPD

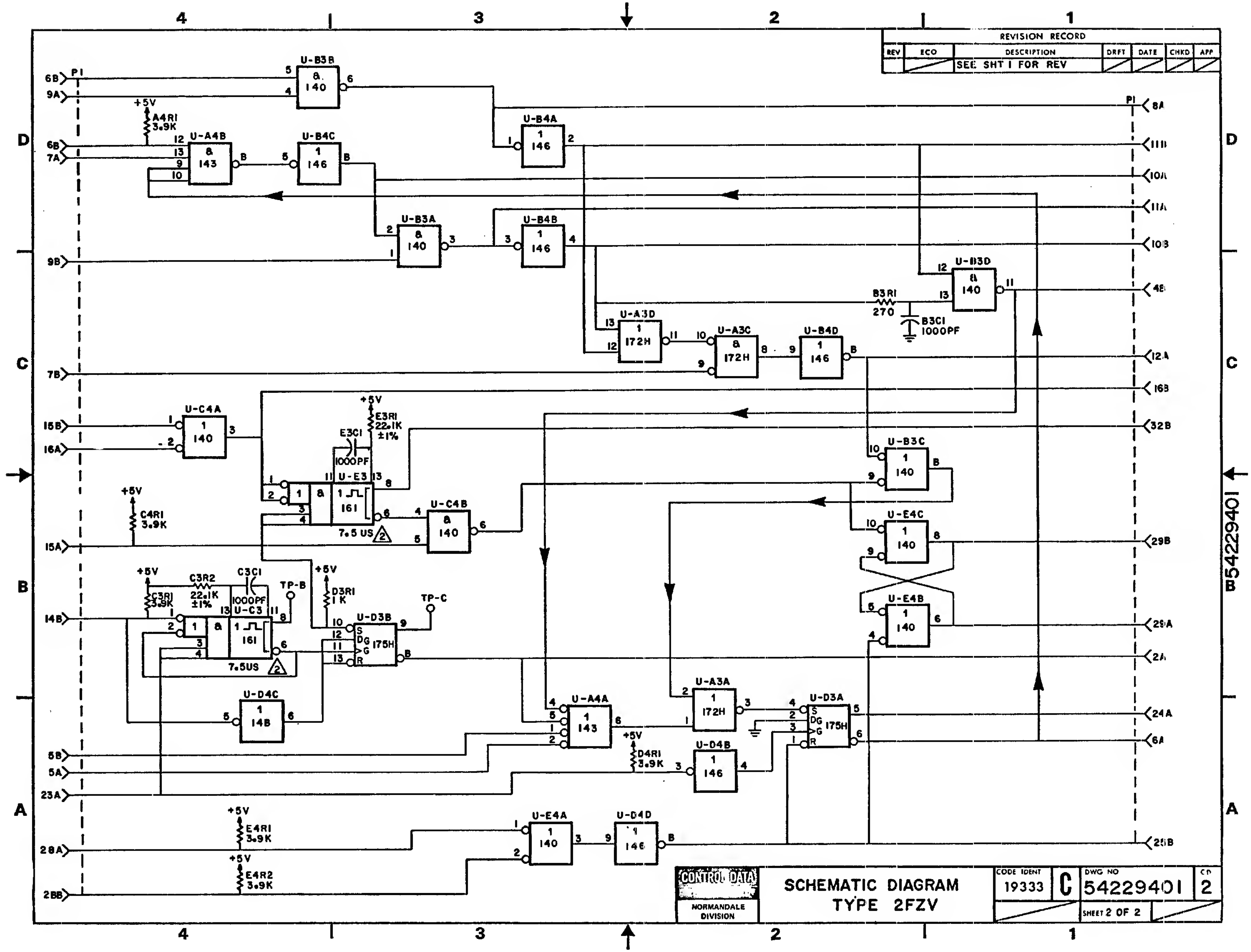
54228200

70629100 E

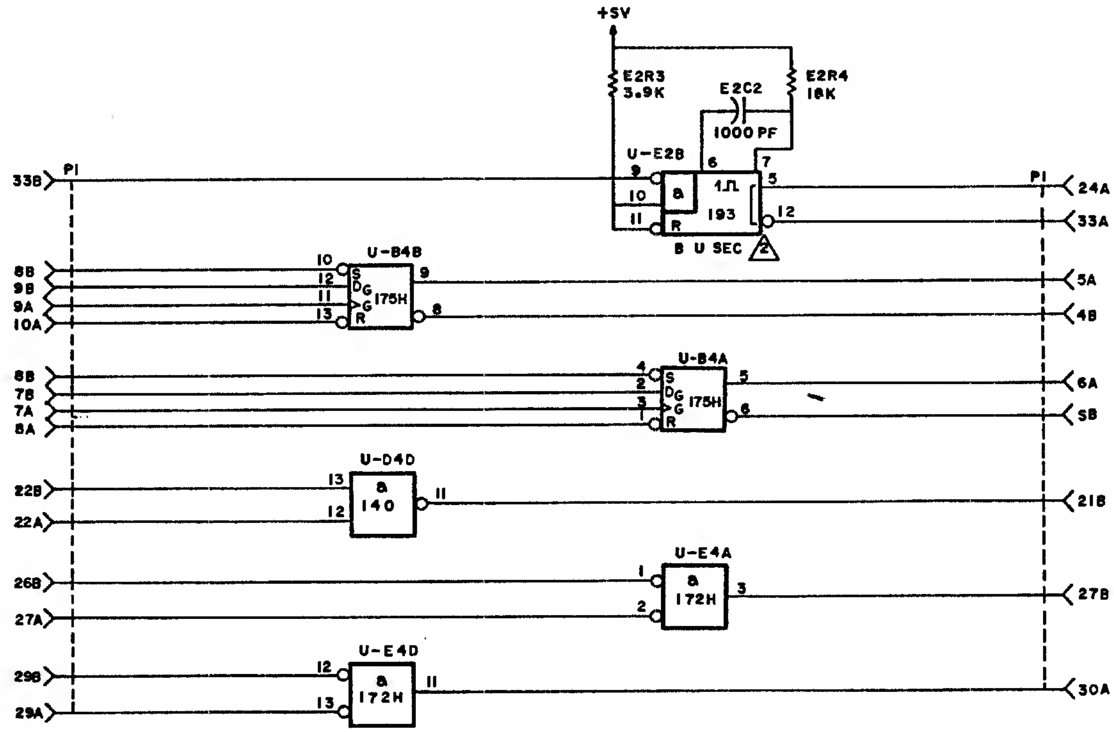

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SEE SHEET 1
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
ACCESS CONTROL
TYPE 1FWV
CODE IDENT 19333
C
DWG NO 54228200
CD 9
SHEET 2
54228200


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23000 | RELEASED | | 3-22-72 | | TR
NOTE:
1 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2 DELAY TIME FOR REFERENCE ONLY.
U-B4F 1 146
U-B4E 1 146
U-D4A 1 146
U-D4E 1 146
U-D4F 1 146
U-E4D 1 140
U-C4C 1 140
U-A3B & 172H
U-C4D 1 140
E4R3 3.9K
C4R2 3.9K
C4R3 3.9K
+5V
P1
12B 13A 13B 14A 24B 23B 27B 27A 26B 26A 30B 30A 31B 21B 22A 22B 4A 3A 17A 17B 21A
34B 1A 34A
99C1 .01UF -30%
99C2 .01UF -30%
99C3 .01UF -30%
99C4 .01UF -30%
99C5 .01UF -30%
99C6 .01UF -30%
99C7 .01UF -30%
99C8 .01UF -30%
TP-A TP-Z
REFERENCE DRAWINGS
COMP ASSY 54229301
COMPONENTS, EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHMS 1/4 W
CAP ±10%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3A1G
DWN 2-11-72
CHK 3-10-72
ENGR 3-10-72
MFG 3-20-72
APPR 3-20-72
TITLE
SCHEMATIC DIAGRAM
R/W/E ENABLE AND
FAULT DETECTION
TYPE 2FZV
CODE IDENT 19333
C
DRAWING NUMBER 54229401
CD 2
SHEET 1 OF 2
54229401
HPD

70629100 E


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SEE SHT I FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2FZV
CODE IDENT 19333
C
DWG NO 54229401
2
SHEET 2 OF 2
54229401

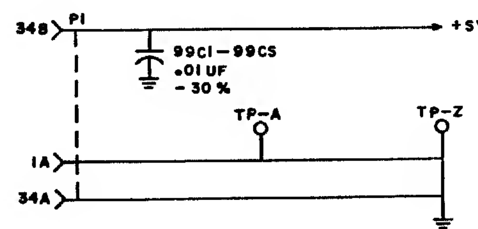
SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23…	RELEASED			2-20-73	



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S MUST HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.



54233400

REFERENCE DRAWINGS		
COMP ASSY 54233300		
COMPONENTS, EXCEPT AS NOTED		
TOLERANCE	VALUE	RATING
RES ± 5%	OHMS	1/4 W
CAP ± 10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	R. RICHTER	1-18-73
CHK	H. Hanson	1-31-73
ENGR	H. Brush	1-31-73
MFG	[illegible]	2-5-73
APPR	[illegible]	2-2-73

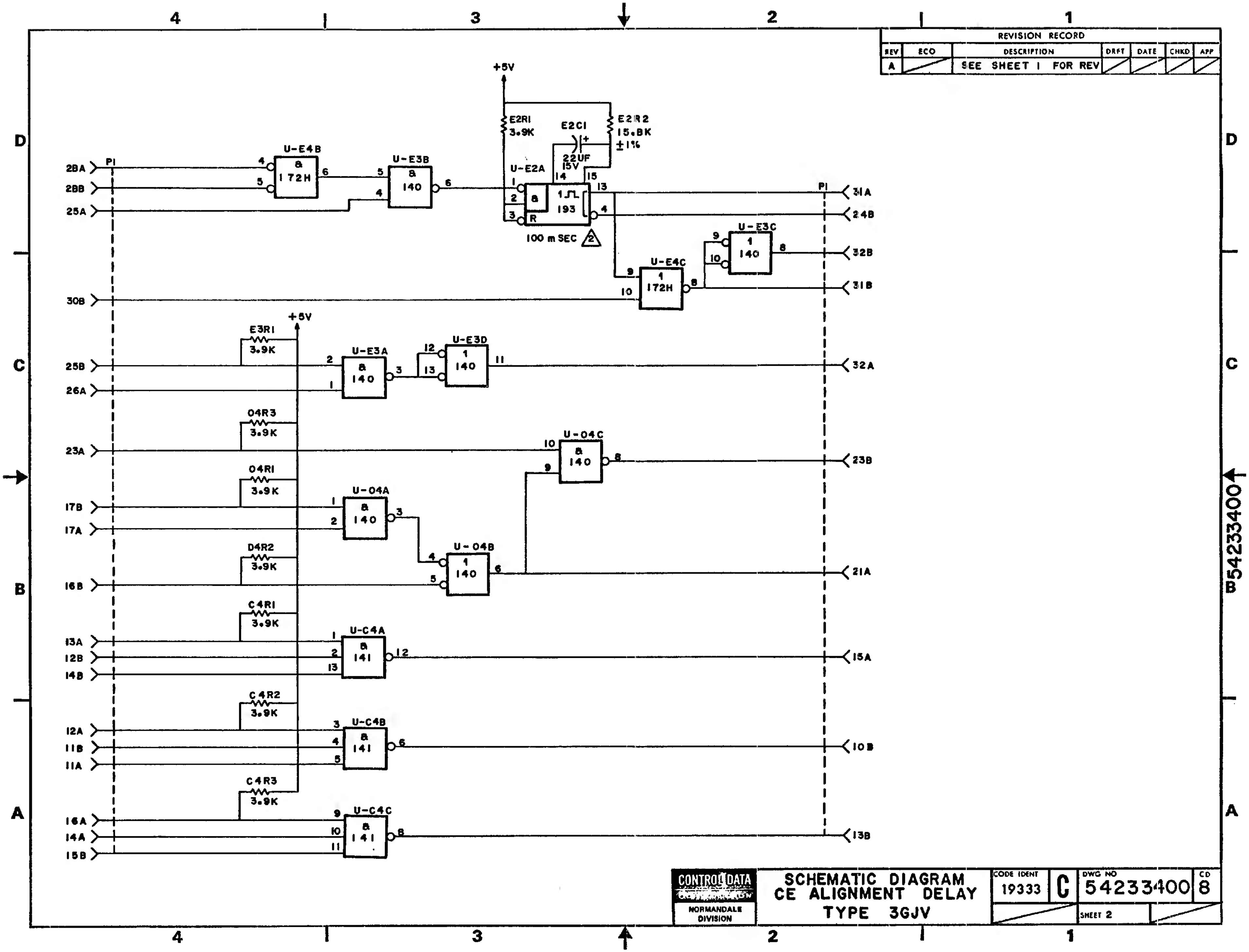
TITLE

SCHEMATIC DIAGRAM CE ALIGNMENT DELAY TYPE 3GJV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54233400	8

SHEET 1 OF 2

—HPD—



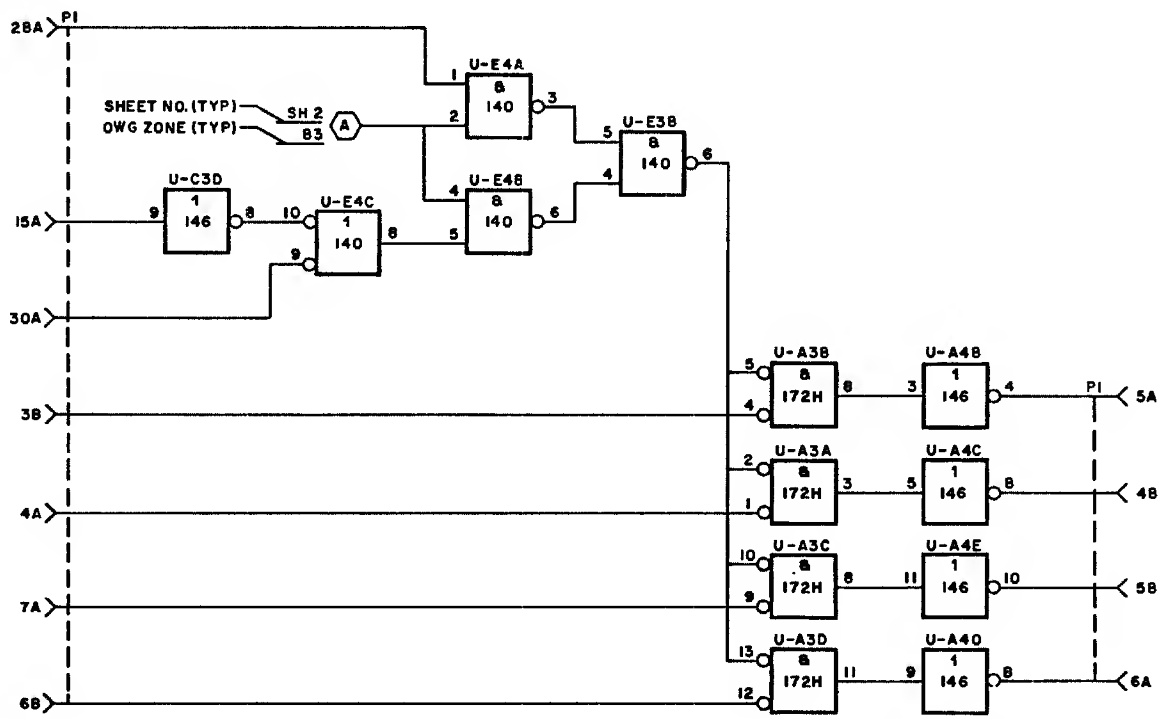
SCHEMATIC DIAGRAM
CE ALIGNMENT DELAY
TYPE 3GJV

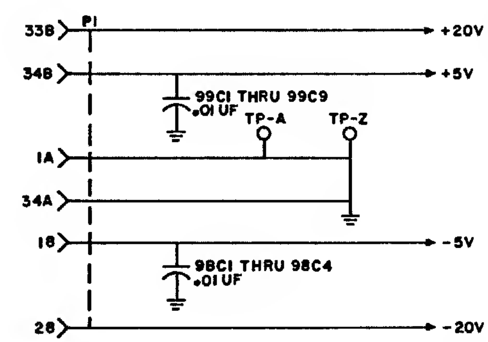
CODE IDENT		DWG NO	CD
19333	C	54233400	8
		SHEET 2	

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED				
	B	PE30914	CONNECTOR PIN CHANGED FROM 6B TO 8A.	RKR	1-16	RRB	II
	C	PE34116	CHANGED INDUCTOR VALUE TO 47 mH	R.K.	1-19-73	RRB	[illegible]

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL 14 PIN I-C'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V. ALL 16 PIN I-C'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V. ALL TRANSISTORS, SNPN, PLANAR, 24562100. ALL DIODES, SILICON, 24553500.
2. TRANSISTOR, SNPN, 2N3642, 50210510.
3. TRANSISTOR, SPNP, 2N3645, 50211210.
4. DIODE, SILICON, 92115023.
5. DIODE, SILICON, 92115021.
6. I-C A2, B2, C2, D2, AND E2 HAVE PIN 13 CONNECTED TO -5V.
7. I-C U-E1 HAS PIN 4 CONNECTED TO -5V AND PINS 9 AND 13 CONNECTED TO +5V.
8. DIODE, GERMANIUM, 11801200.





REFERENCE DRAWINGS	
COMP ASS'Y 54233700	
COMPONENTS, EXCEPT AS NOTED	

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	S. ZAK	10-2-72
CHK	[illegible]	10-10-72
ENGR	[illegible]	10-10-72
MFG	[illegible]	10-12-72
APPR	[illegible]	[illegible]

TITLE

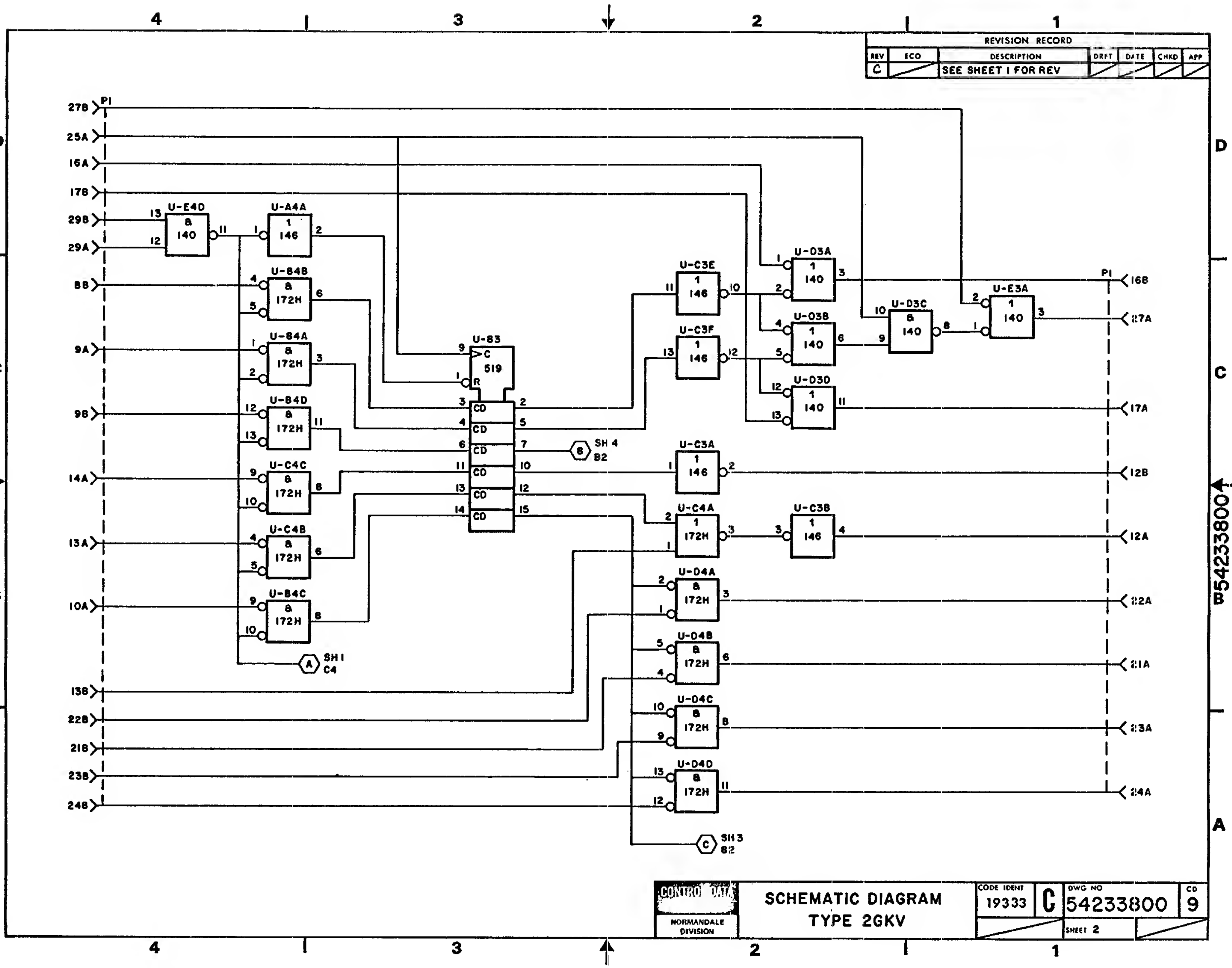
SCHEMATIC DIAGRAM STATIC DIAGNOSTIC TYPE 2GKV

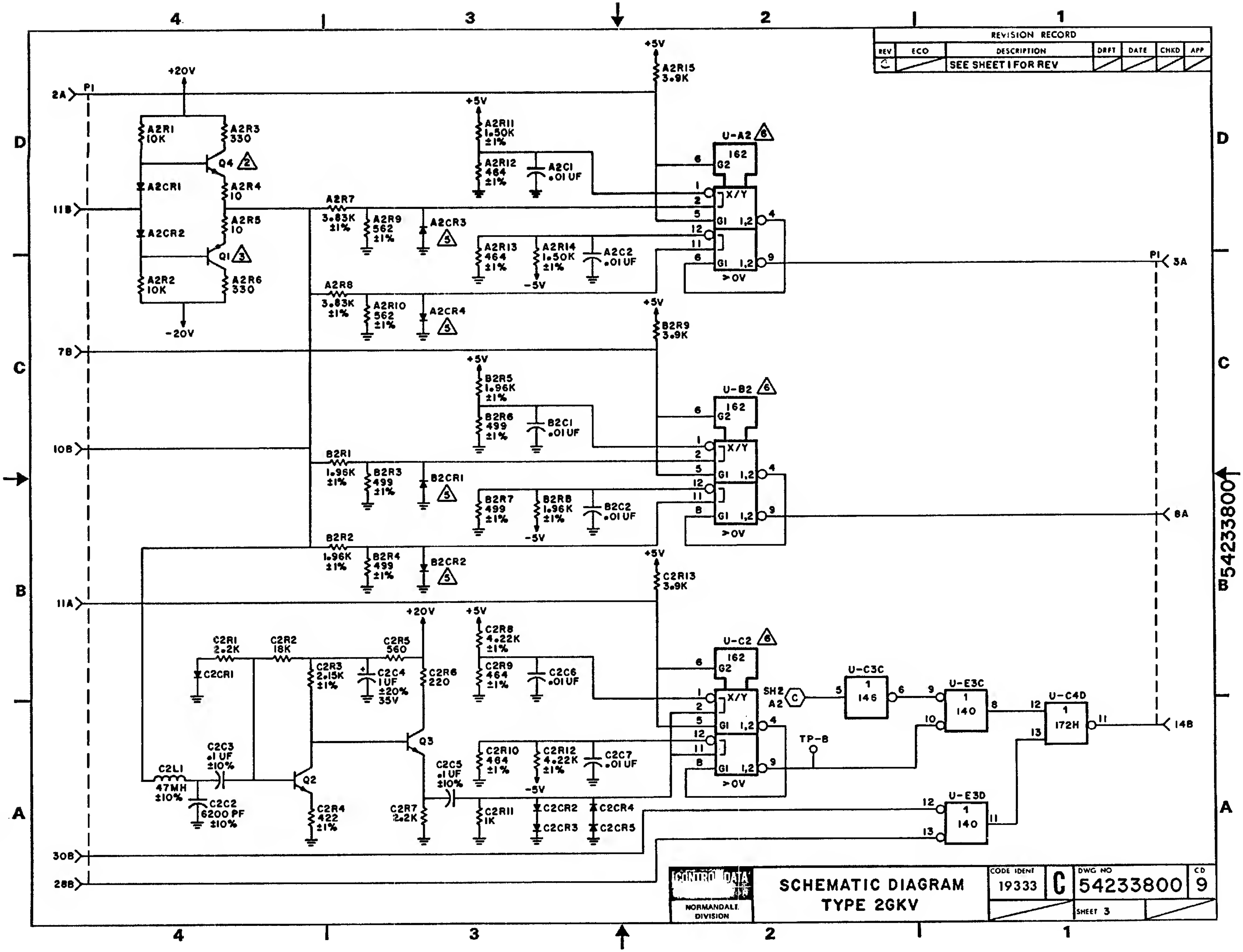
CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54233800	9

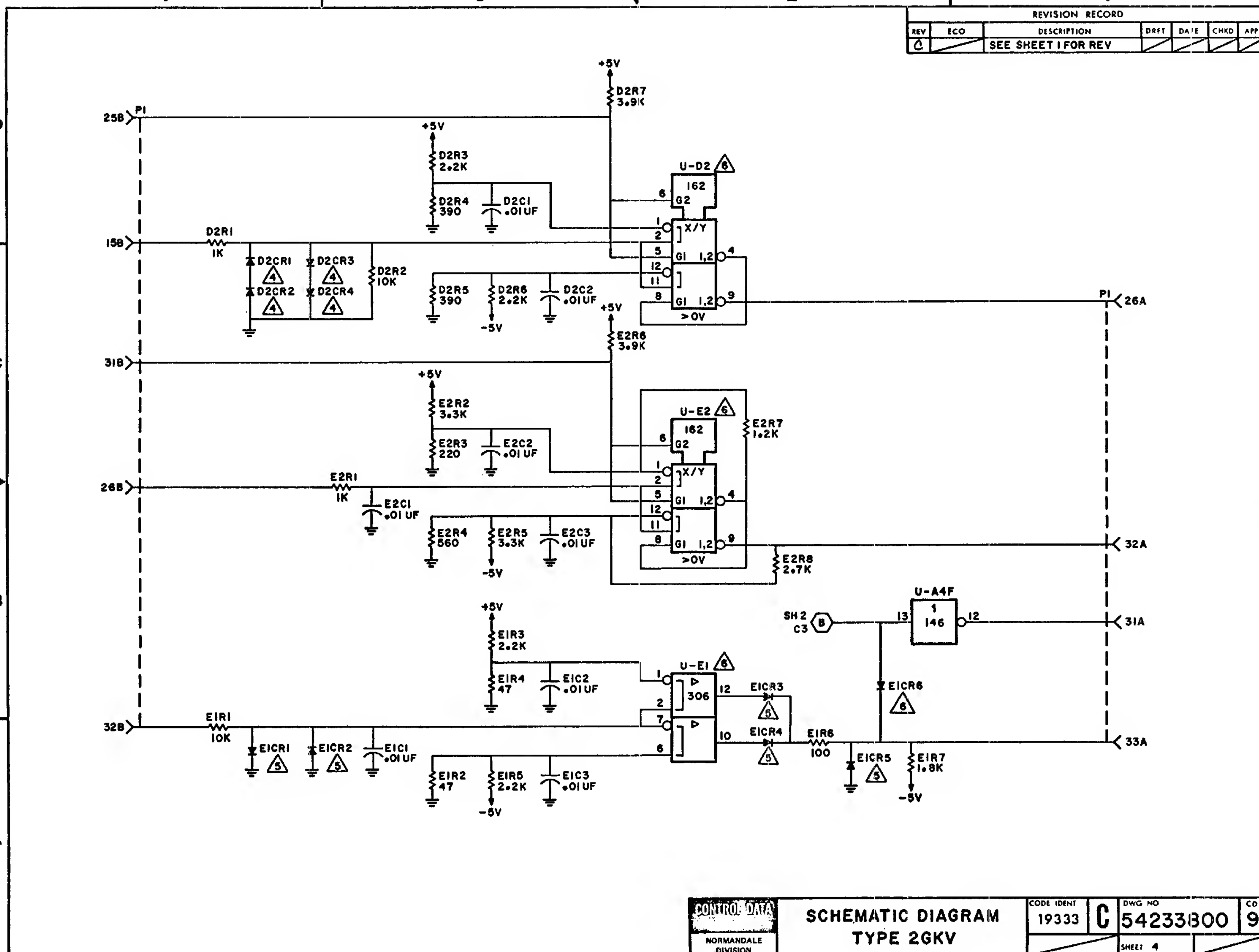
SHEET 1 OF 4

HPD

54233800


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
C SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2GKV
CODE IDENT 19333
C
DWG NO 54233800
CD 9
SHEET 2
54233800


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
C SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2GKV
CODE IDENT 19333
C
DWG NO 54233800
CD 9
SHEET 3
54233800



CONTROL DATA
NORMANDALE DIVISION

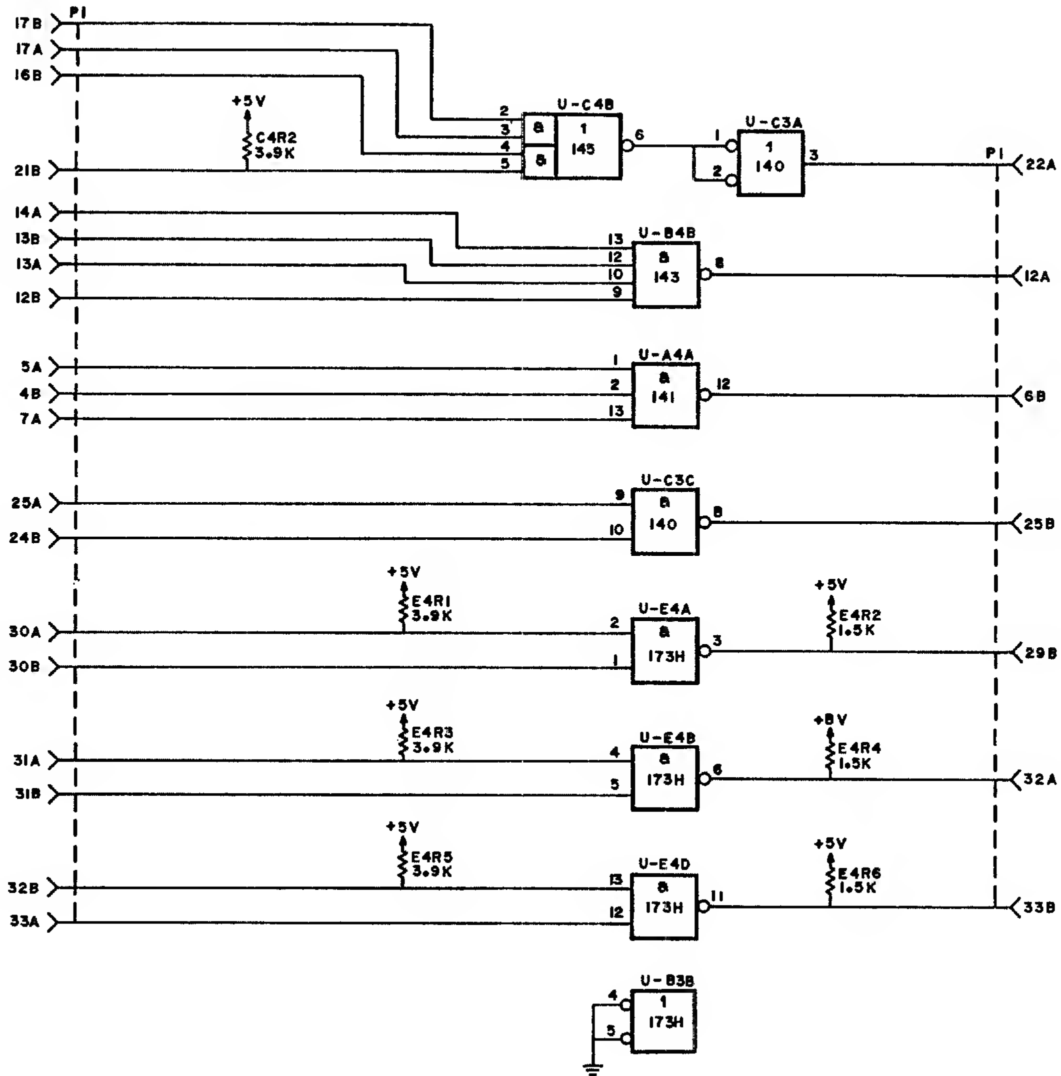
SCHEMATIC DIAGRAM
TYPE 2GKV

CODE IDENT 19333 C DWG NO 54233800 CD 9
SHEET 4

SHEET REVISION STATUS								

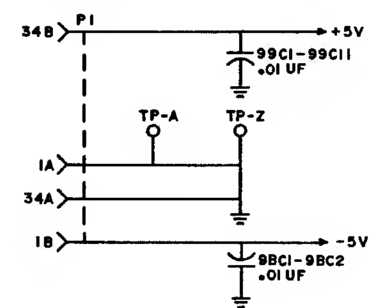
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE2[illegible]	RELEASED				
B	PE30970	CHANGE GND TO -5V	RB	12-8-72	[illegible]	III



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310.
   ALL DIODES, SILICON, 92115021.
2. TRANSISTOR, SPNP, 2N4916, 50211610.
3. TRANSISTOR, SNPN, 2N3568, 50210810.
4. DIODE, ZENER, 50240108.
5. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
6. VALUE OF D4R1 TO BE SELECTED IN PRODUCTION TO GIVE A PULSE OF 55 US ±7 US AT TEST POINT G.
7. VALUE OF 2R1 TO BE SELECTED IN PRODUCTION TO DETECT A SPEED OF 3000 R.P.M. ±300 R.P.M.
8. DELAY TIME FOR REFERENCE ONLY
9. AR10 HAS PIN 7 CONNECTED TO +5V AND PIN 4 CONNECTED TO -5V.



REFERENCE DRAWINGS	
COMP ASSY	54234100

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	K STREETER	3-2-72
CHK	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
MFG	[illegible]	3-7-72
APPR	[illegible]	[illegible]

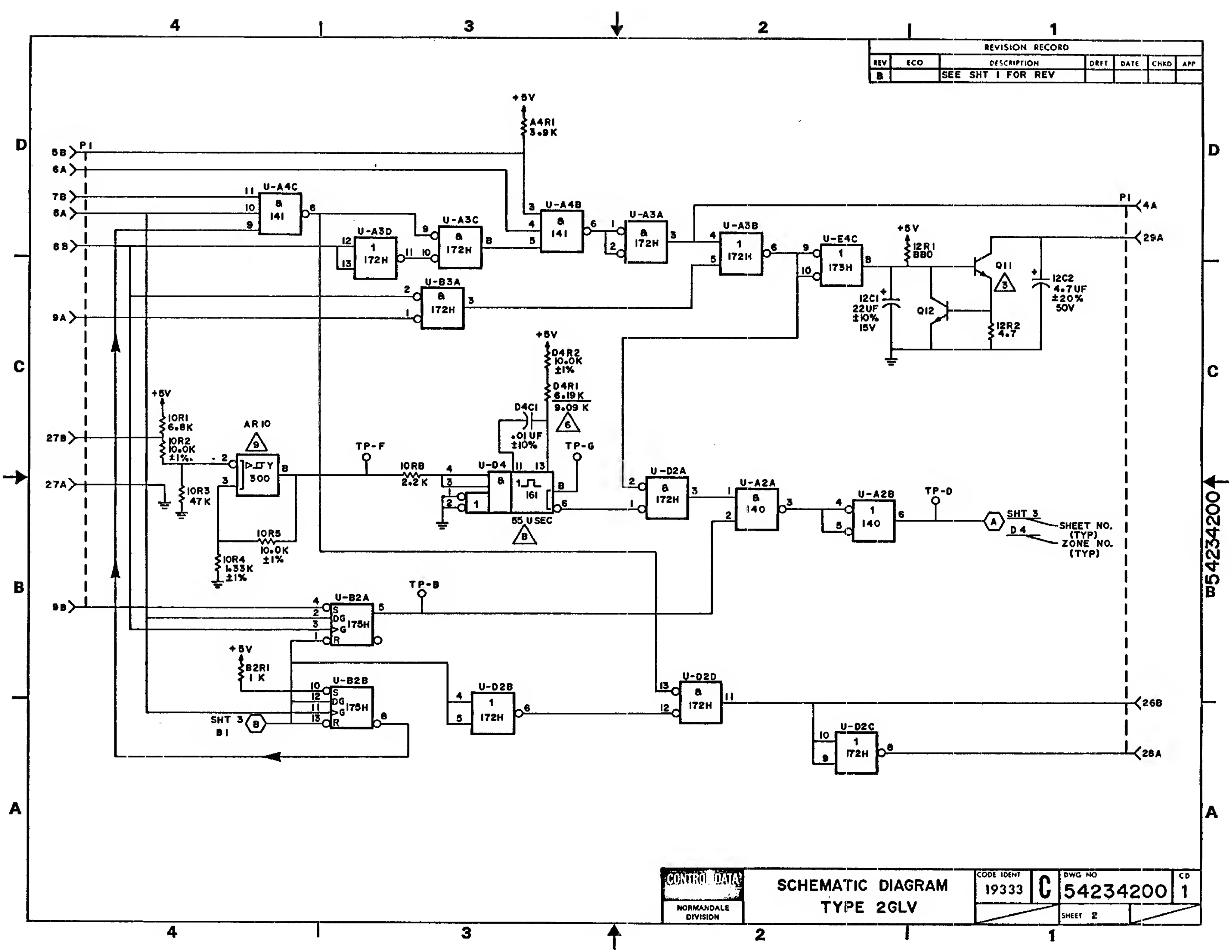
TITLE: SCHEMATIC DIAGRAM MOTOR CONTROL & SPEED DETECTOR TYPE 2GLV

CODE IDENT	SIZE	DRAWING NUMBER	CO
19333	C	54234200	1

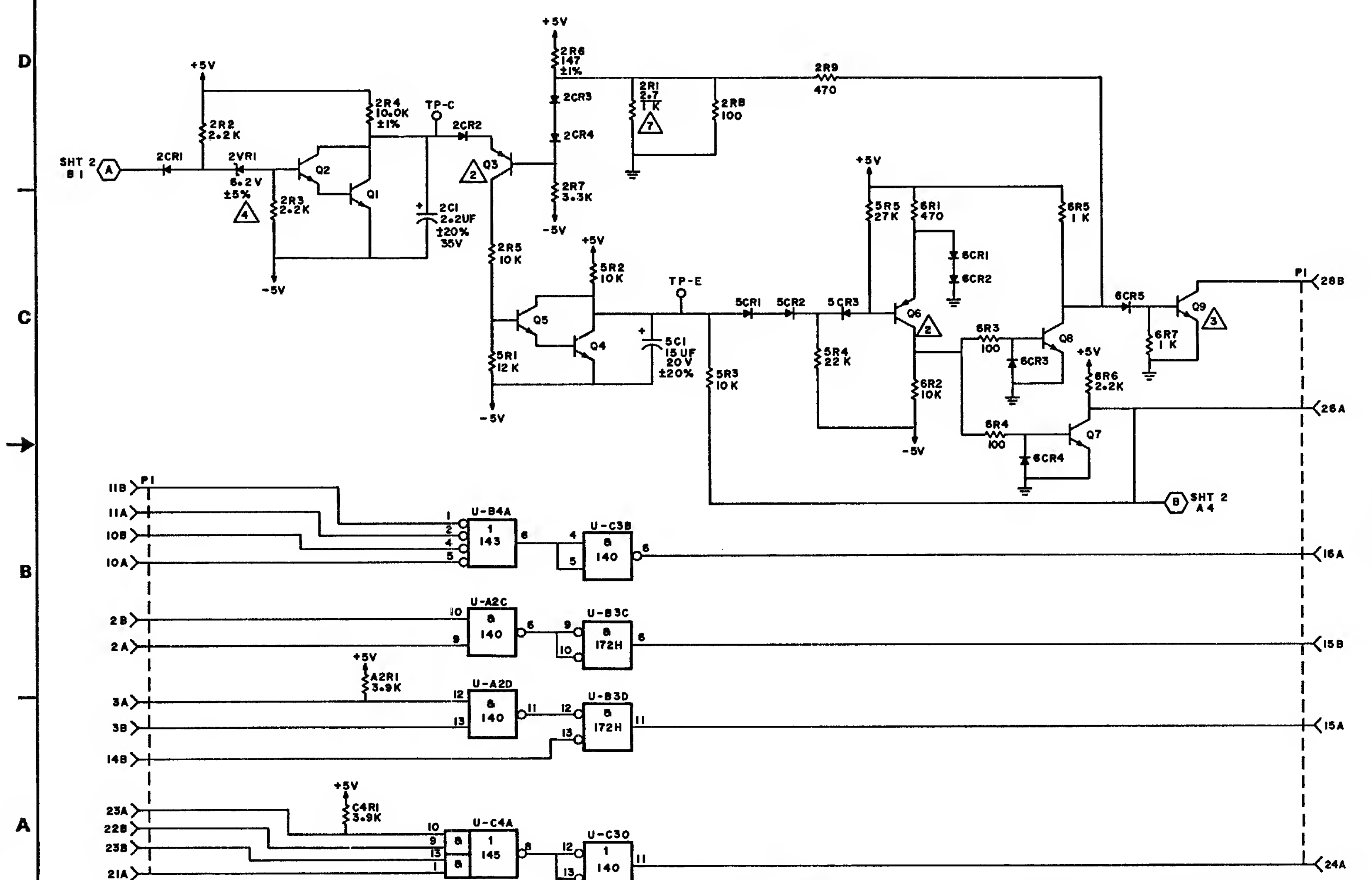
SHEET 1 OF 3

HPD

54234200


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
B | | SEE SHT 1 FOR REV
P1
5B
6A
7B
8A
8B
9A
27B
27A
9B
4A
29A
26B
28A
U-A4C 8 141
U-A3D 1 172H
U-A3C 8 172H
U-B3A 8 172H
U-A4B 8 141
U-A3A 8 172H
U-A3B 1 172H
U-E4C 1 173H
+5V
A4R1 3.9K
12R1 880
Q11
Q12
12C1 22UF ±10% 15V
12R2 4.7
12C2 4.7UF ±20% 50V
10R1 6.8K
10R2 10.0K ±1%
10R3 47K
AR10
300
TP-F
10R8 2.2K
U-D4 8
161
D4C1 .01UF ±10%
D4R2 10.0K ±1%
D4R1 6.19K 9.09K
TP-G
55 USEC
10R5 10.0K ±1%
10R4 1.33K ±1%
U-D2A 8 172H
U-A2A 8 140
U-A2B 1 140
TP-D
SHT 3
D4
SHEET NO. (TYP)
ZONE NO. (TYP)
TP-B
U-B2A 175H
U-B2B 175H
B2R1 1K
SHT 3
B1
U-D2B 1 172H
U-D2D 8 172H
U-D2C 1 172H
54234200
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2GLV
CODE IDENT 19333
C
DWG NO 54234200
CD 1
SHEET 2

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TYPE 2GLV

CODE IDENT		DWG NO	CD
19333	C	54234200	1

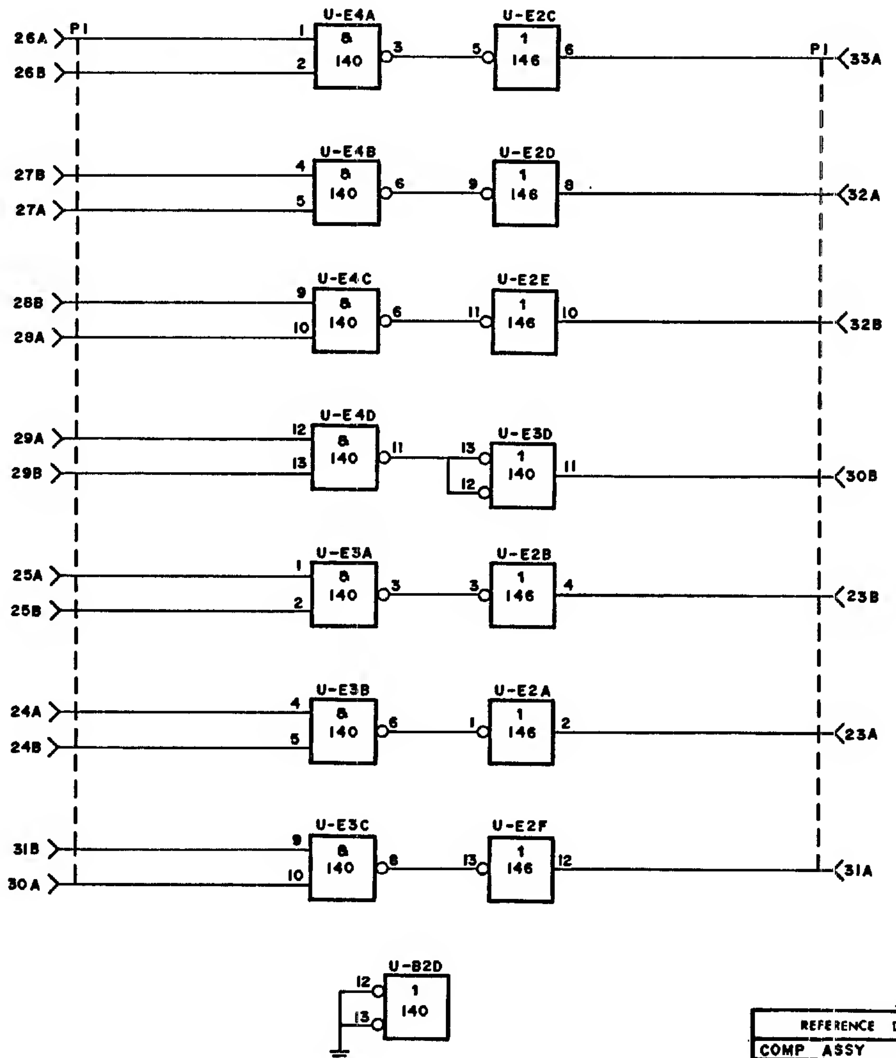
SHEET 3

54234200

70629100 E

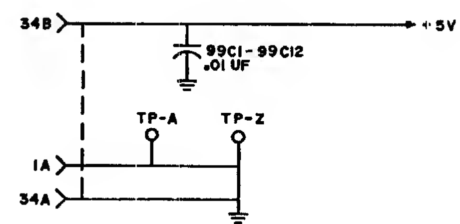
70629100 E

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. IC TYPE 166 HAS PIN 6 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.



B54235000

REFERENCE DRAWINGS			
COMP ASSY	54234900		
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

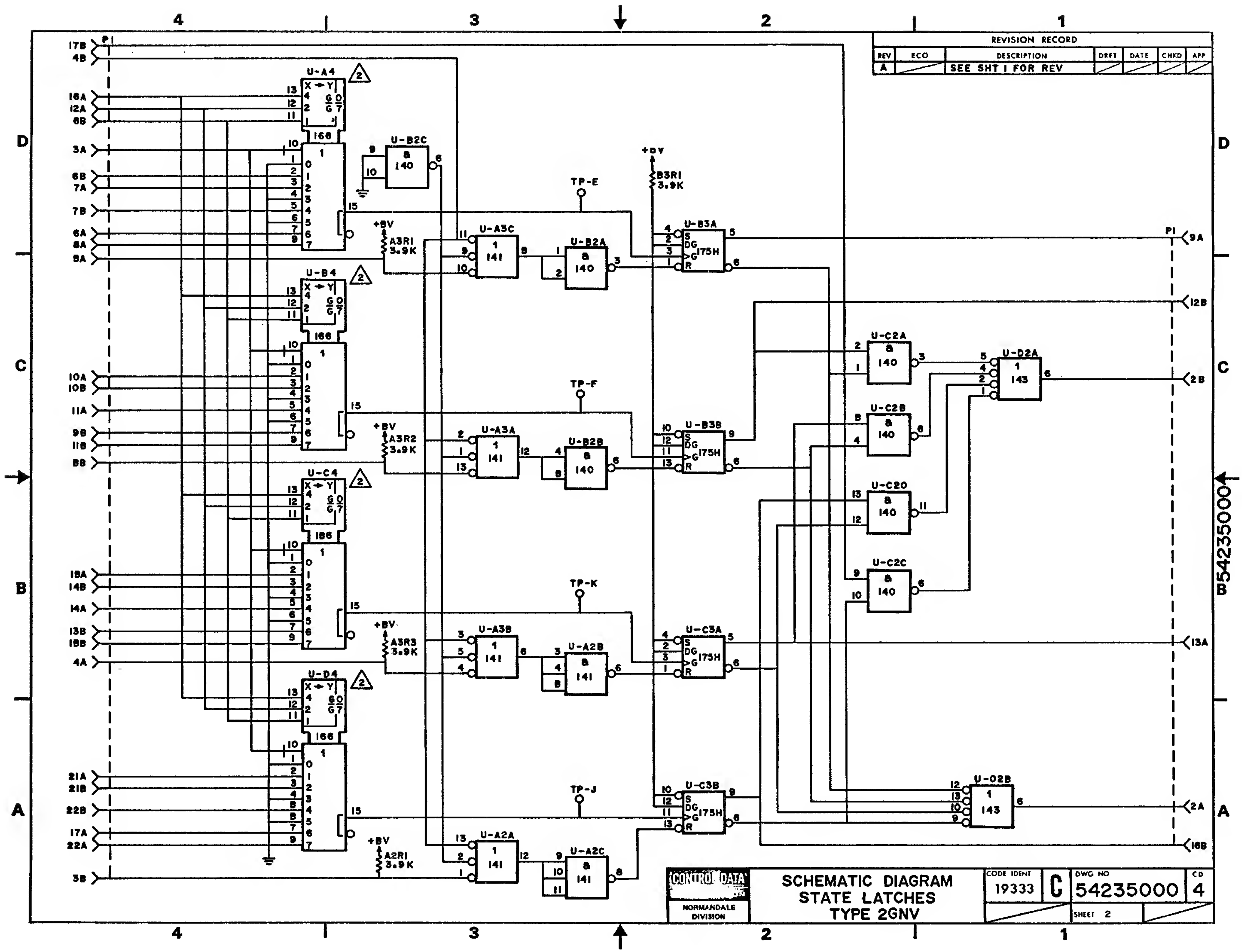
FIRST USED ON	BR3A6
DWN	K STREETER 3-23-72
CHK	9-7-72
ENGR	9-7-72
MFG	
APPR	9/14/72

TITLE: SCHEMATIC DIAGRAM STATE LATCHES TYPE 2GNV

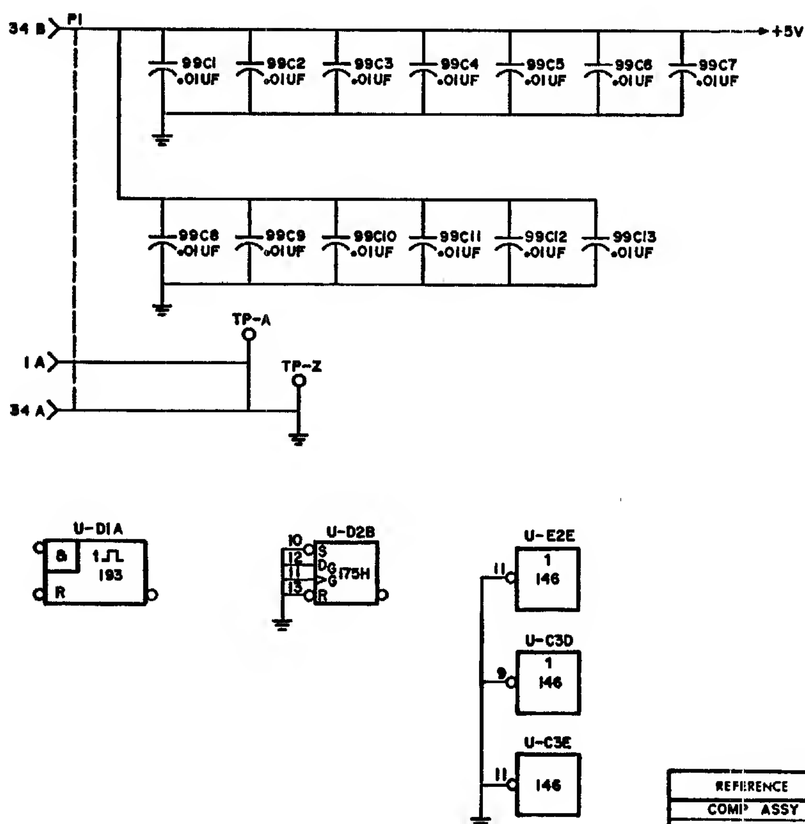
CODE IDENT 19333 | C | DRAWING NUMBER 54235000 | CD 4

SHEET 1 OF 2

HPO1


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHT 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
STATE LATCHES
TYPE 2GNV
CODE IDENT 19333
C
DWG NO 54235000
CD 4
SHEET 2

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
			REVISION RECORD				
	A	PE23000	RELEASED				
	B	PE30859	VALUE & DELAY TIME CHG	SZ	10-30-72	DMS	II



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
3. DELAY TIME FOR REFERENCE ONLY.

54235400

REFERENCE DRAWINGS		
COMP ASSY 54235300		
COMPONENTS, EXCEPT AS NOTED		
TOLERANCE	VALUE	RATING
RES ±5%	OHMS	1/4W
CAP ±10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

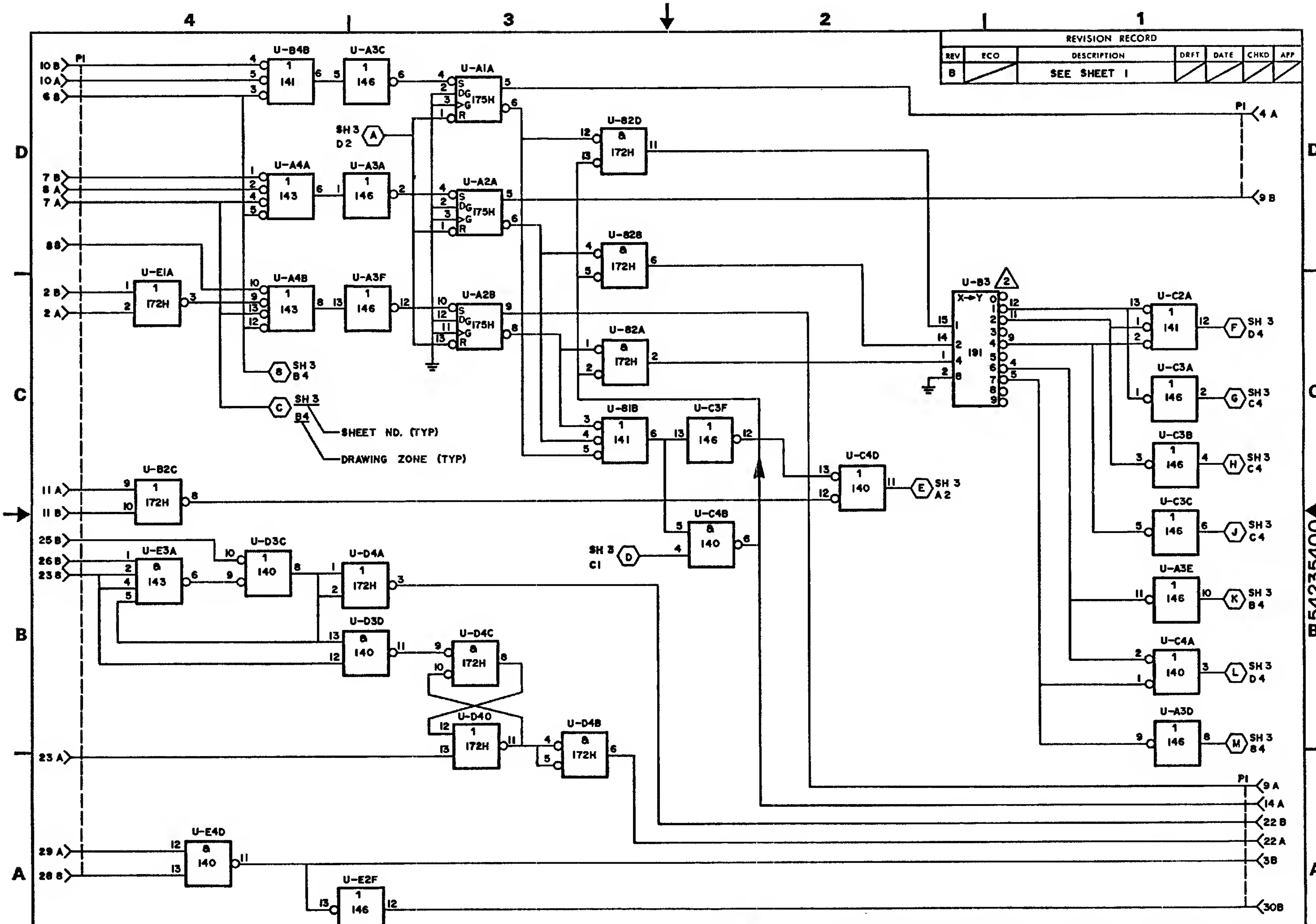
FIRST USED ON	BR3A6	
DWN	D.G. TUTTLE	6-24-72
CHK		9-7-72
ENGR		9-8-72
MFG		9-14-72
APPR		9/14/72

TITLE
SCHEMATIC DIAGRAM MONITOR LATCH & CONTROL TYPE 2GPV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54235400	6

SHEET 1 OF 3

HPD



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				

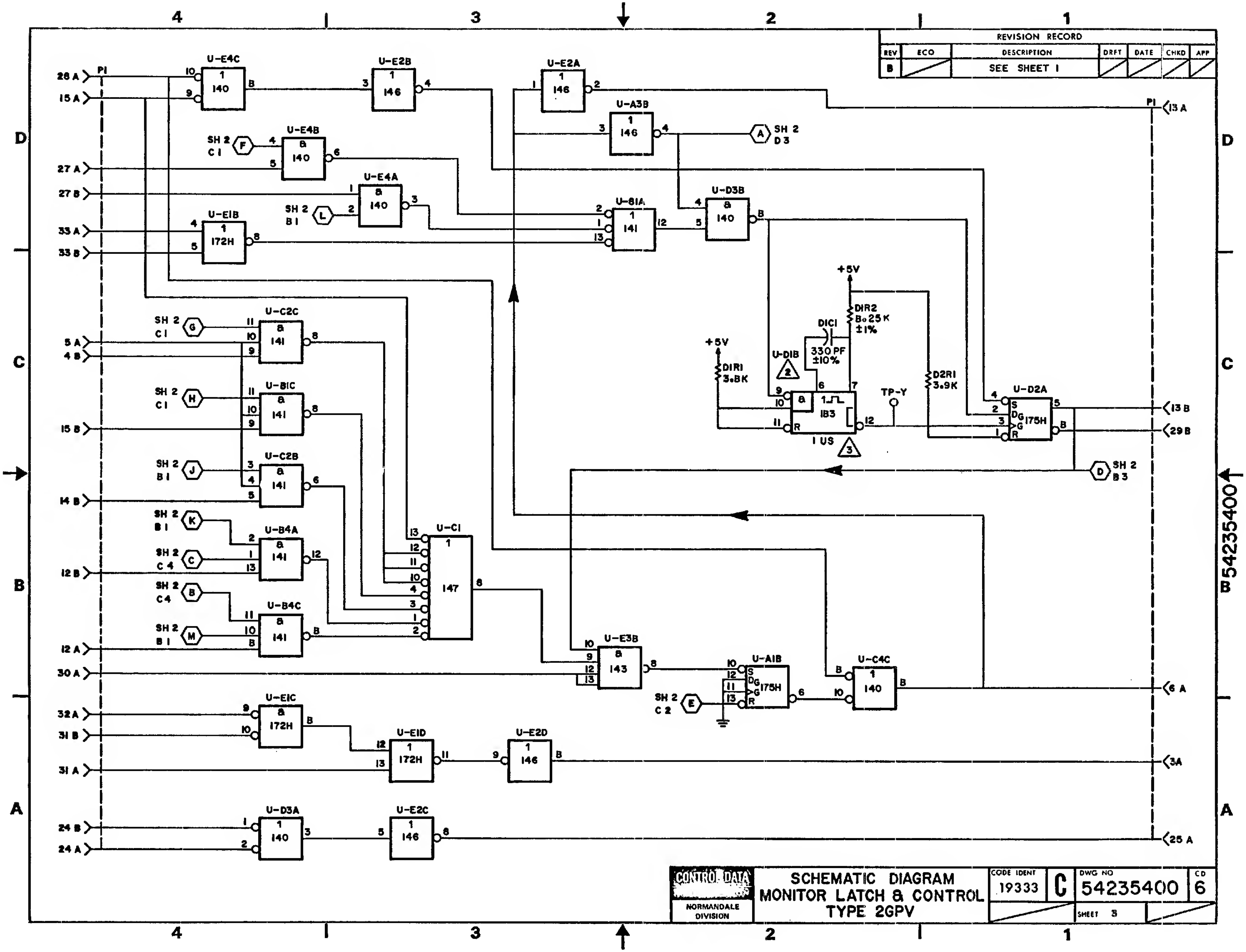
CONTROL DATA NORMANDALE DIVISION

SCHEMATIC DIAGRAM
MONITOR LATCH & CONTROL
TYPE 2GPV

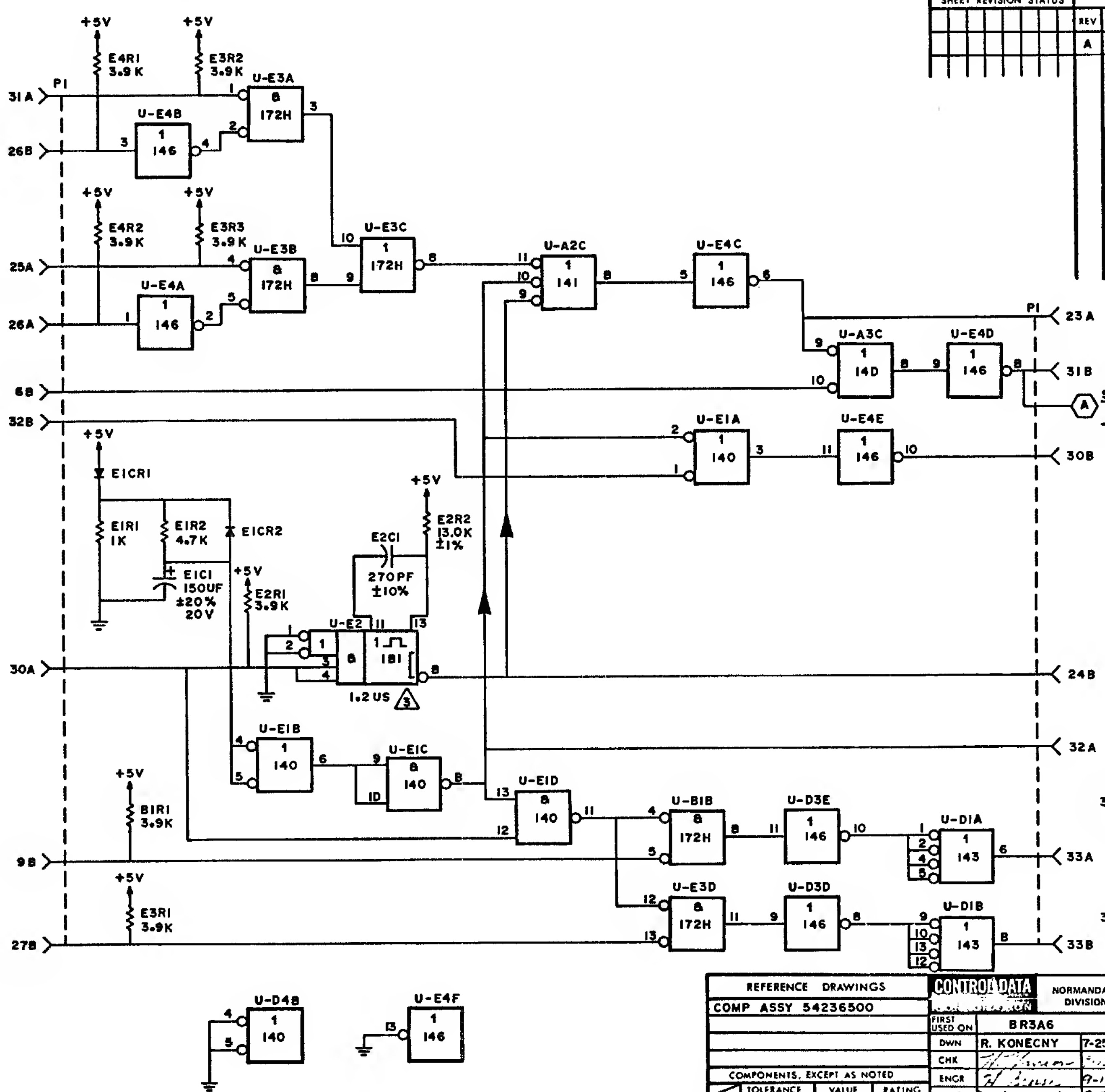
CODE IDENT 19333 C DWG NO 54235400 CD 6

SHEET 2

54235400


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
B | SEE SHEET I
U-E4C
U-E2B
U-E2A
U-A3B
U-E4B
U-E4A
U-E1B
U-B1A
U-D3B
U-C2C
U-B1C
U-C2B
U-B4A
U-B4C
U-C1
U-E3B
U-A1B
U-C4C
U-E1C
U-E1D
U-E2D
U-D3A
U-E2C
U-D1B
U-D2A
+5V
D1R2 8.25K ±1%
D1C1 330 PF ±10%
D1R1 3.8K
D2R1 3.9K
TP-Y
1 US
SH 2 D3
SH 2 B3
SH 2 C2
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
MONITOR LATCH & CONTROL
TYPE 2GPV
CODE IDENT 19333
C
DWG NO 54235400
CD 6
SHEET 3
54235400

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
2. ALL DIODES SILICON, 92115021.
3. DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASSY 54236500

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	−30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	R. KONECNY	7-25-72
CHK	[illegible]	[illegible]
ENGR	[illegible]	9-19-72
MFG	[illegible]	9-21-72
APPR	[illegible]	[illegible]

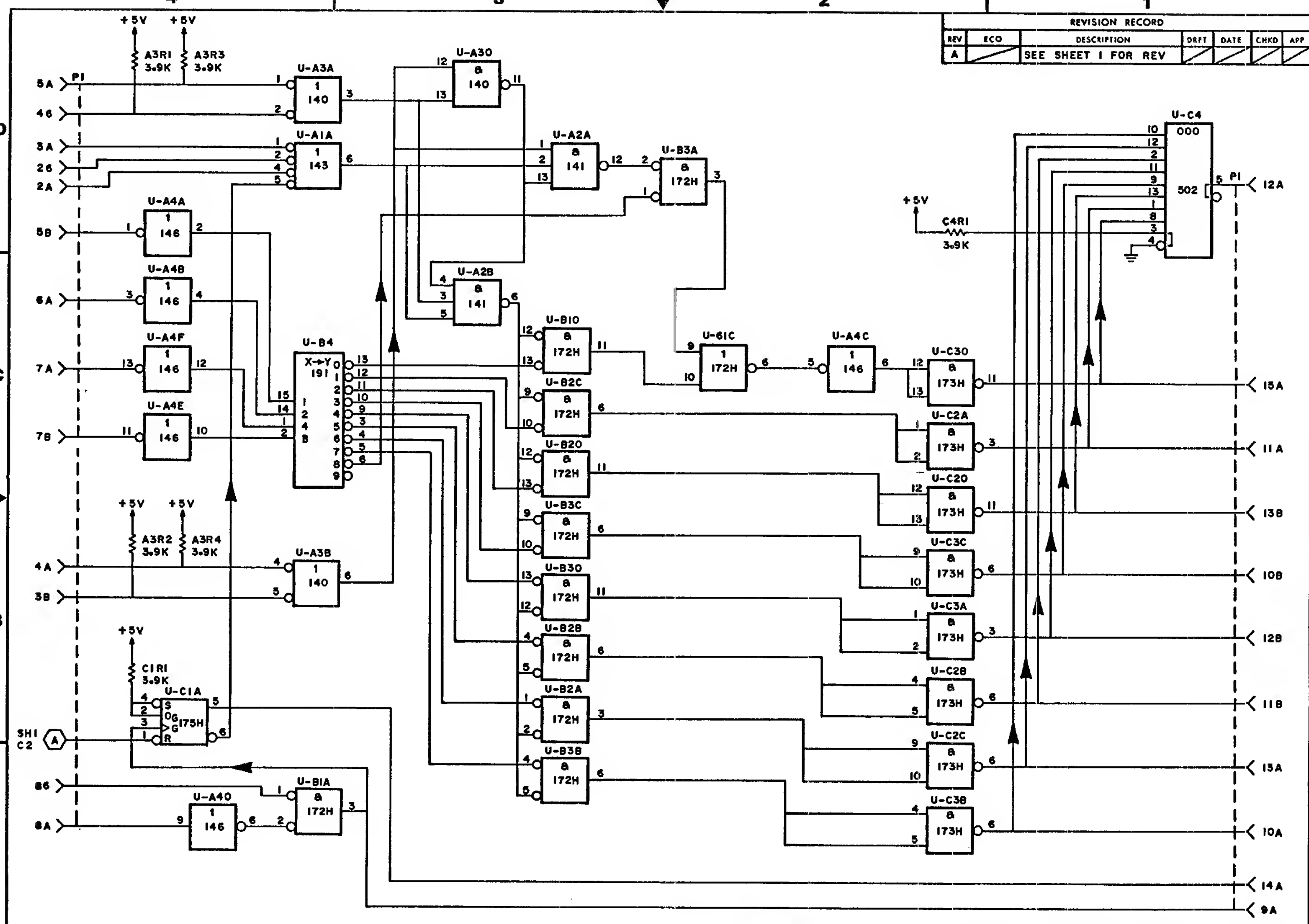
TITLE: SCHEMATIC DIAGRAM INTERRUPT/RESET LOGIC, PARITY GENERATOR TYPE 2GSV

CODE IDENT 19333 — C — DRAWING NUMBER 54236600 — CD 0

SHEET 1 OF 3

54236600

HPD



CONTROL DATA NORMANDALE DIVISION

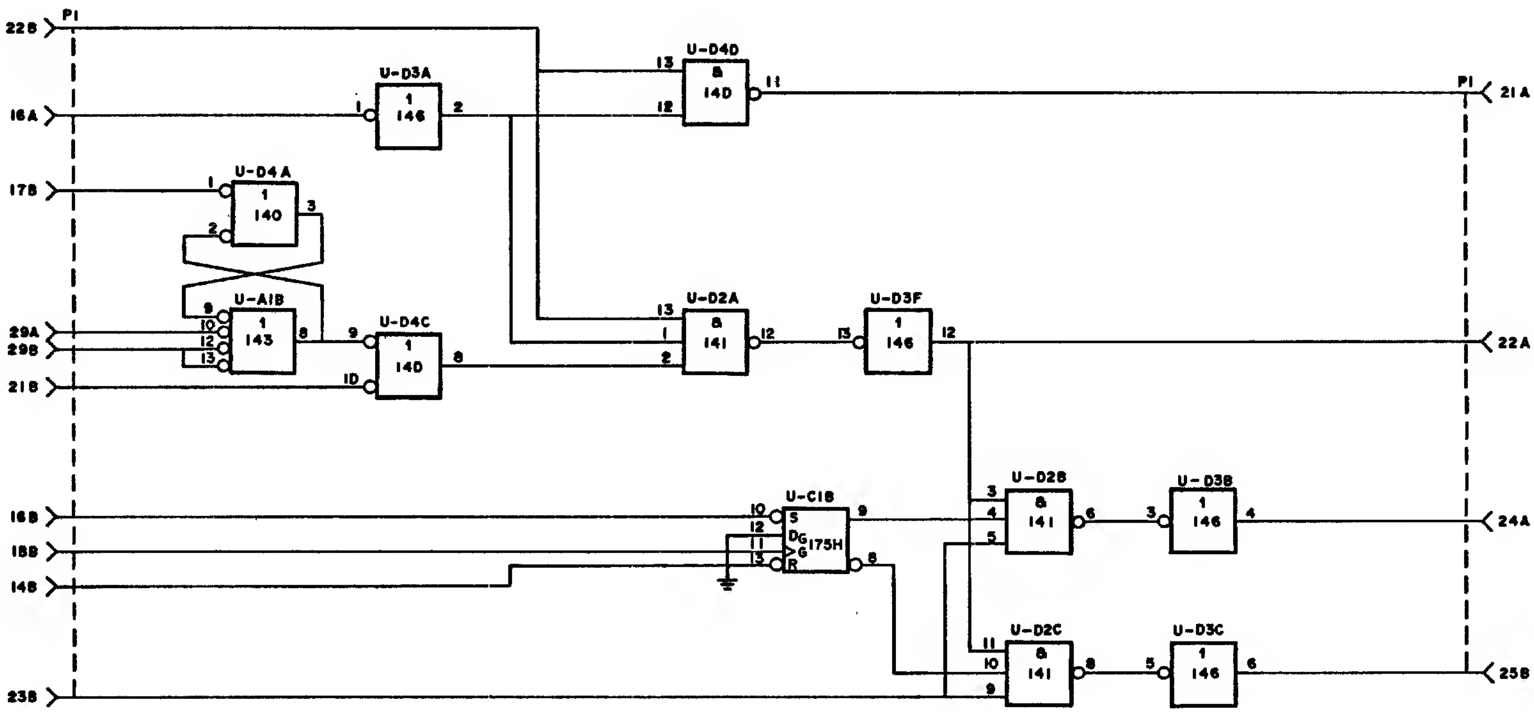
SCHEMATIC DIAGRAM TYPE 2GSV

CODE IDENT		DWG NO	CD
19333	C	54236600	0

SHEET 2

54236600

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



54236600

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TYPE 2GSV

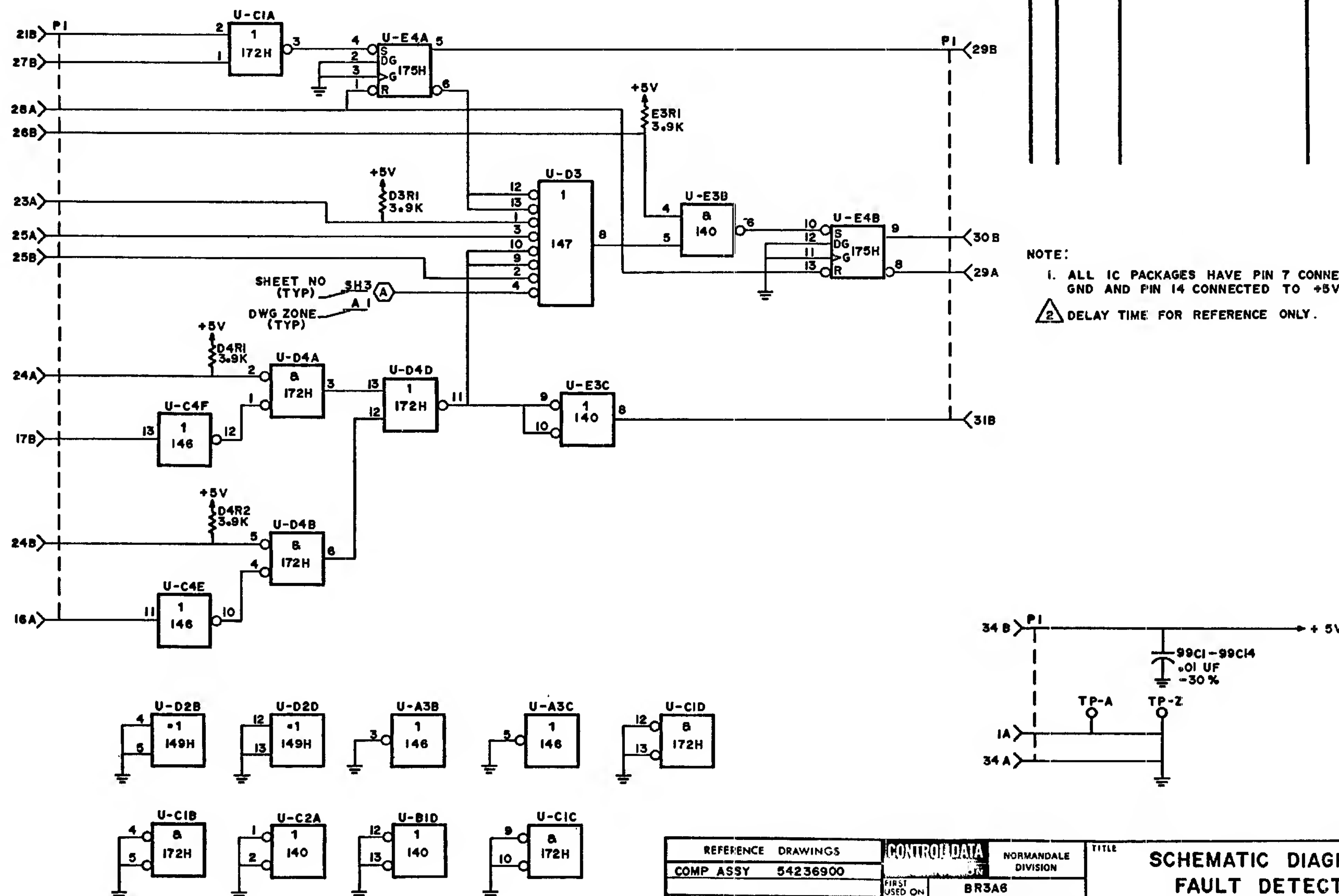
CODE IDENT		DWG NO	CD
19333	C	54236600	0
		SHEET 3	

70629100 E

SHEET REVISION STATUS							

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED				



NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS	
COMP ASSY	54236900

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON: BR3A6

DWN		7-24-72
CHK		7-31-72
ENGR		8-7-72
MFG		9-7-72
APPR		9/5/72

TITLE

SCHEMATIC DIAGRAM FAULT DETECT TYPE 2GTV

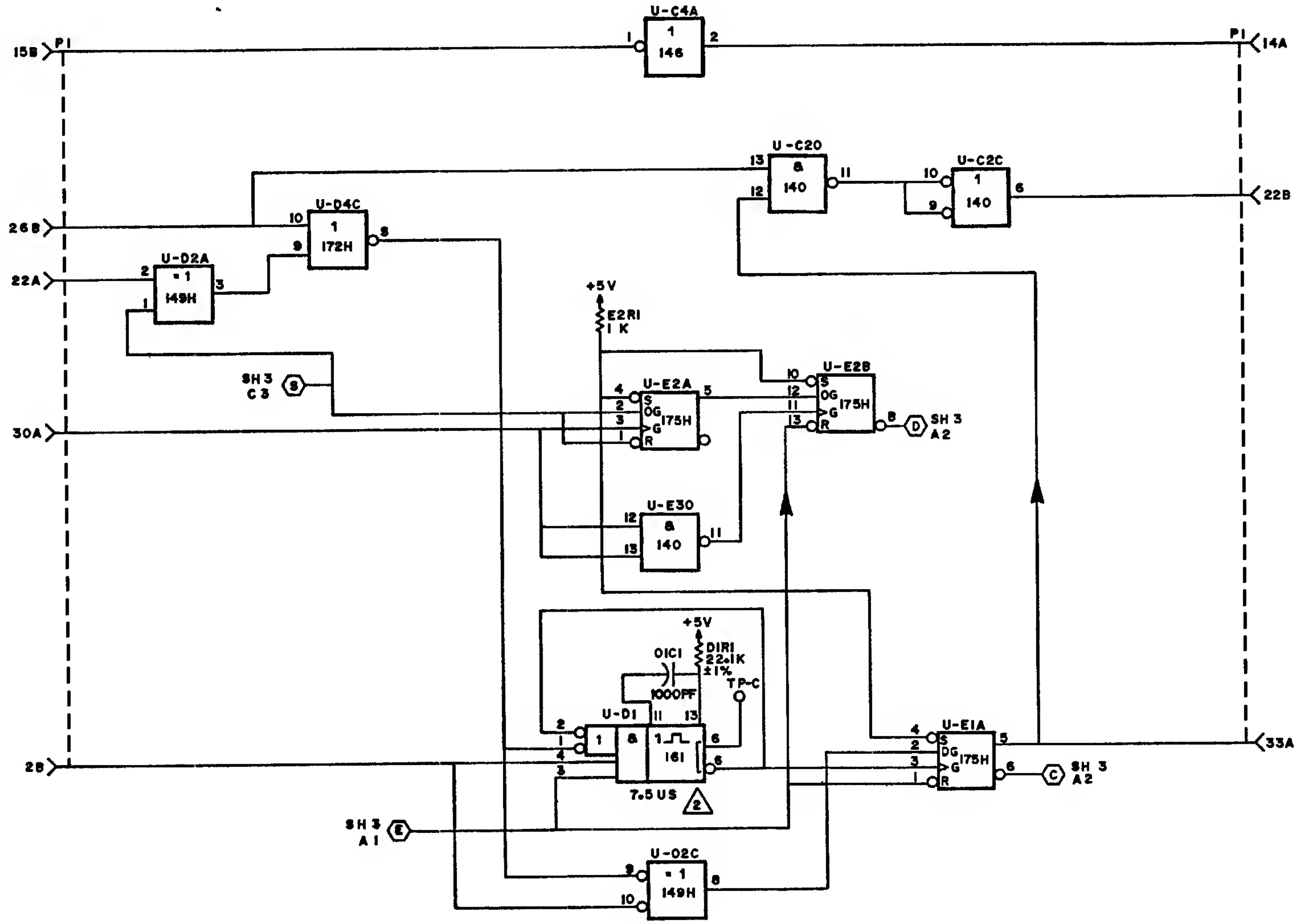
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54237000	2

SHEET 1 OF 3

HPD

B54237000

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT I FOR REV				

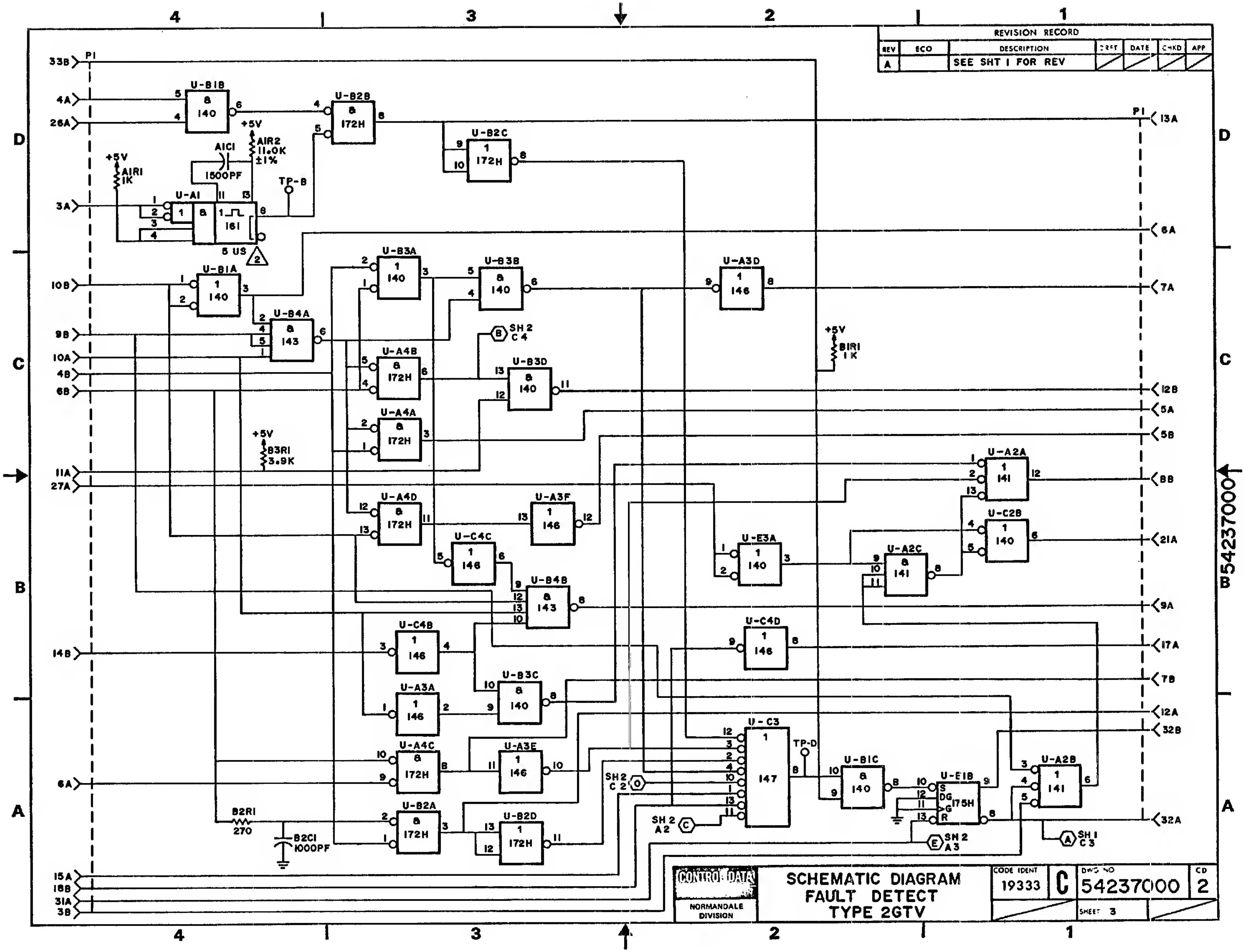


54237000

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 2GTV

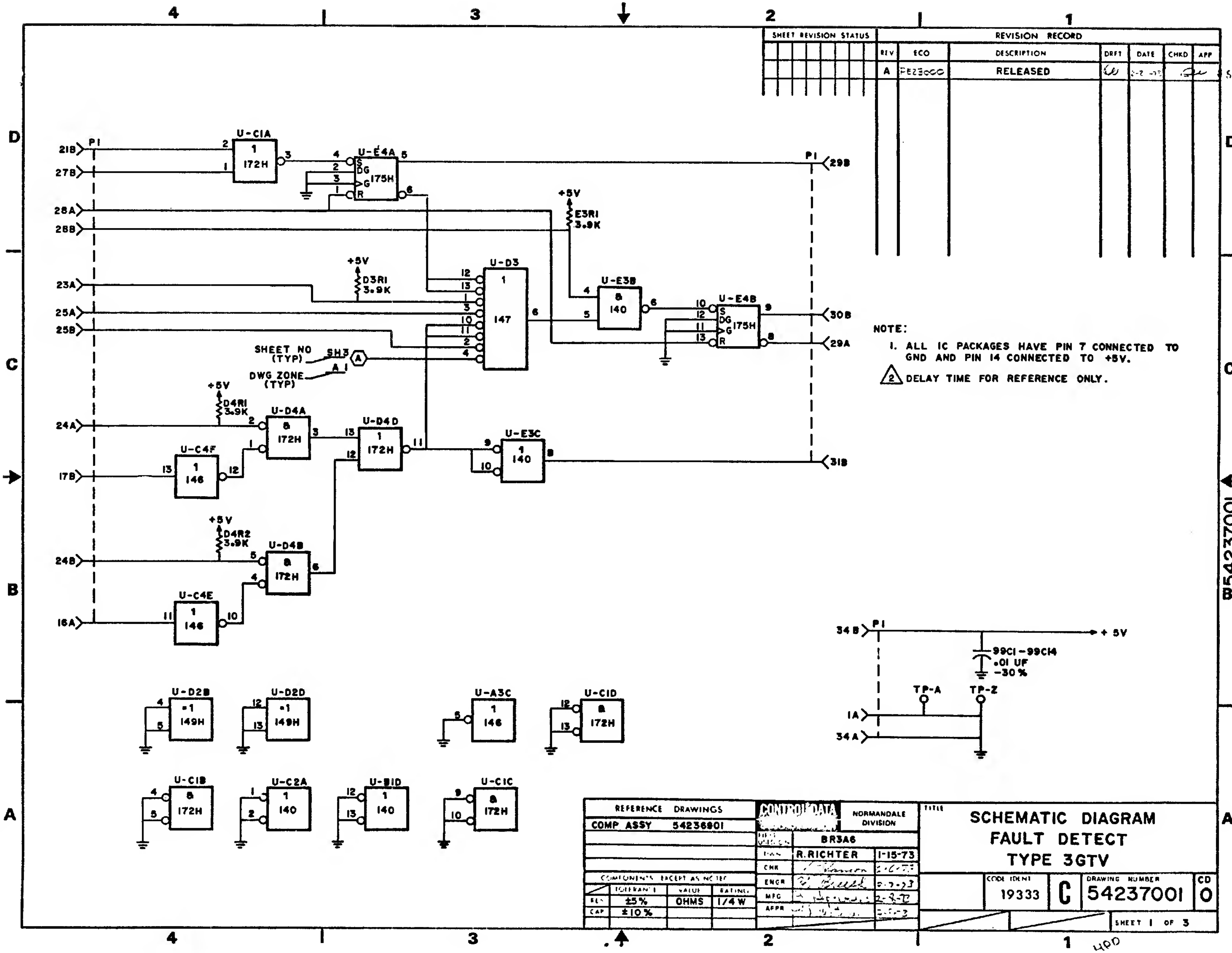
CODE IDENT		DWG NO	CD
19333	C	54237000	2
		SHEET 2	



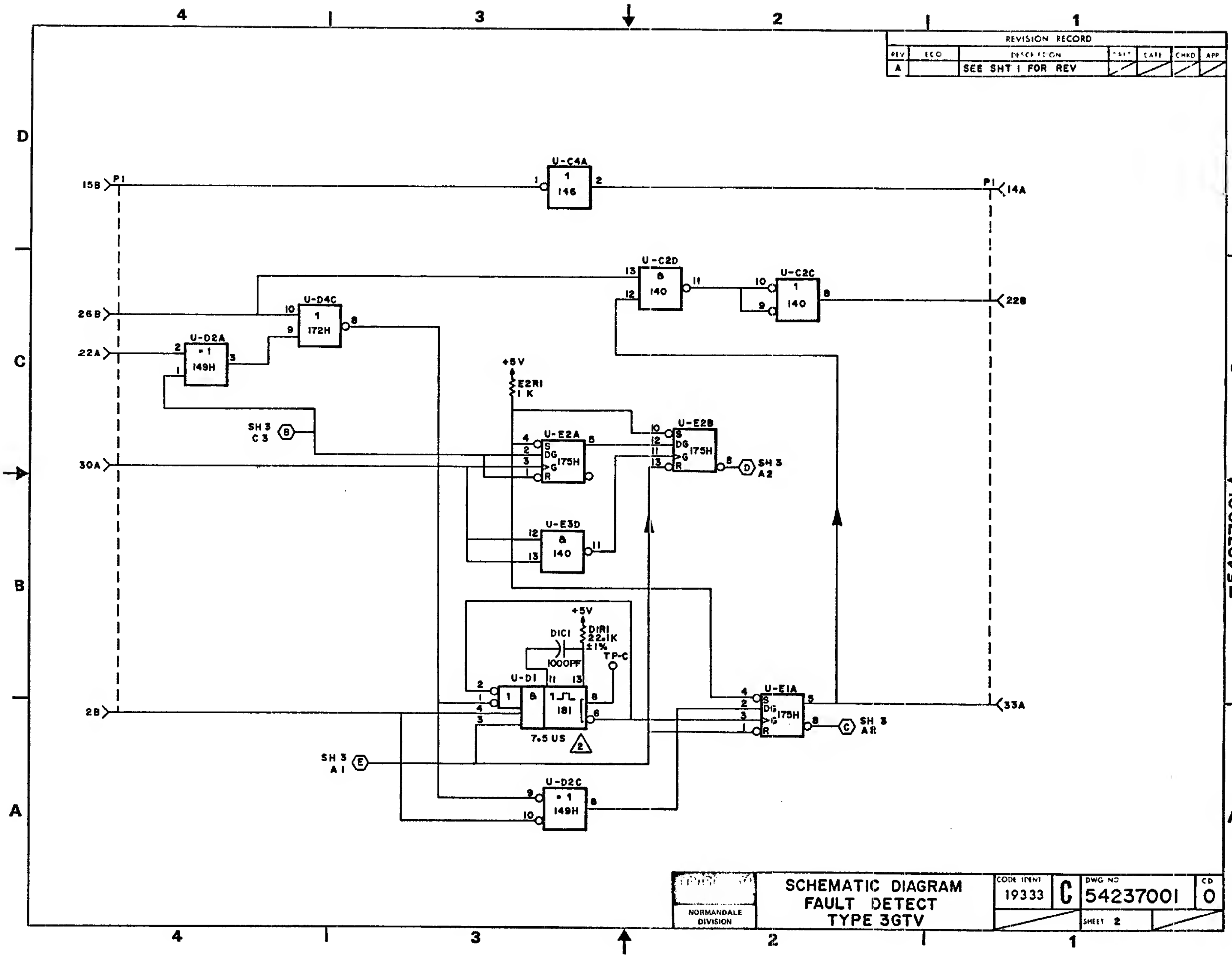
CONTROL DATA
NORMANDALE DIVISION

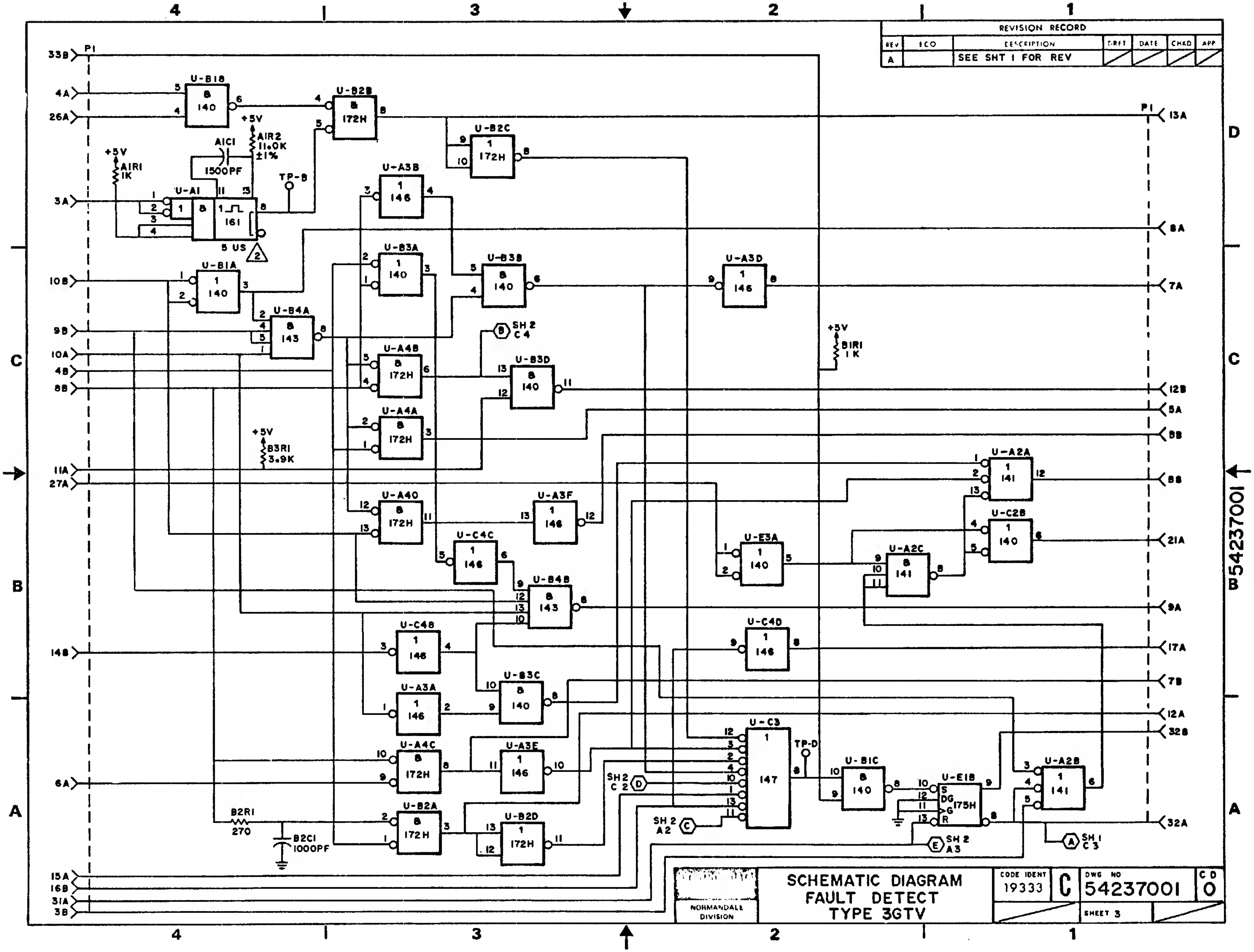
SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 2GTV

CODE IDENT		DWG NO	CD
19333	C	54237000	2
		SHEET 3	


REVISION RECORD
A FE23000 RELEASED
NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2 DELAY TIME FOR REFERENCE ONLY.
SHEET NO (TYP)
DWG ZONE (TYP)
REFERENCE DRAWINGS
COMP ASSY 54236801
CONTROL DATA NORMANDALE DIVISION
BR3A6
R.RICHTER 1-15-73
COMPONENTS EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHMS 1/4 W
CAP ±10%
SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 3GTV
CODE IDENT 19333
C
DRAWING NUMBER 54237001
CD 0
SHEET 1 OF 3
54237001

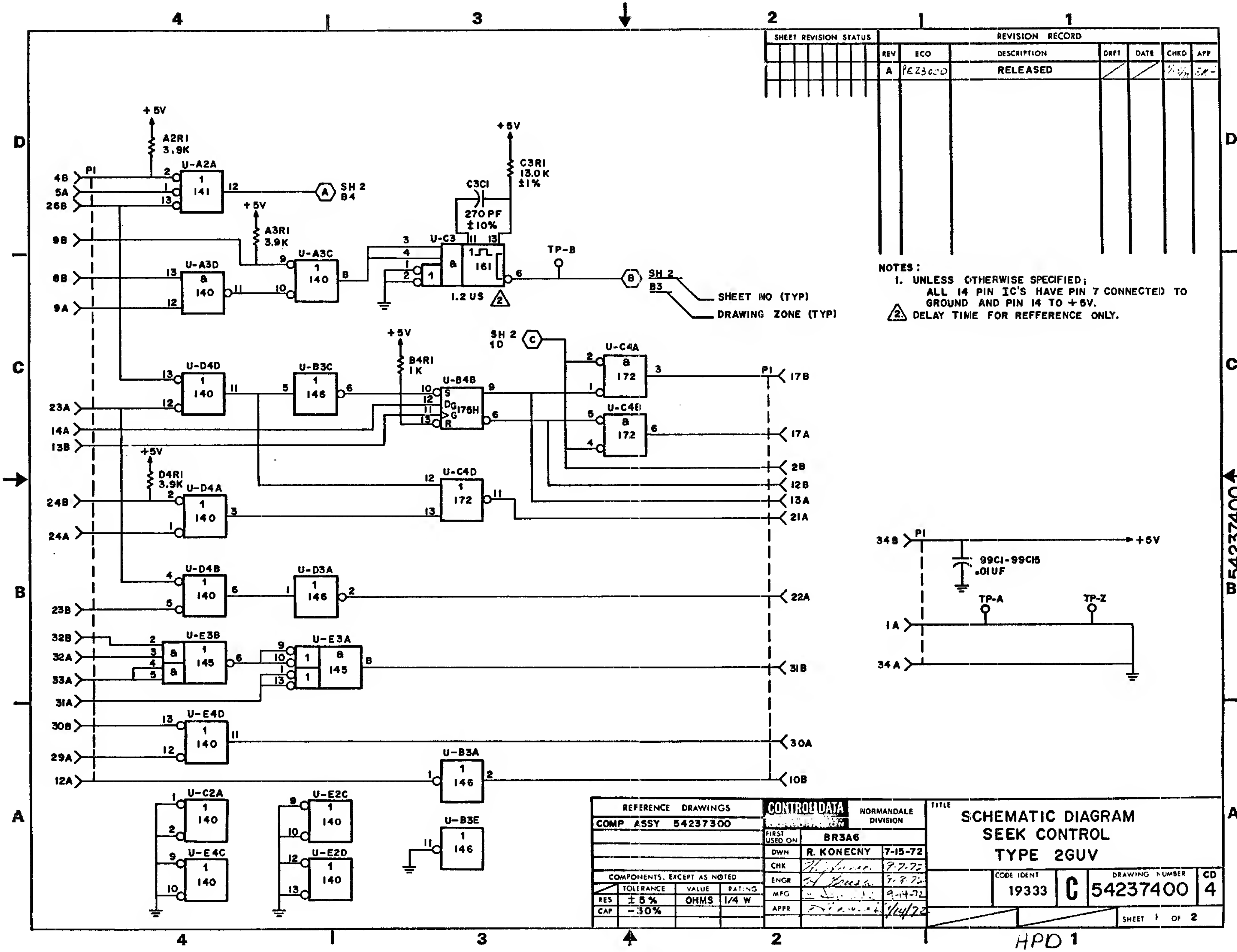
70629100 E


REVISION RECORD
REV
ECO
DESCRIPTION
DATE
CHKD
APP
A
SEE SHT 1 FOR REV
U-C4A
1
146
15B
P1
14A
U-C2D
&
140
U-C2C
1
140
22B
26B
U-D4C
1
172H
22A
U-D2A
=1
149H
+5V
E2R1
1 K
SH 3
C 3
U-E2A
175H
U-E2B
175H
SH 3
A 2
30A
U-E3D
&
140
+5V
D1C1
D1R1
22.1K
±1%
1000PF
TP-C
U-D1
181
7.5 US
2B
U-E1A
175H
33A
SH 3
A2
SH 3
A 1
U-D2C
=1
149H
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 3GTV
CODE IDENT
19333
C
DWG NO
54237001
0
SHEET 2
54237001

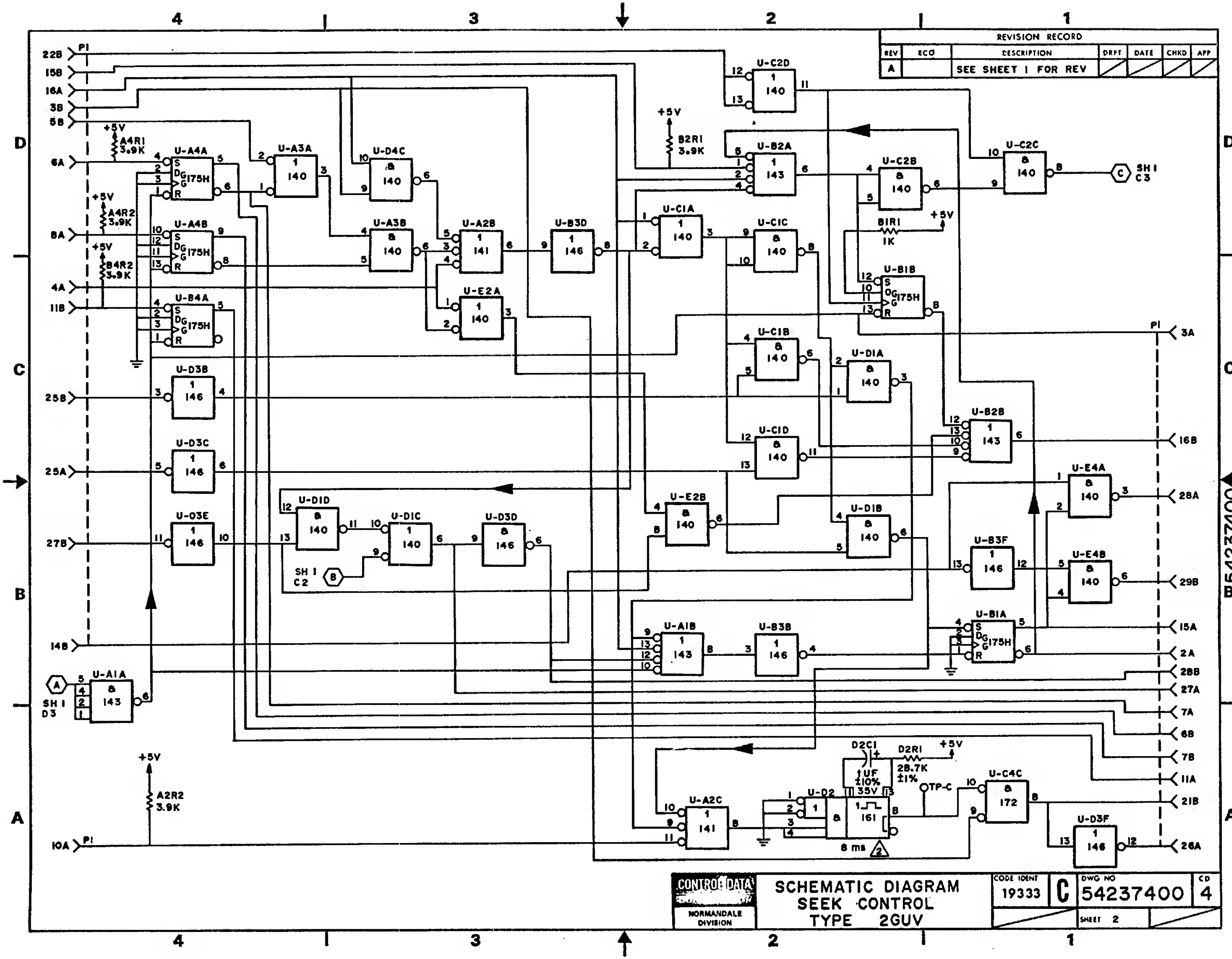

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHT 1 FOR REV
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 3GTV
CODE IDENT 19333
C
DWG NO 54237001
CD 0
SHEET 3
54237001

70629100 E

70629100 E



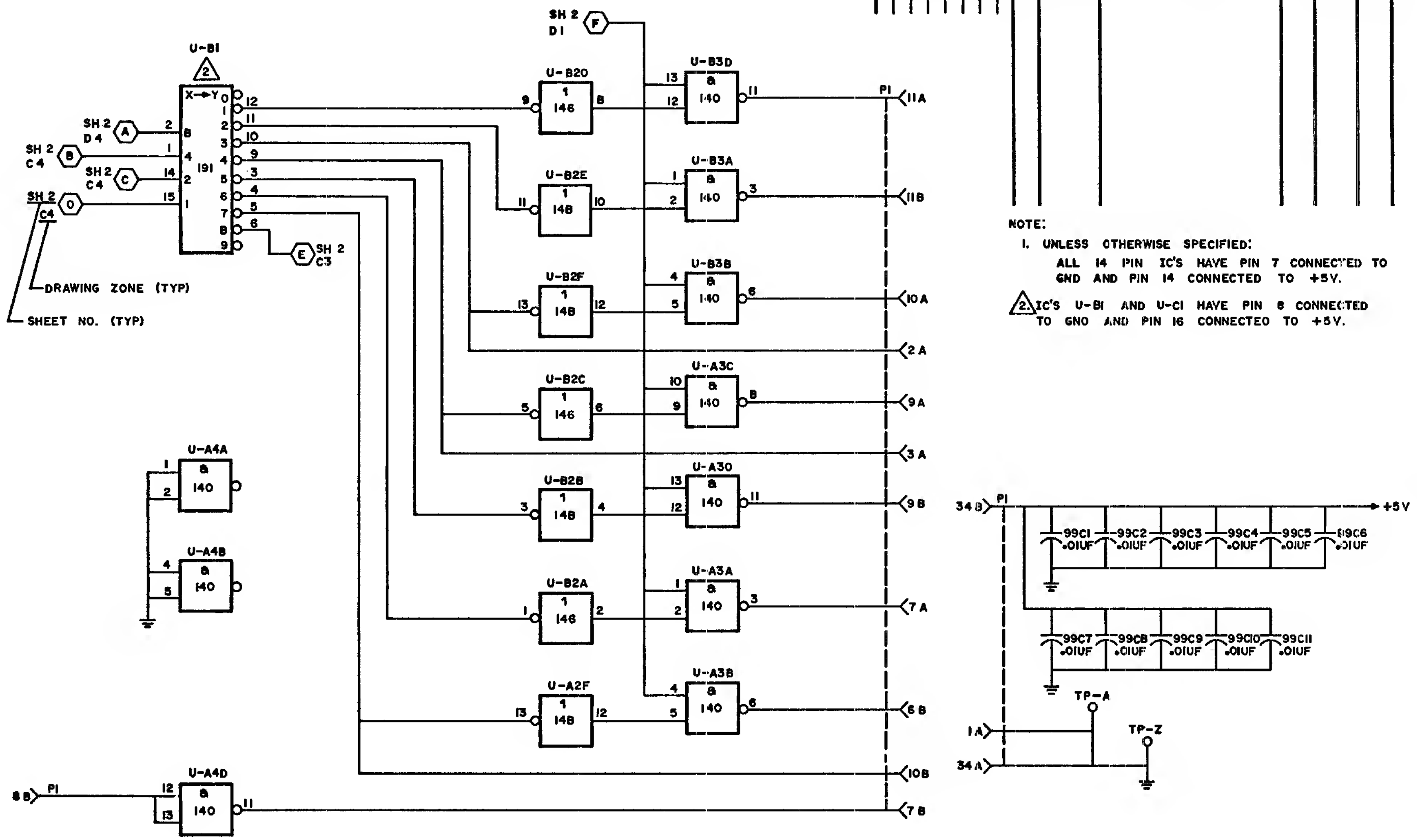
4-139


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
SEEK CONTROL
TYPE 2GUV
CODE IDENT 19333
C
DWG NO 54237400
CD 4
SHEET 2
54237400

SHEET REVISION STATUS							

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	523000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. IC'S U-B1 AND U-C1 HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.

REFERENCE DRAWINGS		
COMP ASSY 54237700		
COMPONENTS, EXCEPT AS NOTED		
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

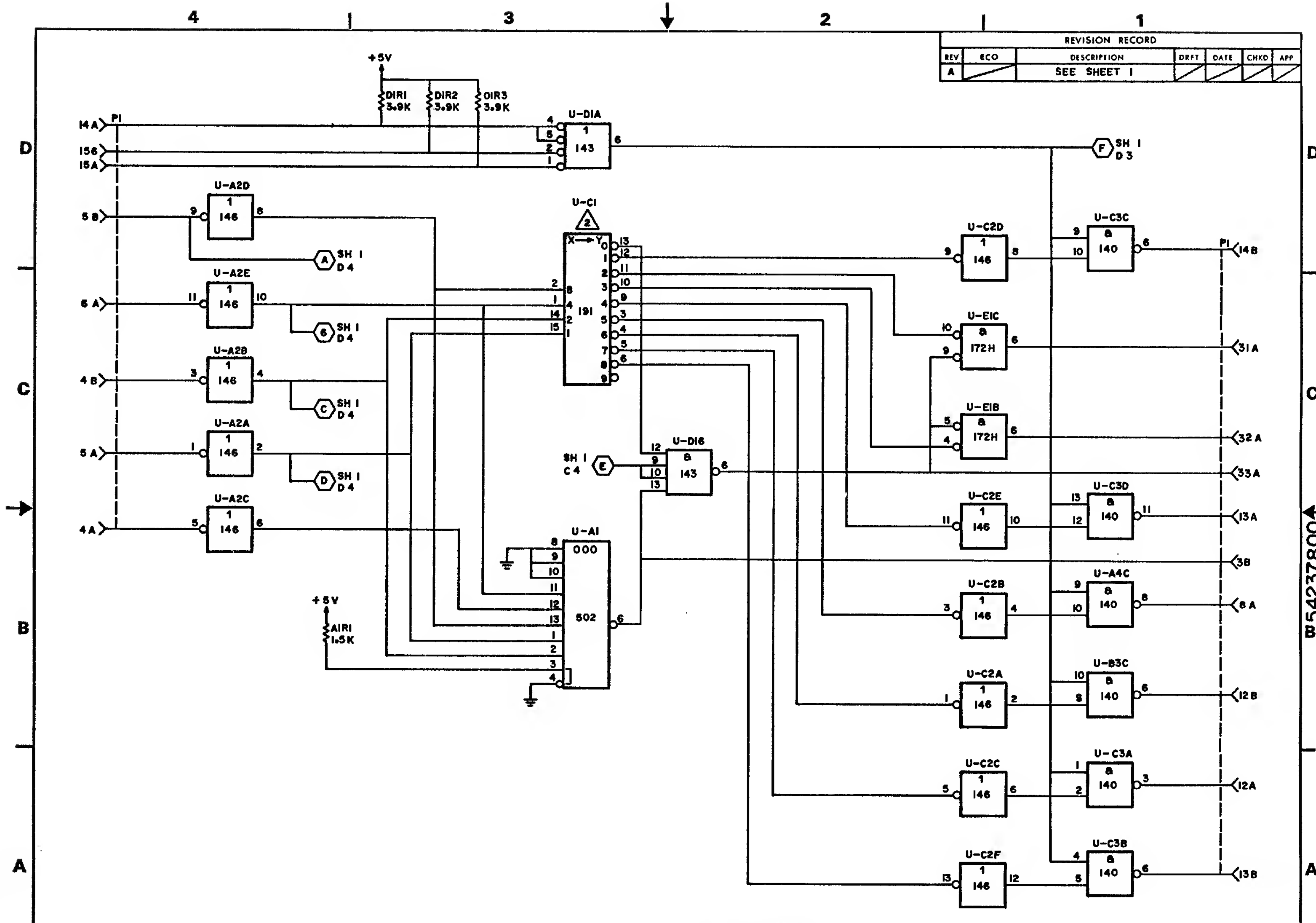
FIRST USED ON	BR3A6	
DWN	D. G. TUTTLE	7-10-72
CHK		7-27-72
ENGR		7-22-72
MFG		8-31-72
APPR		9/5/72

TITLE
SCHEMATIC DIAGRAM
TAG DECODE
TYPE 2GVV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54237800	5

SHEET 1 OF 3

54237800



REVISION RECORD

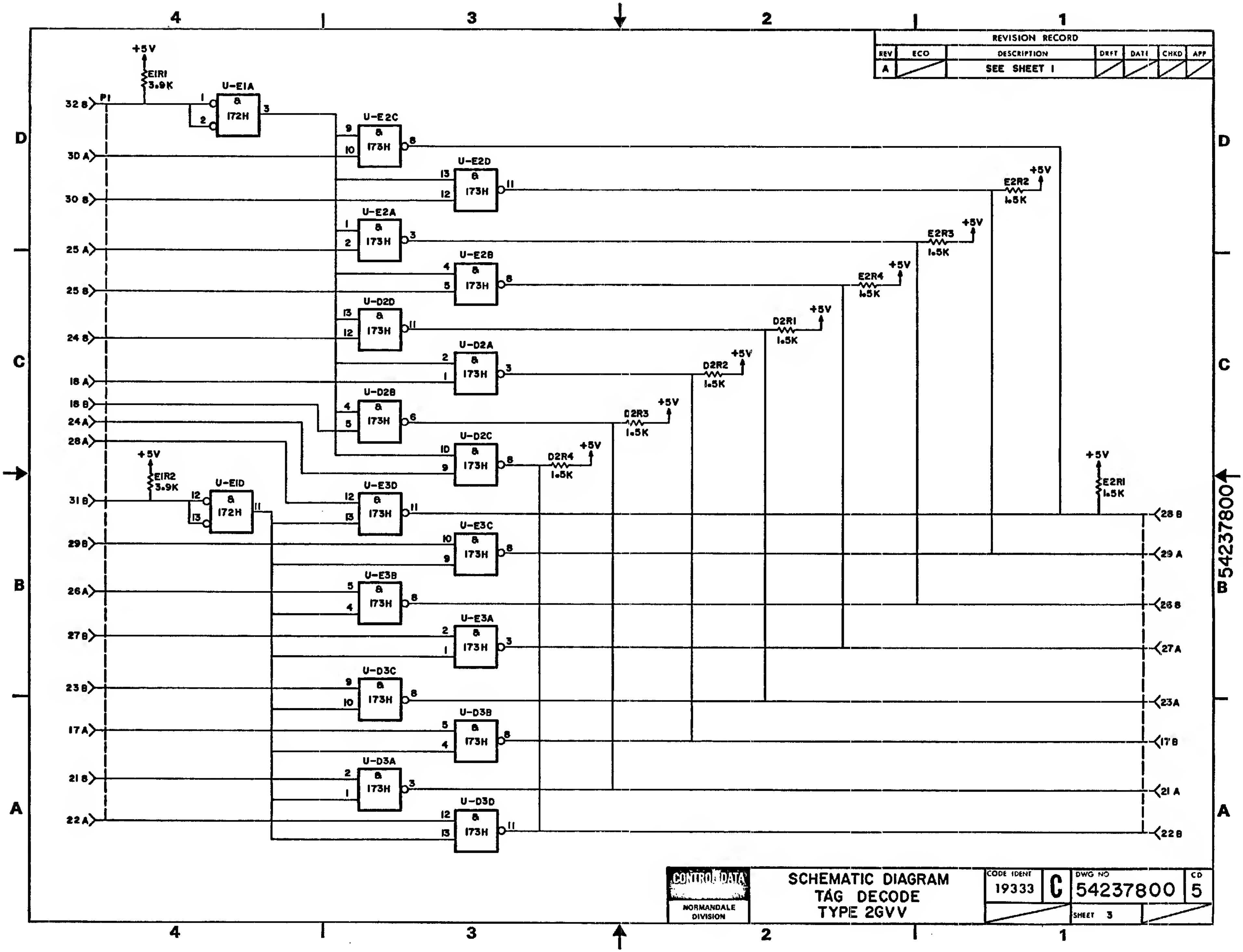
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TAG DECODE
TYPE 2GVV

CODE IDENT 19333 C
DWG NO 54237800 CD 5
SHEET 2

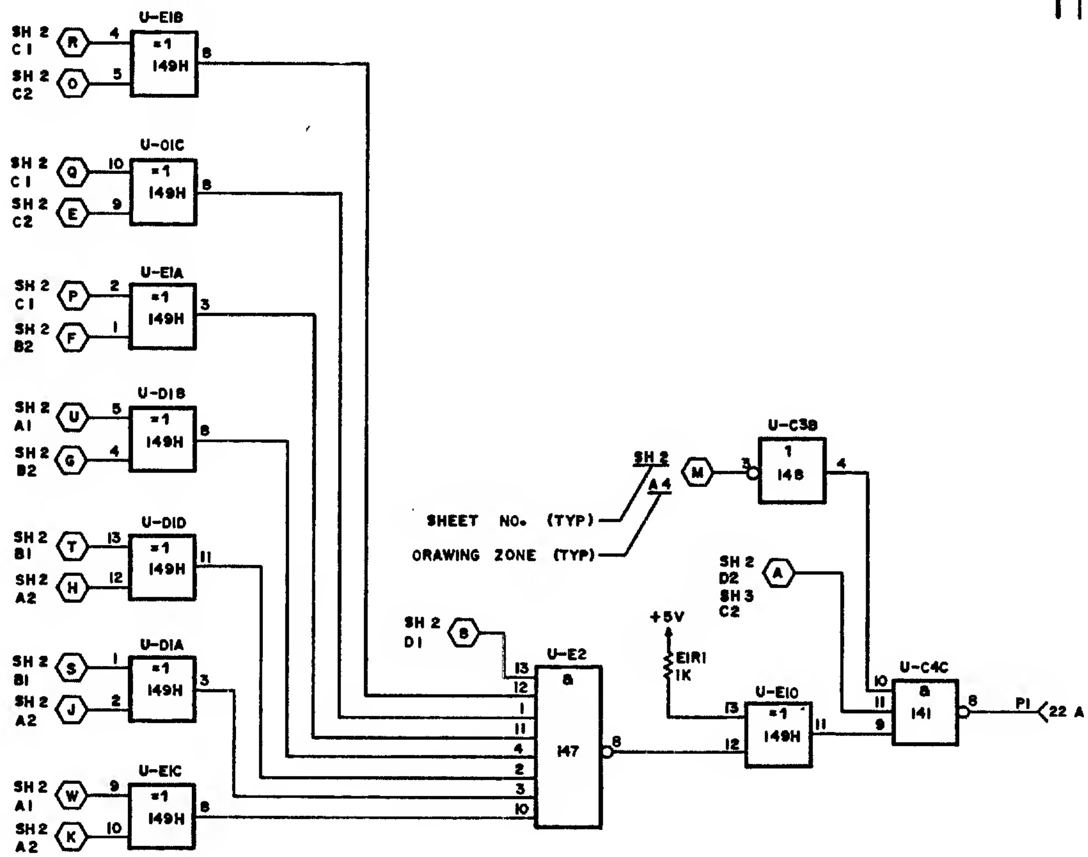
54237800


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1
+5V
E1R1 3.9K
E1R2 3.9K
P1
U-E1A 172H
U-E1D 172H
U-E2C 173H
U-E2D 173H
U-E2A 173H
U-E2B 173H
U-D2D 173H
U-D2A 173H
U-D2B 173H
U-D2C 173H
U-E3D 173H
U-E3C 173H
U-E3B 173H
U-E3A 173H
U-D3C 173H
U-D3B 173H
U-D3A 173H
U-D3D 173H
E2R1 1.5K
E2R2 1.5K
E2R3 1.5K
E2R4 1.5K
D2R1 1.5K
D2R2 1.5K
D2R3 1.5K
D2R4 1.5K
32B 30A 30B 25A 25B 24B 18A 18B 24A 28A 31B 29B 26A 27B 23B 17A 21B 22A
28B 29A 26B 27A 23A 17B 21A 22B
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TAG DECODE
TYPE 2GVV
CODE IDENT 19333
C
DWG NO 54237800
CD 5
SHEET 3
54237800

SHEET REVISION STATUS								

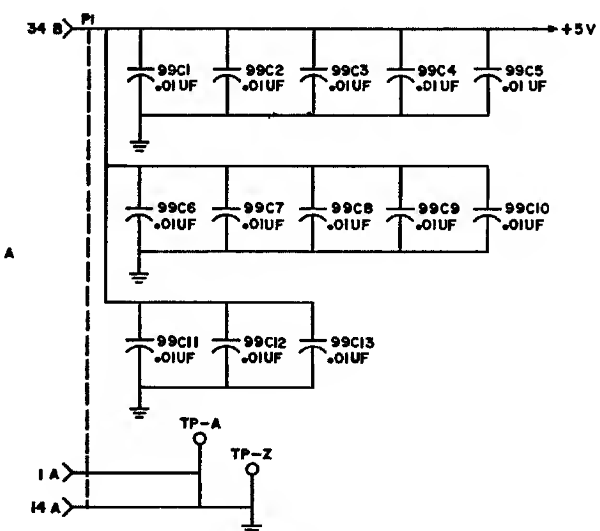
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED				
B	PE30907	CONNECTOR PIN CHANGED FROM 29A TO 29B	RKR	11-16-72		



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS			
COMP ASSY 54238100			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	D. G. TUTTLE	7-14-72
CHK		7-27-72
ENGR		8-30-72
MFG		9-7-72
APPR		9/5/72

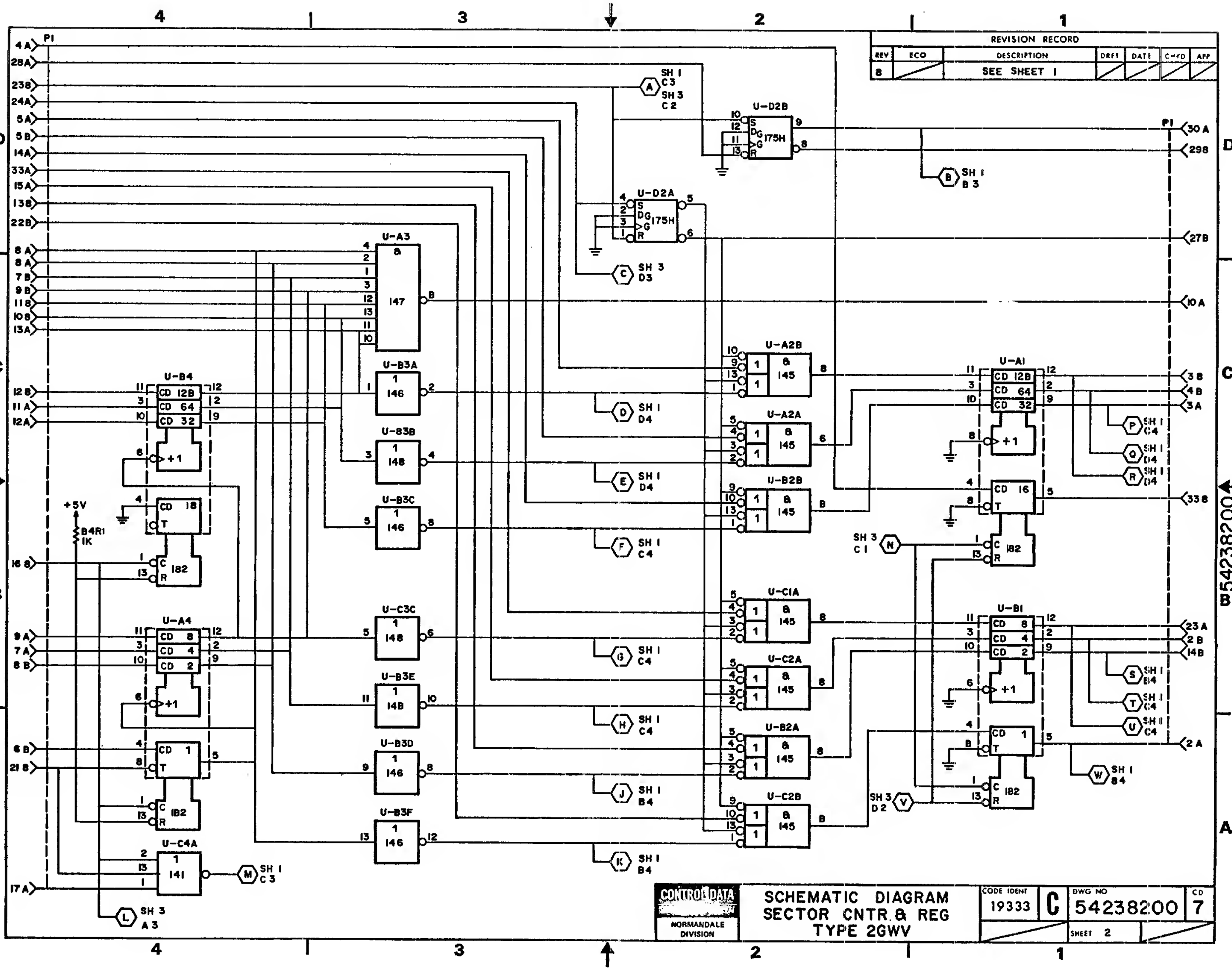
TITLE: SCHEMATIC DIAGRAM SECTOR CNTR & REG TYPE 2GWV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54238200	7

SHEET 1 OF 3

HPD

54238200

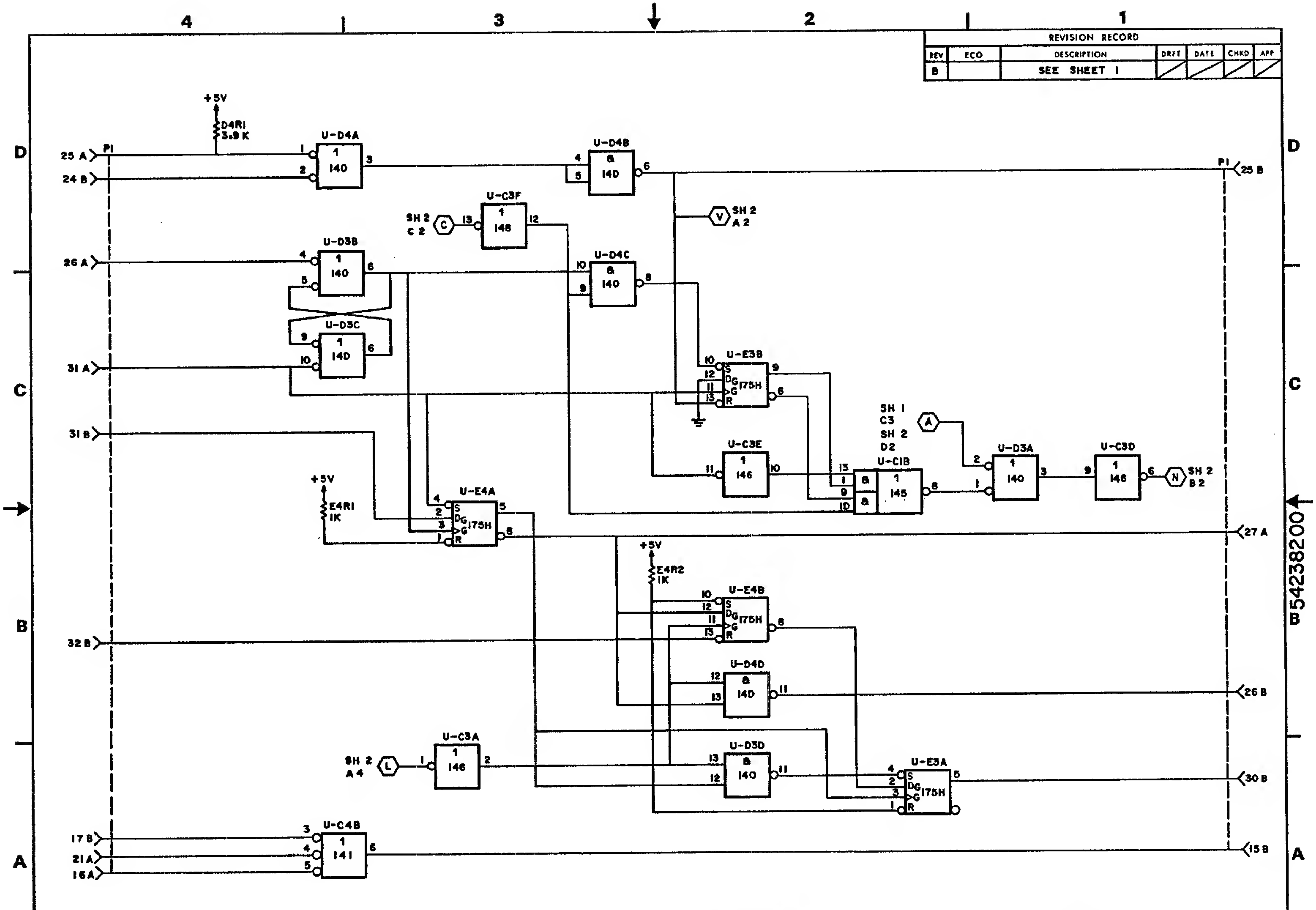


CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
SECTOR CNTR & REG
TYPE 2GWV

CODE IDENT 19333 | C | DWG NO 54238200 | CD 7
SHEET 2

54238200



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
SECTOR CNTR & REG
TYPE 2GWV

CODE IDENT 19333 | C | DWG NO 54238200 | CD 7

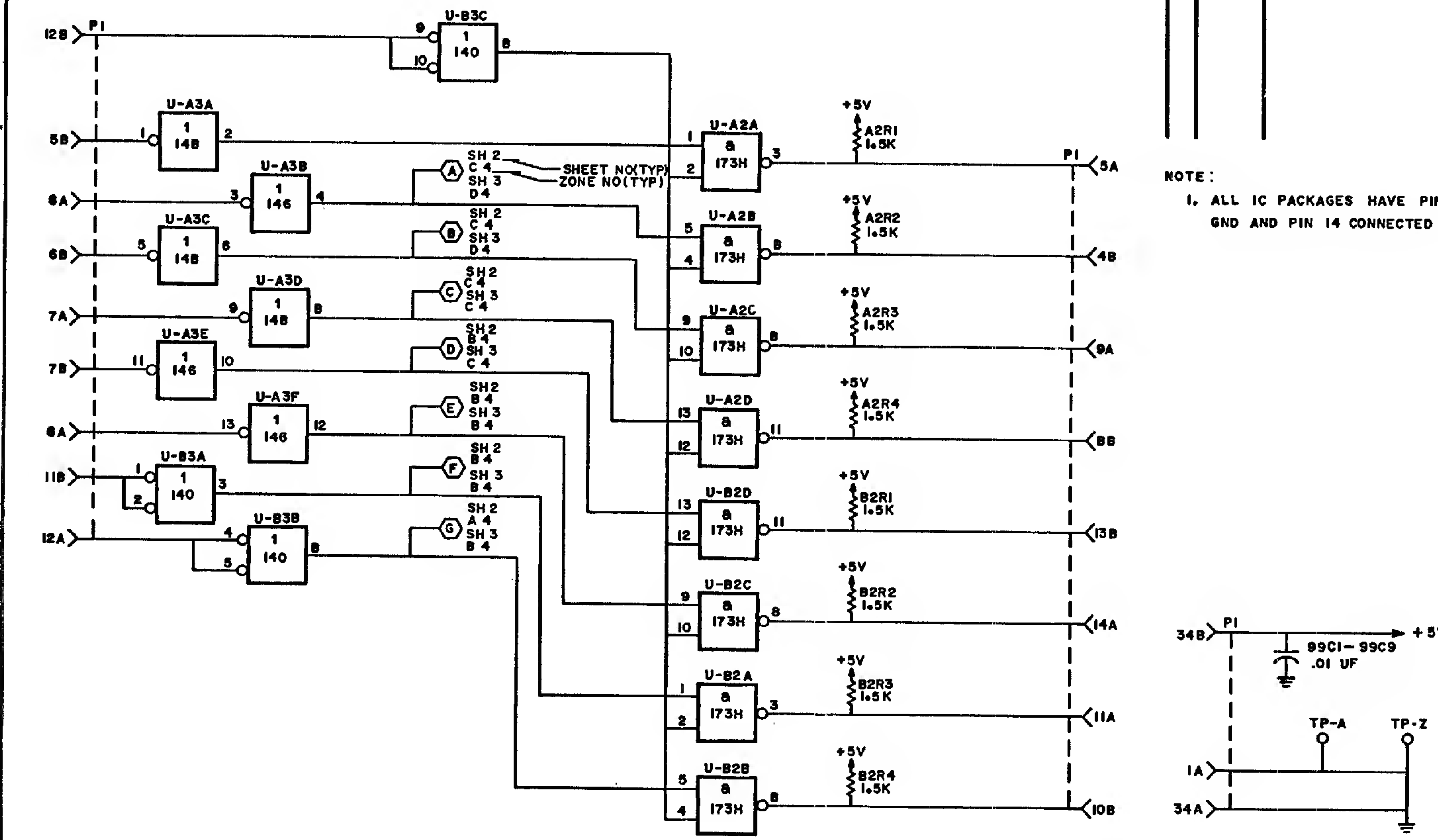
SHEET 3

54238200

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE2[illegible]	RELEASED			[illegible]	[illegible]

NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS	
COMP ASSY	54238500

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3A6	
DWN	K STREETER	7-1-72
CHK	[illegible]	7-27-72
ENGR	[illegible]	9-22-72
MFG	[illegible]	9-21-72
APPR	[illegible]	7/5/72

TITLE

SCHEMATIC DIAGRAM INPUT STEERING TYPE 2GXV

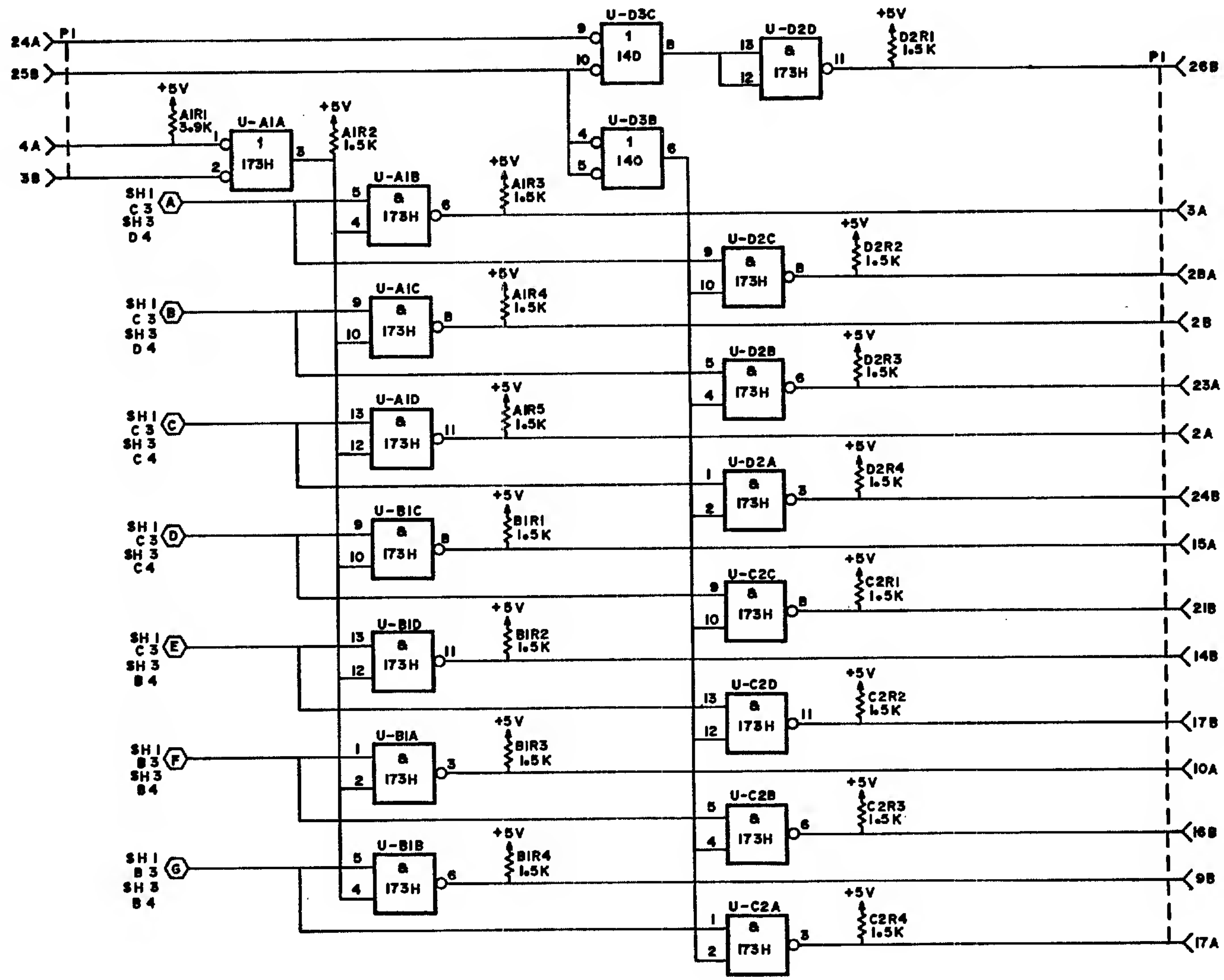
CODE IDENT		DRAWING NUMBER	CD
19333	C	54238600	8

SHEET 1 OF 3

HPD

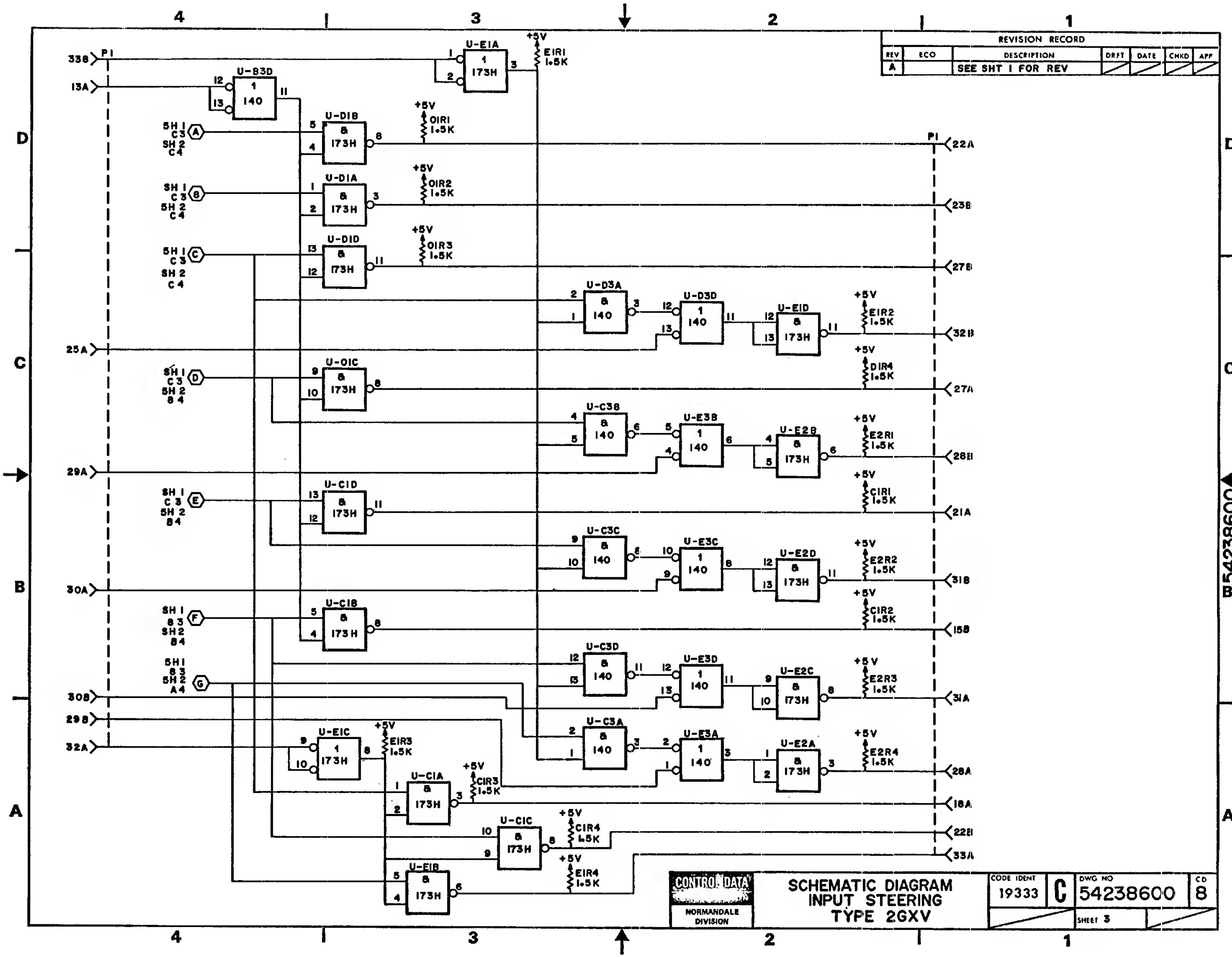
B54238600

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

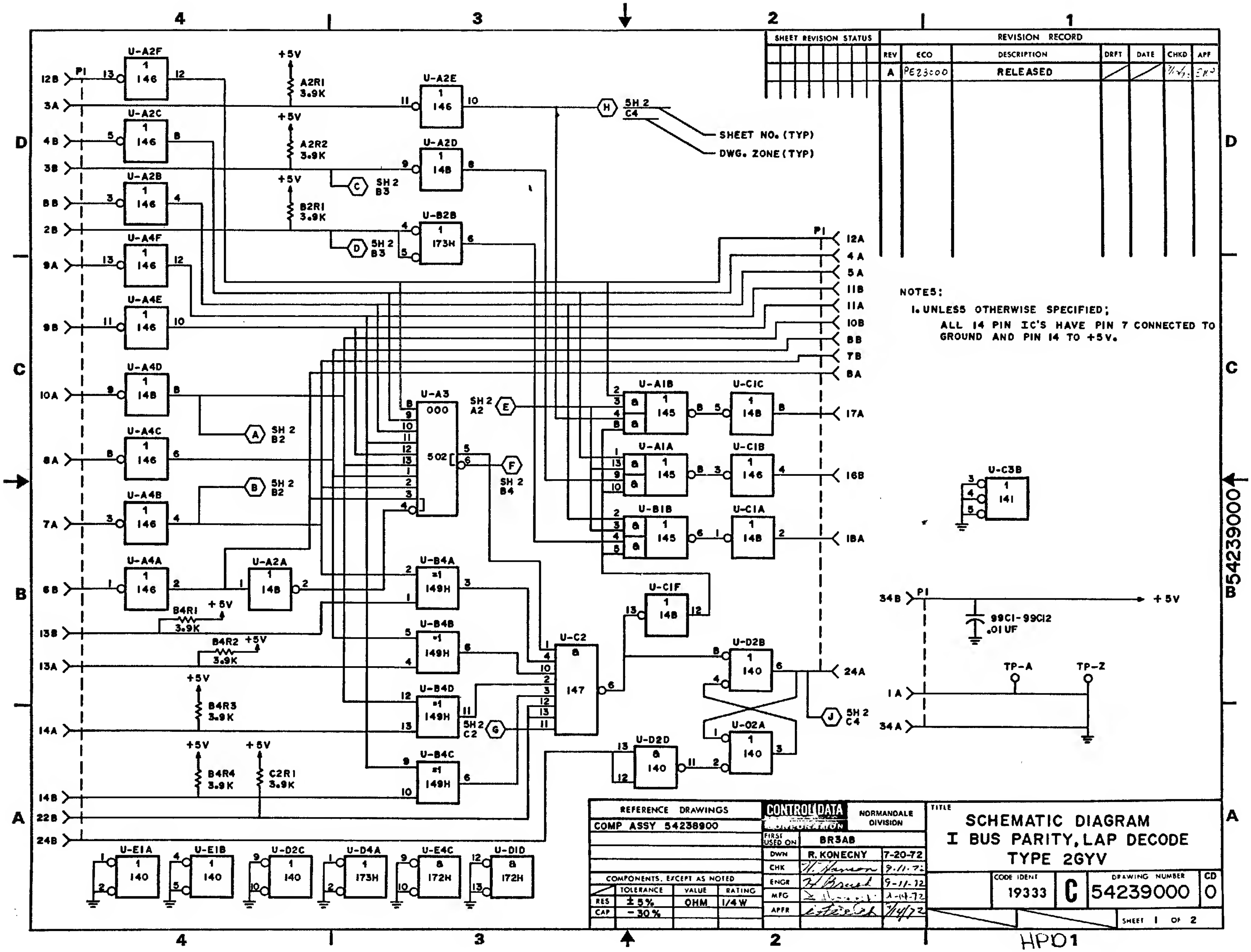


CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM INPUT STEERING TYPE 2GXV	CODE IDENT 19333	C	DWG NO 54238600	CD 8
				SHEET 2	

70629100 E

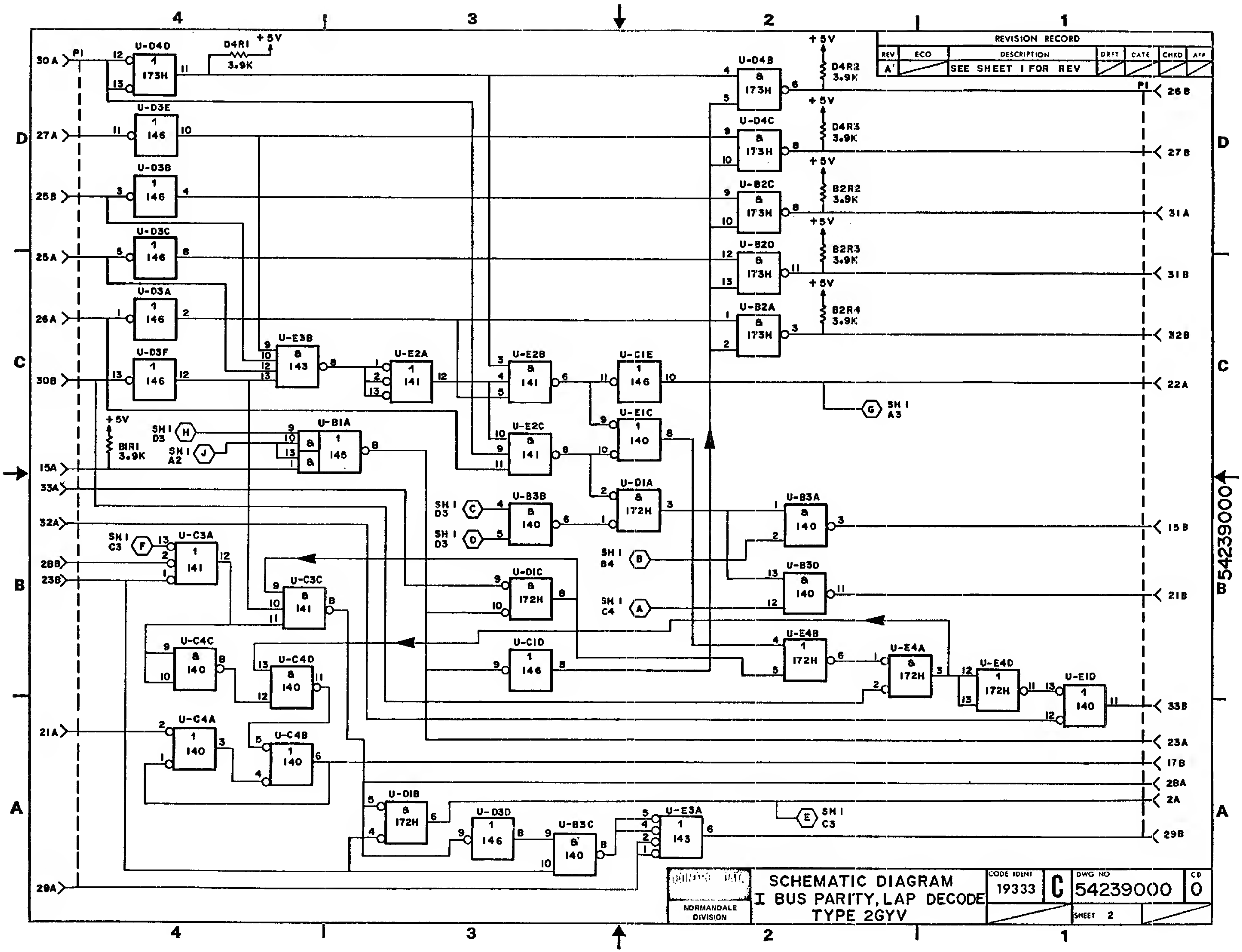


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHT 1 FOR REV
U-E1A
U-B3D
U-D1B
U-D1A
U-D1D
U-D3A
U-D3D
U-E1D
U-D1C
U-C3B
U-E3B
U-E2B
U-C1D
U-C3C
U-E3C
U-E2D
U-C1B
U-C3D
U-E3D
U-E2C
U-C3A
U-E3A
U-E2A
U-E1C
U-C1A
U-C1C
U-E1B
173H
140
+5V
1.5K
E1R1
01R1
01R2
01R3
E1R2
D1R4
E2R1
C1R1
E2R2
C1R2
E2R3
E2R4
E1R3
C1R3
C1R4
E1R4
P1
33B
13A
25A
29A
30A
30B
29B
32A
22A
23B
27B
32B
27A
28B
21A
31B
15B
31A
28A
18A
22B
33A
SH 1 C3
SH 2 C4
SH 2 B4
SH 1 B3
SH 2 A4
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
INPUT STEERING
TYPE 2GXV
CODE IDENT
19333
C
DWG NO
54238600
CD
8
SHEET 3
54238600


SHEET REVISION STATUS
REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A PE23000 RELEASED
SHEET NO. (TYP)
DWG. ZONE (TYP)
NOTES:
1. UNLESS OTHERWISE SPECIFIED;
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 TO +5V.
99C1-99C12
.01 UF
TP-A
TP-Z
REFERENCE DRAWINGS
COMP ASSY 54238900
CONTROL DATA CORPORATION
NORMANDALE DIVISION
FIRST USED ON BR3AB
DWN R. KONECNY 7-20-72
CHK 9-11-72
ENGR 9-11-72
COMPONENTS, EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHM 1/4 W
CAP -30%
TITLE
SCHEMATIC DIAGRAM
I BUS PARITY, LAP DECODE
TYPE 2GYV
CODE IDENT 19333
C
DRAWING NUMBER 54239000
CD 0
SHEET 1 OF 2
54239000

HPO1

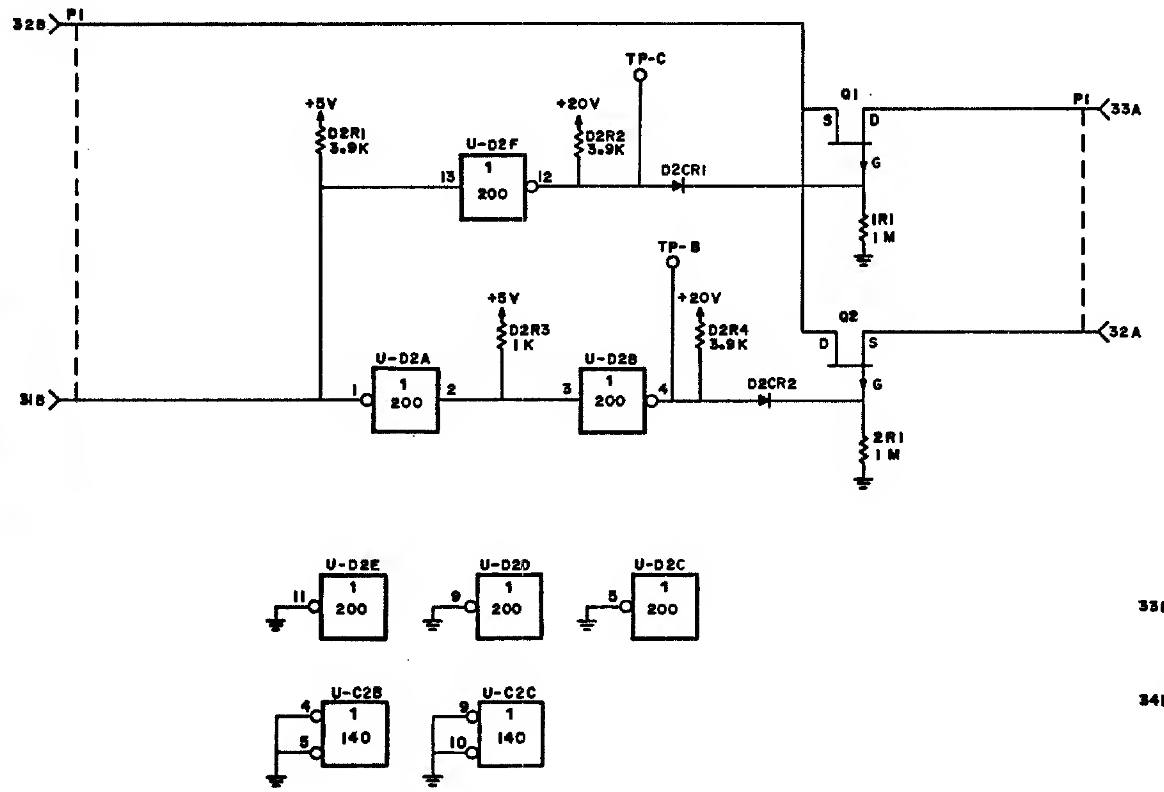
70629100 E


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A' SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
I BUS PARITY, LAP DECODE
TYPE 2GYV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54239000
CD 0
SHEET 2
54239000

SHEET REVISION STATUS							

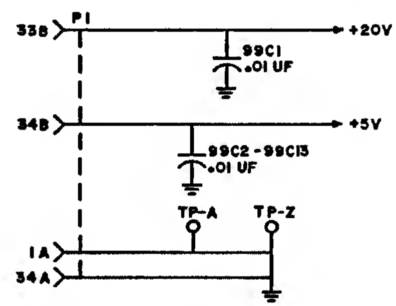
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED.
   ALL DIODES SILICON, 24553500.
   ALL TRANSISTORS FET, 2N5019, 50218200.
2. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS	
COMP ASSY	54239300

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	8R3A6
DWN	H. STREETER 7-13-72
CHK	7-2?-72
ENGR	9-2?-72
MFG	8-31-72
APPR	9/5/72

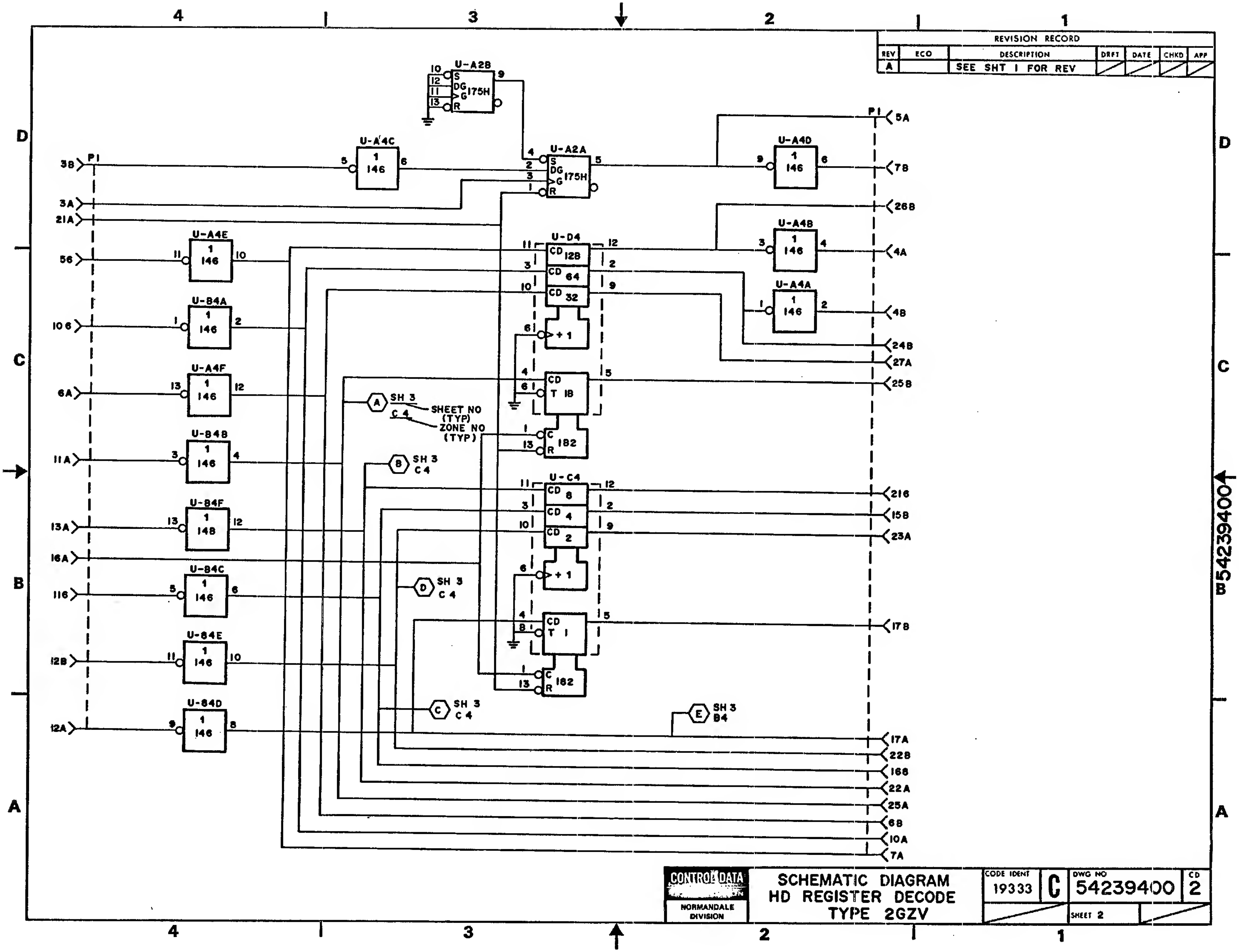
TITLE

SCHEMATIC DIAGRAM HD REGISTER DECODE TYPE 2GZV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54239400	2

SHEET 1 OF 3

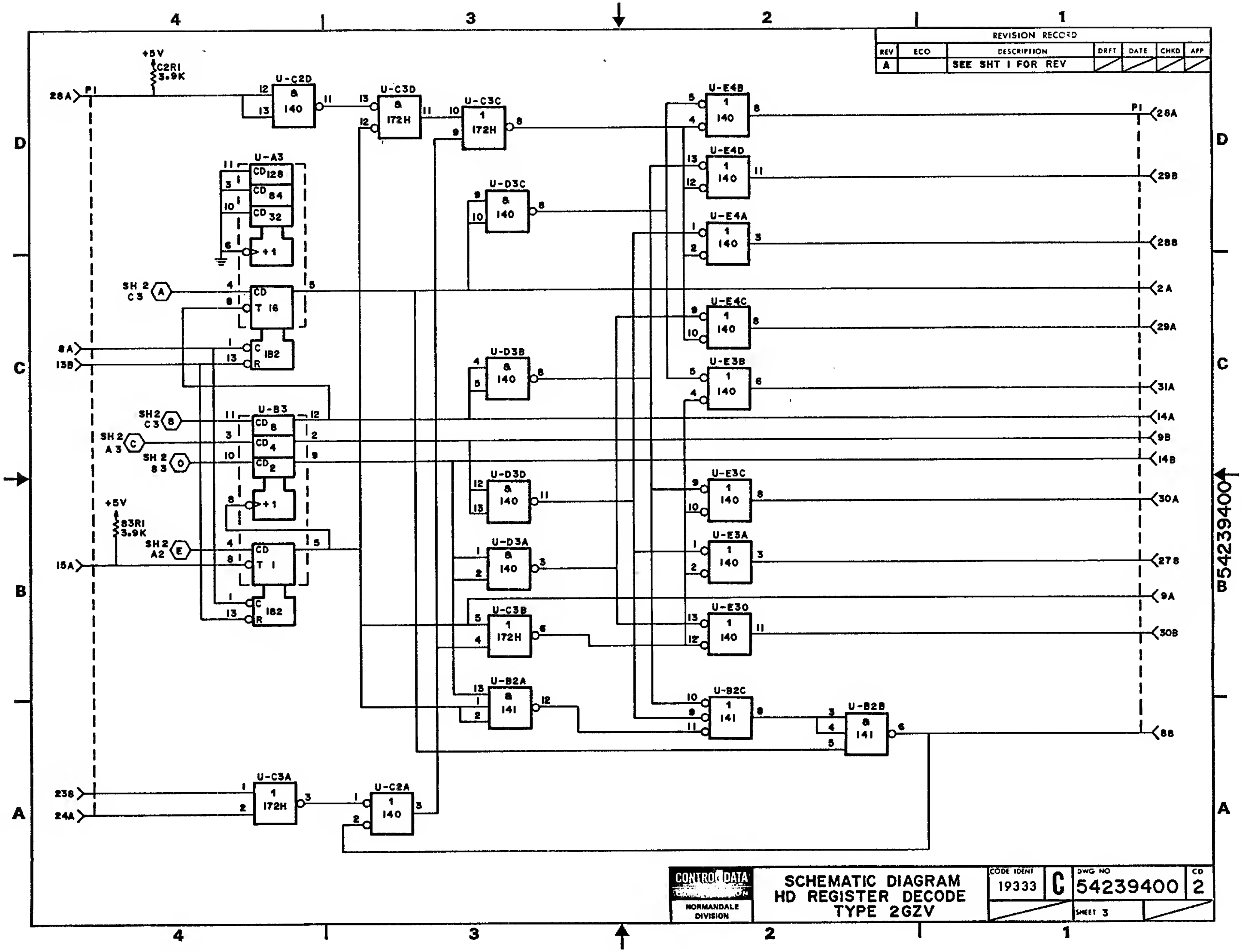
54239400

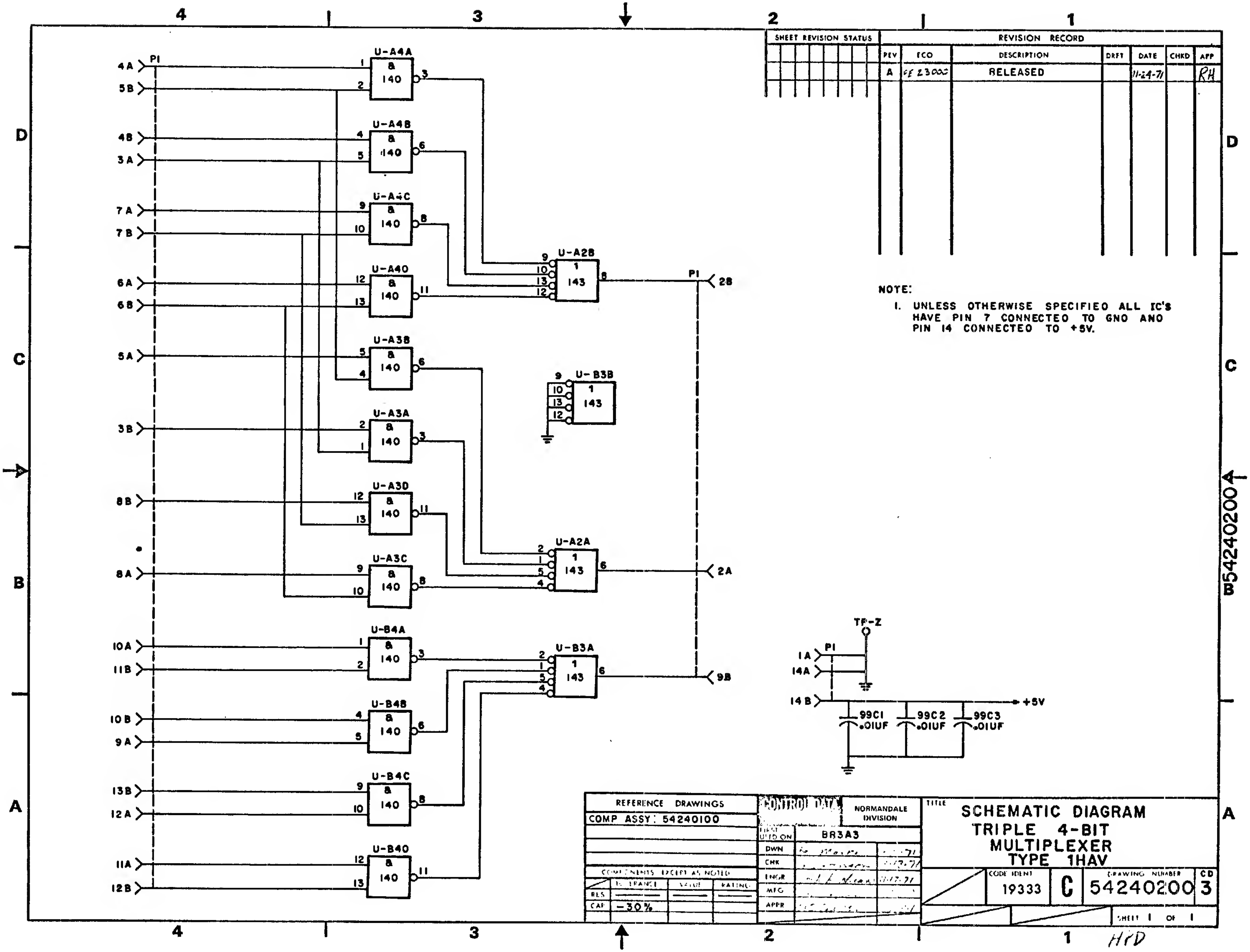


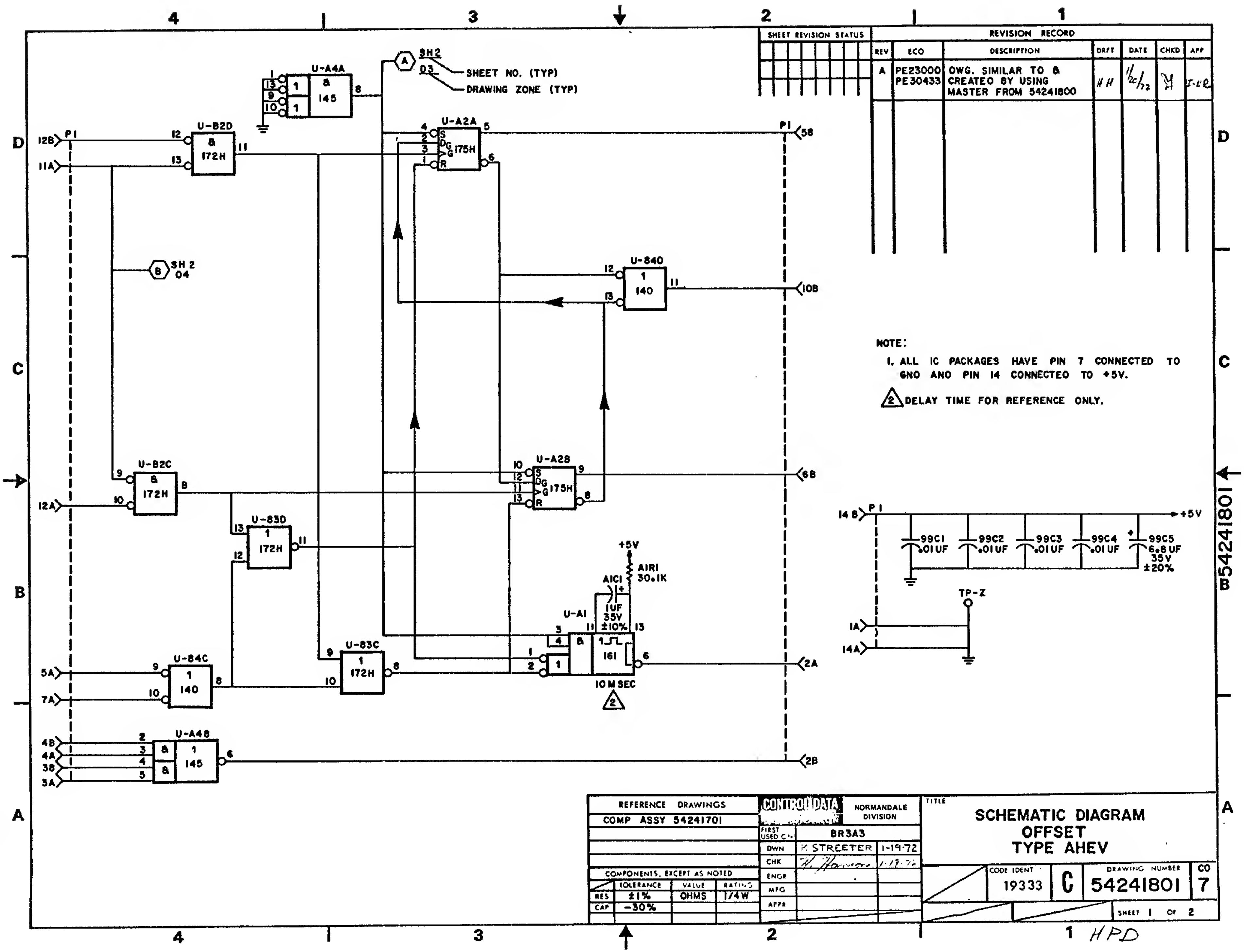
CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
HD REGISTER DECODE
TYPE 2GZV

CODE IDENT		DWG NO	CD
19333	C	54239400	2
		SHEET 2	

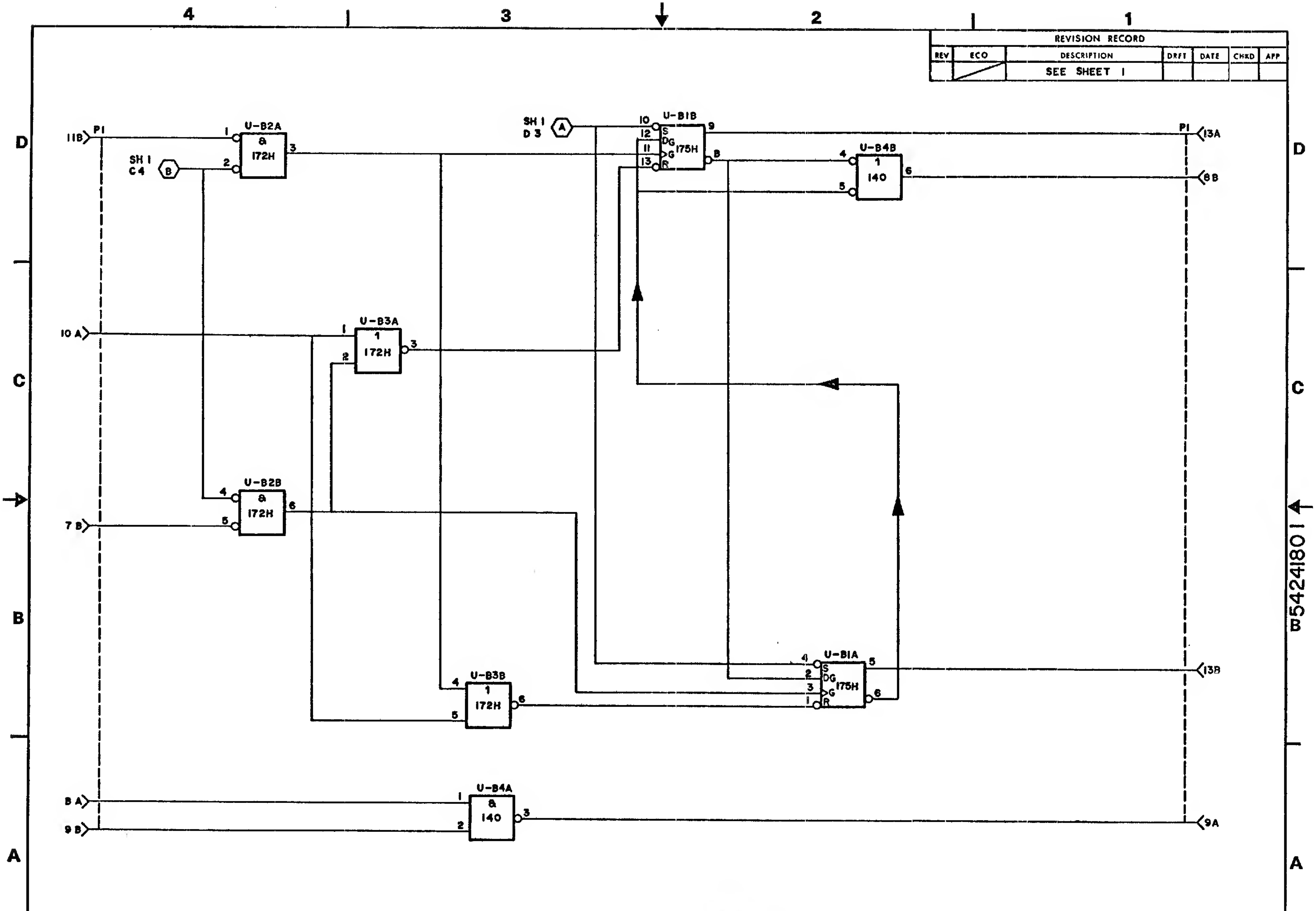

REVISION RECORD
REV
ECO
DESCRIPTION
DRFT
DATE
CHKD
APP
A
SEE SHT 1 FOR REV
SCHEMATIC DIAGRAM
HD REGISTER DECODE
TYPE 2GZV
CONTROL DATA
NORMANDALE DIVISION
CODE IDENT
19333
C
DWG NO
54239400
CD
2
SHEET 3
54239400


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | FE 23000 | RELEASED | | 11-24-71 | | RH
NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
U-A4A
U-A4B
U-A4C
U-A4D
U-A3B
U-A3A
U-A3D
U-A3C
U-B4A
U-B4B
U-B4C
U-B4D
U-A2B
U-A2A
U-B3B
U-B3A
8
140
1
143
P1
4A
5B
4B
3A
7A
7B
6A
6B
5A
3B
8B
8A
10A
11B
10B
9A
13B
12A
11A
12B
2B
2A
9B
TP-Z
1A
14A
14B
+5V
99C1 .01UF
99C2 .01UF
99C3 .01UF
REFERENCE DRAWINGS
COMP ASSY: 54240100
COMPONENTS EXCEPT AS NOTED
TOLERANCE
VALUE
RATING
RES
CAP -30%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3A3
DWN
CHK
ENGR
MFG
APPR
TITLE
SCHEMATIC DIAGRAM
TRIPLE 4-BIT
MULTIPLEXER
TYPE 1HAV
CODE IDENT 19333
C
DRAWING NUMBER 54240200
CD 3
SHEET 1 OF 1
HFD
54240200A


REVISION RECORD
SHEET REVISION STATUS
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23000 PE30433 | DWG. SIMILAR TO & CREATED BY USING MASTER FROM 54241800
SHEET NO. (TYP)
DRAWING ZONE (TYP)
SH2 D3
SH 2 D4
U-A4A
U-B2D
U-A2A
U-B4D
U-B2C
U-A2B
U-B3D
U-B4C
U-B3C
U-A1
U-A4B
172H
175H
145
140
161
P1
12B
11A
12A
5A
7A
4B
4A
3B
3A
5B
10B
6B
2A
2B
14B
1A
14A
+5V
A1R1 30.1K
A1C1 1UF 35V ±10%
10 MSEC
TP-Z
99C1 .01 UF
99C2 .01 UF
99C3 .01 UF
99C4 .01 UF
99C5 6.8 UF 35V ±20%
NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2 DELAY TIME FOR REFERENCE ONLY.
REFERENCE DRAWINGS
COMP ASSY 54241701
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±1% OHMS 1/4W
CAP -30%
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BR3A3
DWN K STREETER 1-19-72
CHK 1-19-72
ENGR
MFG
APPR
TITLE
SCHEMATIC DIAGRAM OFFSET TYPE AHEV
CODE IDENT 19333
C
DRAWING NUMBER 54241801
CO 7
SHEET 1 OF 2
54241801
HPD

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1				

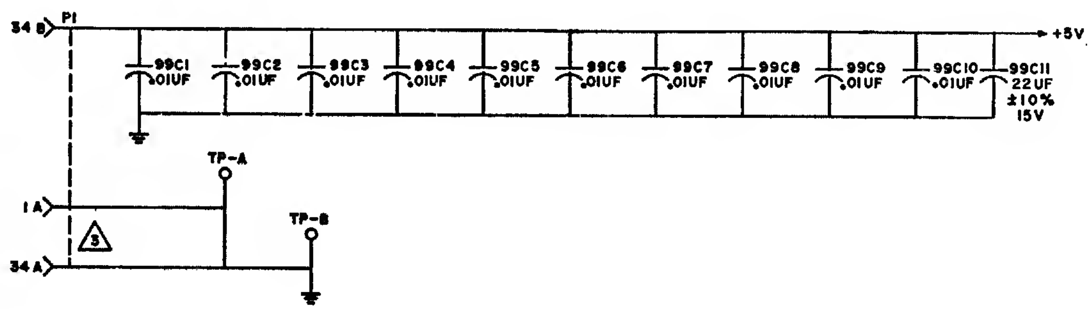


CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
OFFSET
TYPE AHEV

CODE IDENT		DWG NO	CD
19333	C	54241801	7
		SHEET 2	

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DEFT	DATE	CHKD	APP
	A	PE23040	RELEASED		3-8-72		



NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
   ALL DIODES, SHOTTKY BARRIER, 50241400.
2. DIODE, SILICON, 92115023.
3. CONNECTOR PINS 2A THRU 7A ARE CONNECTED TO GND.
4. JUMPER PLUG-DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
5. MATCHED WITH AHPV PER ENGINEERING TEST PROCEDURE.

54245001

REFERENCE DRAWINGS			
COMP ASSY 54244901			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

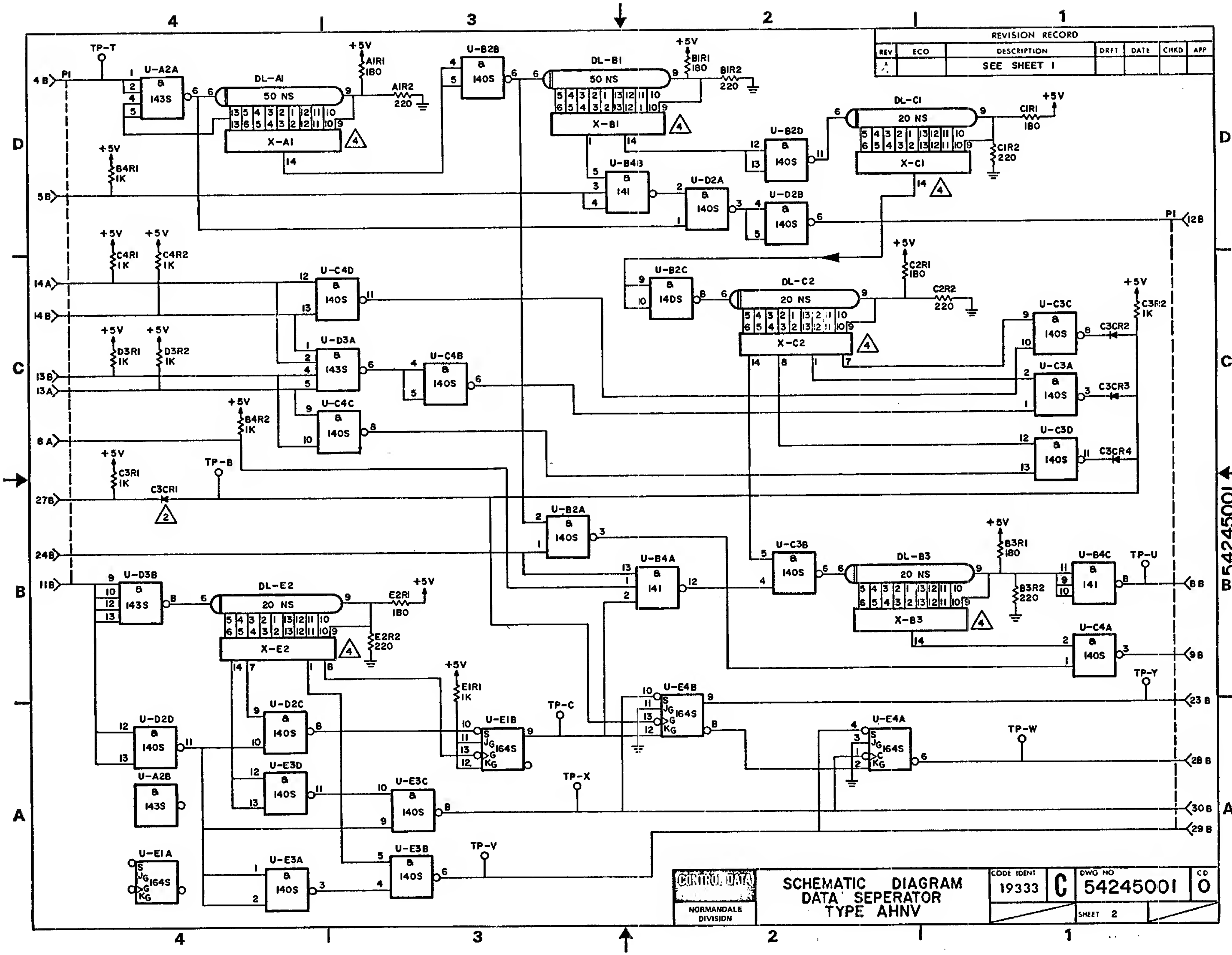
CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3A3	
DWN	K STREETER	1-13-72
CHK	L. Hanson	1-21-72
ENGE	H Hamati	1-21-72
MFG	Swanson	2-1-72
APPR	Lewis	2-3-72

TITLE: SCHEMATIC DIAGRAM DATA SEPERATOR TYPE AHNV

CODE IDENT 19333 — SIZE C — DRAWING NUMBER 54245001 — C.D. 0

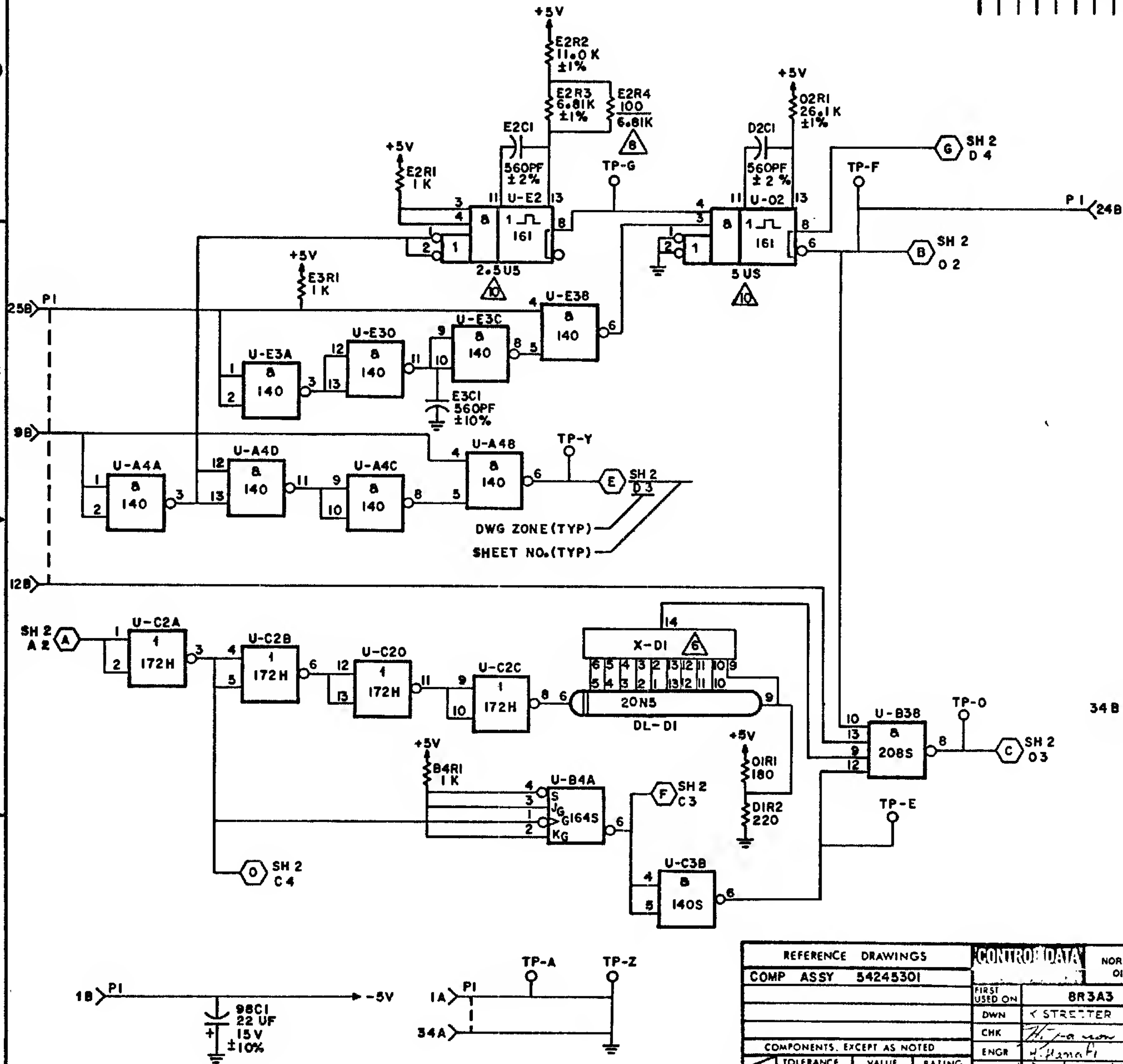
SHEET 1 OF 2


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SEE SHEET 1
DL-A1 50 NS
X-A1
DL-B1 50 NS
X-B1
DL-C1 20 NS
X-C1
DL-C2 20 NS
X-C2
DL-B3 20 NS
X-B3
DL-E2 20 NS
X-E2
TP-T
TP-B
TP-C
TP-X
TP-V
TP-W
TP-U
TP-Y
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
DATA SEPERATOR
TYPE AHNV
CODE IDENT 19333
C
DWG NO 54245001
CD 0
SHEET 2
54245001

SHEET REVISION STATUS								

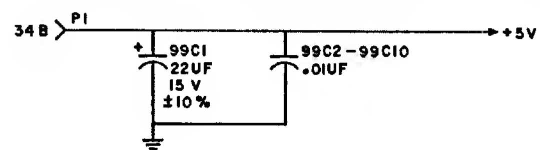
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	-E23000	RELEASED		3-8-72		



NOTE:

1. UNLESS OTHERWISE SPECIFIED
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, 92115021
   ALL ZENER DIODE VOLTAGE TOLERANCE ARE ±5%.
2. TRANSISTOR SPNP, 2N4258, 50211510.
3. DIODE SILICON, 92115023.
4. DIODE SILICON, SCHOTTKY BARRIER, 50241400.
5. DIODE GERMANIUM, 11801200.
6. DELAY TAPS ARE EVERY 2.0NS ±.25NS. PROPER TAP IS SELECTED PER ENGINEERING TEST PROCEDURE.
7. ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
8. COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
9. MATCHED WITH AHNV PER ENGINEERING TEST PROCEDURE
10. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMP ASSY 54245301

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	8R3A3	
DWN	K STRETTER	1-12-72
CHK	[signature]	1-25-72
ENGR	[signature]	1-31-72
MFG	[signature]	2-1-72
APPR	[signature]	2-3-72

TITLE
SCHEMATIC DIAGRAM PHASE LOCK OSC TYPE AHPV

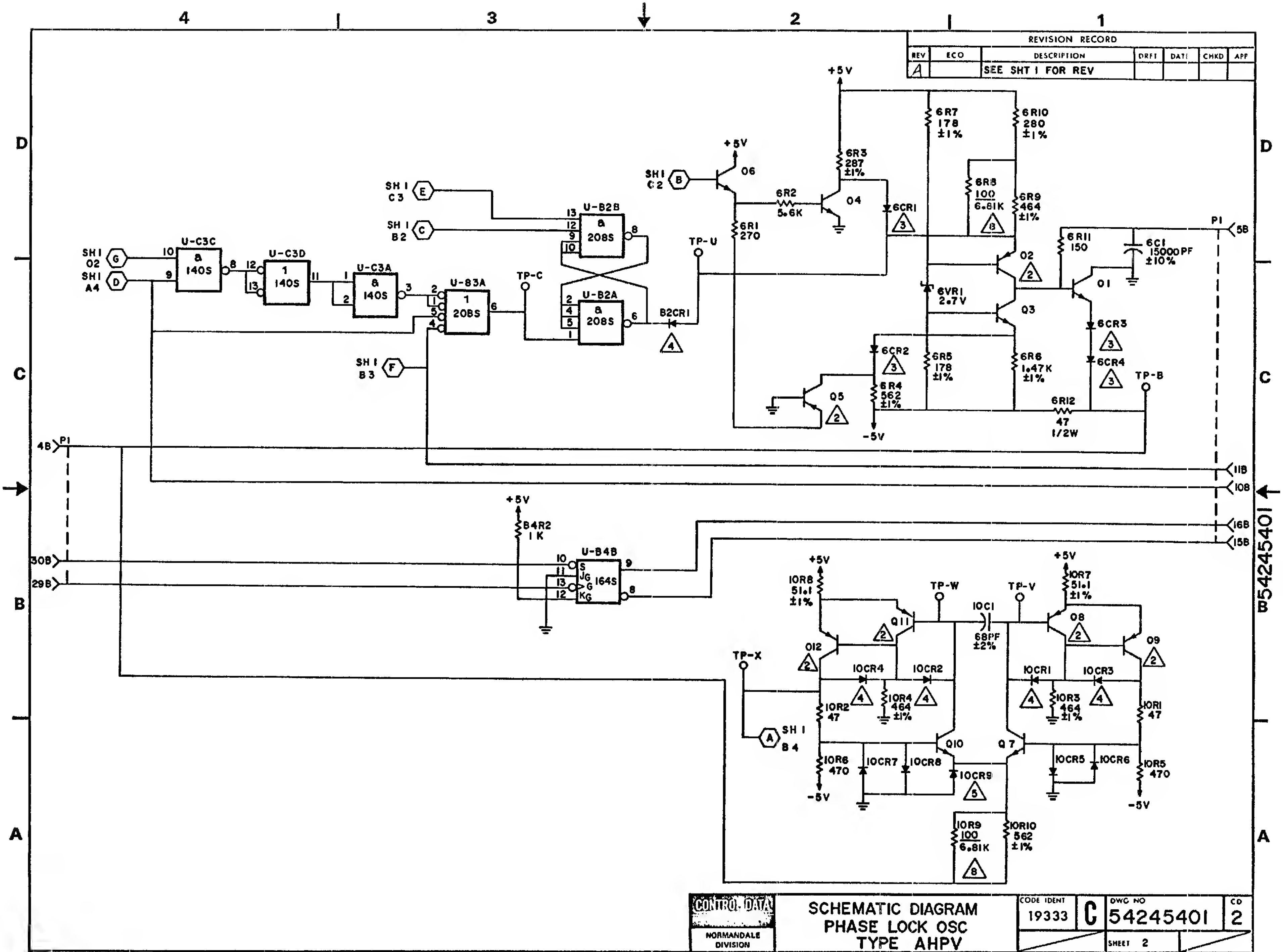
CODE IDENT		DRAWING NUMBER	CD
19333	C	54245401	2

SHEET 1 OF 2

54245401

HPD

70629100 E



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

CONTROL DATA
NORMANDALE DIVISION

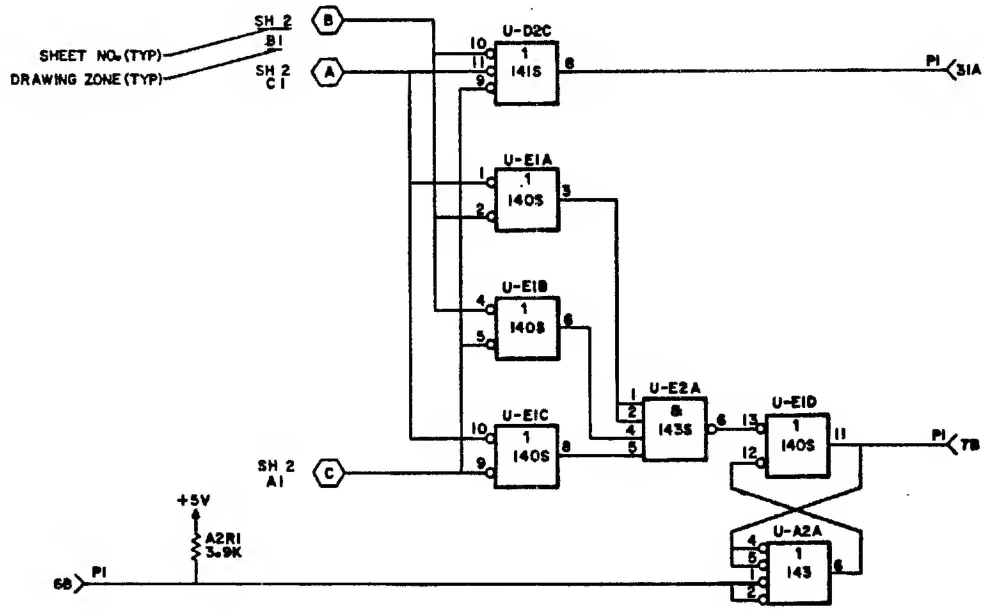
SCHEMATIC DIAGRAM
PHASE LOCK OSC
TYPE AHPV

CODE IDENT 19333 C DWG NO 54245401 CD 2

SHEET 2

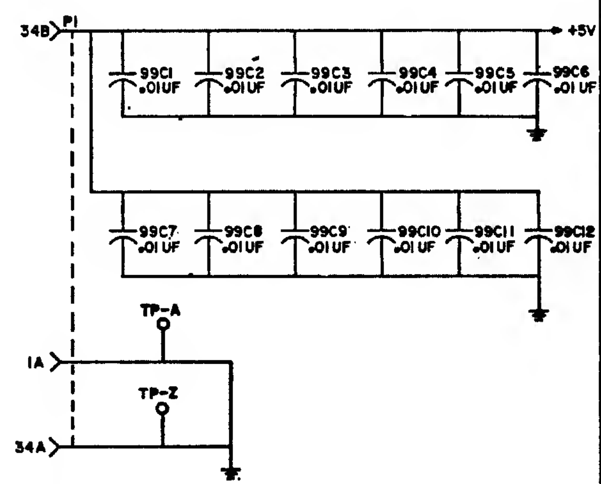
54245401

HPD



NOTES:

1. ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY LINES C1 AND D1 HAVE PINS 7 AND 8 CONNECTED TO GND.
3. DELAY TAPS ARE EVERY 2.00 ±0.25 NS. DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE
	A	FE 23000	RELEASED		12-

REFERENCE DRAWINGS			
COMP ASS'Y 54245700			
COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

NORMANDALE DIVISION

LOCATION	BR3A3	
DWN	R. BOCHE	11-9-71
CHK	H. Hanson	2-6-71
ENGR	W. Peterson	2/6/71
MFG	S. Johnson	12/9/71
APPR	B. Lewis	12-9-71

TITLE: SCHEMATIC DIAGRAM WRITE COMPENSATION TYPE 1HQV

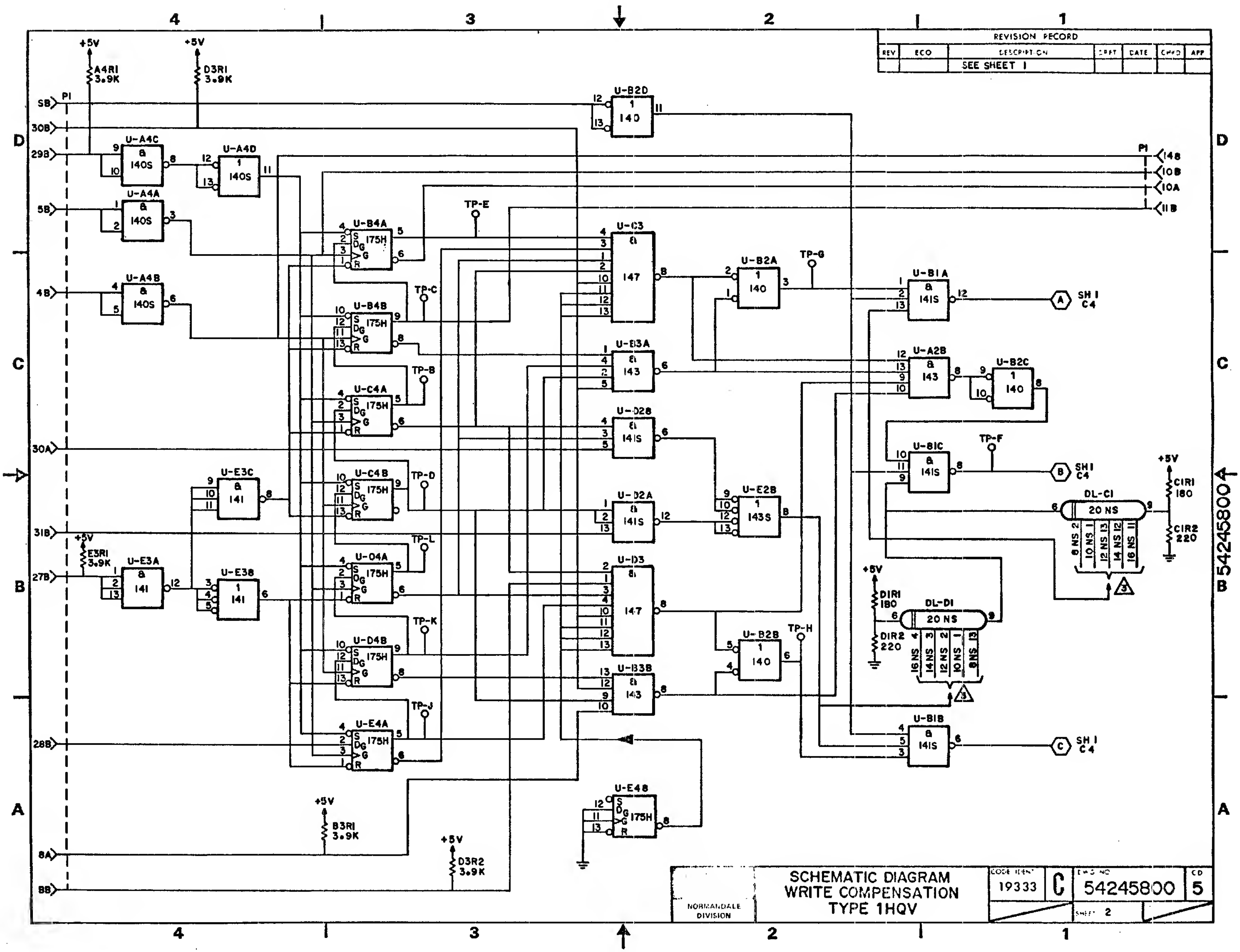
ORIG

CODE IDENT 19333 | C | DRAWING NUMBER 54245800 | CD 5

SHEET 1 OF 2

HPD

54245800



REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1				

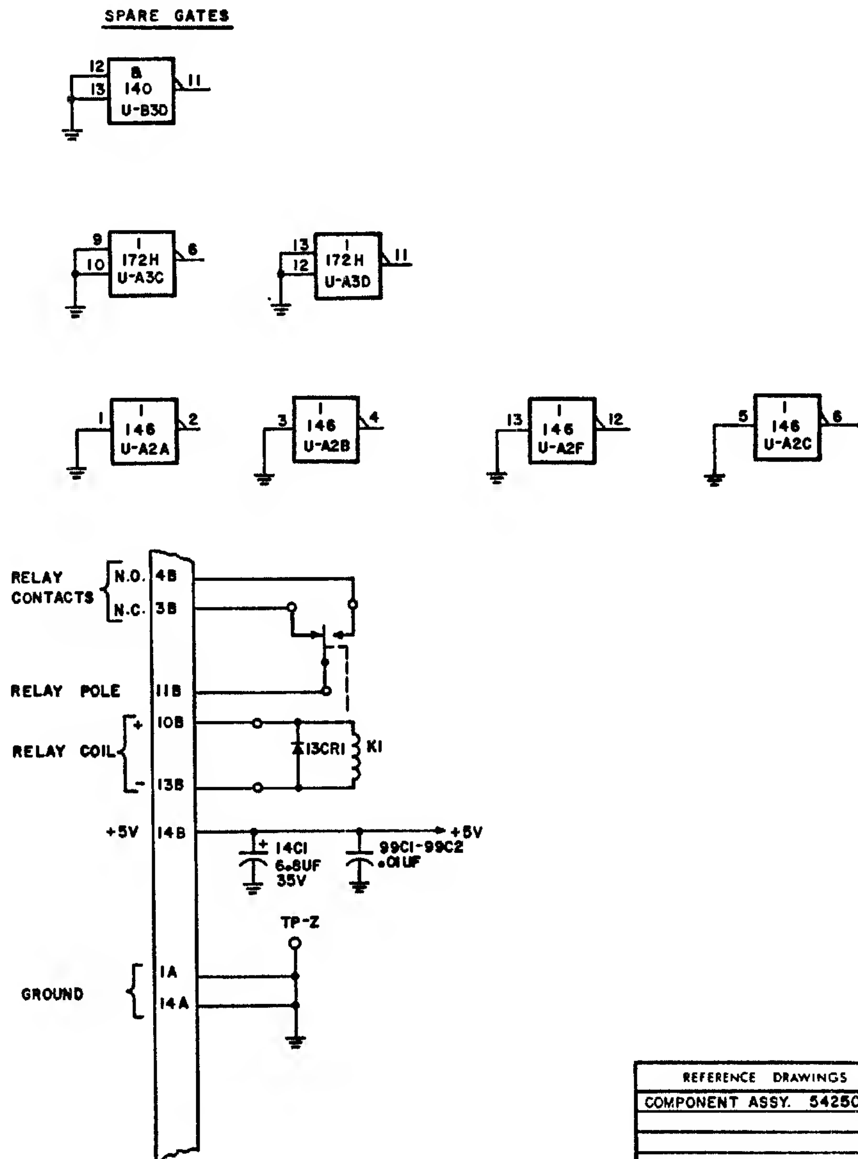
SCHEMATIC DIAGRAM
WRITE COMPENSATION
TYPE 1HQV

NORMANDALE DIVISION

CODE IDENT 19333 C DWG NO 54245800 CD 5 SHEET 2

70629100 E

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	[illegible]	RELEASED	[illegible]	8-9-73	[illegible]	[illegible]



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   DIODE, SILICON 92115023
   RELAY, FIND NO. 7, P.N. 94366100.

REFERENCE DRAWINGS			
COMPONENT ASSY. 54250900			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES			
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

USED ON	BR3B8	
DWN	V. WILSON	7/27/73
CHK	[illegible]	7-27-73
ENGR	[illegible]	7-27-73
MFG	[illegible]	8-8-73
APPR	[illegible]	[illegible]

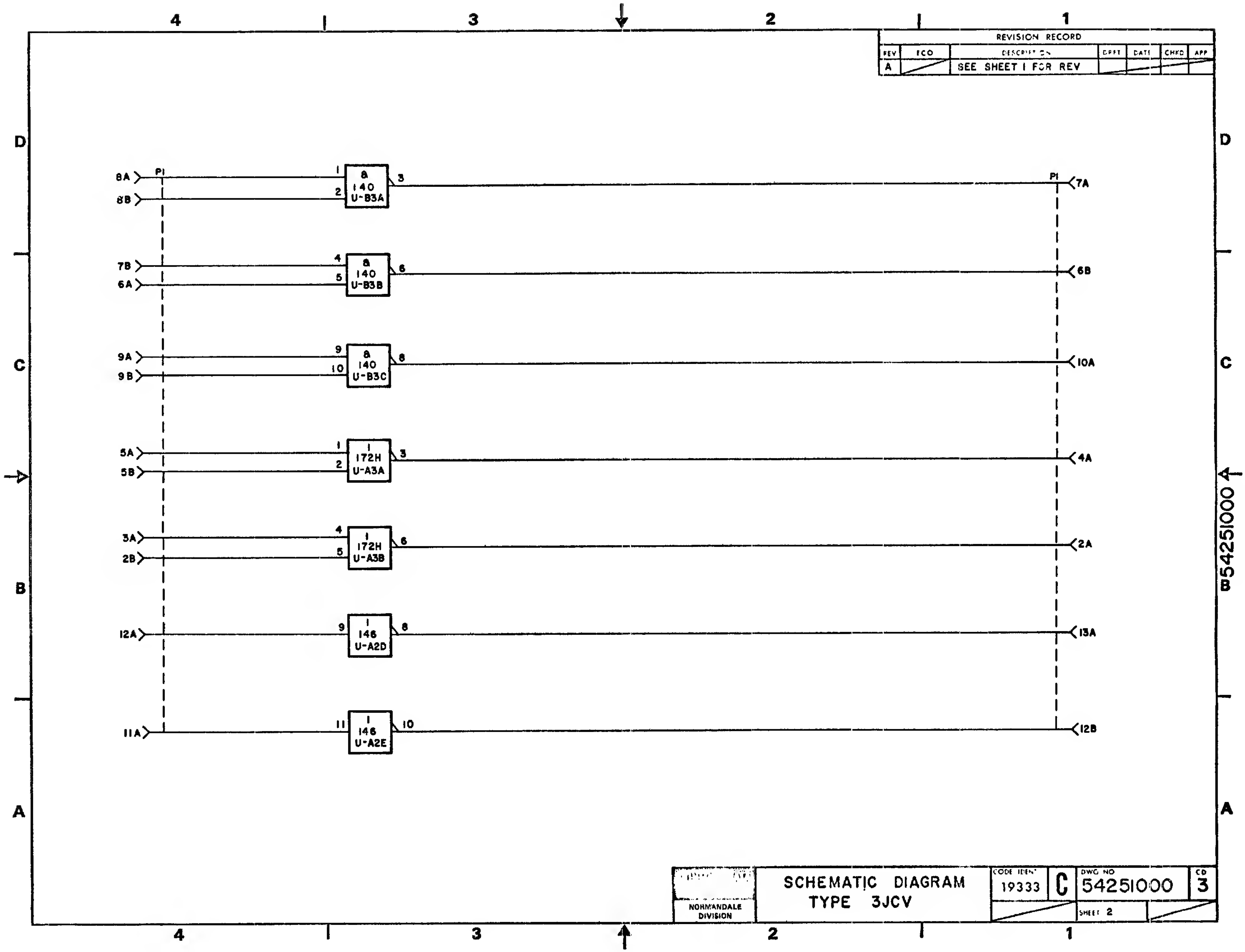
TITLE: SCHEMATIC DIAGRAM POWER INTERRUPT TYPE 3JCV

CODE IDENT 19333 | C | DRAWING NUMBER 54251000 | CD 3

SCALE 2/1 | SHEET 1 OF 2

HPD-C

54251000


REVISION RECORD
REV | ECO | DESCRIPTION | DFFT | DATE | CHKD | APP
A | SEE SHEET I FOR REV
8A
8B
P1
8 140 U-B3A
7A
7B
6A
8 140 U-B3B
6B
9A
9B
8 140 U-B3C
10A
5A
5B
1 172H U-A3A
4A
3A
2B
1 172H U-A3B
2A
12A
1 146 U-A2D
13A
11A
1 146 U-A2E
12B
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 3JCV
CODE IDENT 19333
C
DWG NO 54251000
CD 3
SHEET 2
B54251000

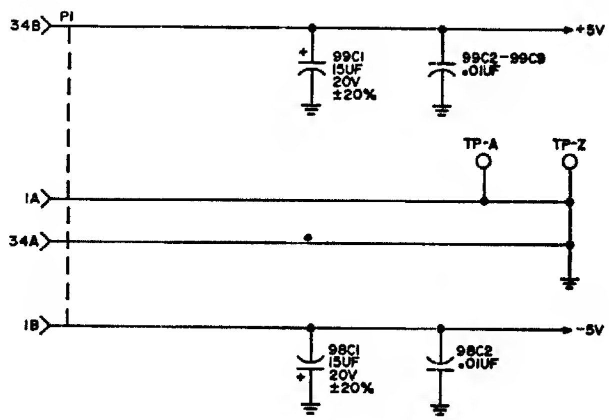
SHEET REVISION STATUS								

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE[illegible]	RELEASED		9-16-73		[illegible]

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMP ASSY 54254100

COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3B8	
DWN	MON BAKER	8-10-73
CHK	[illegible]	8-16-73
ENGR	[illegible]	9-20-73
MFG	[illegible]	[illegible]
APPR		

TITLE

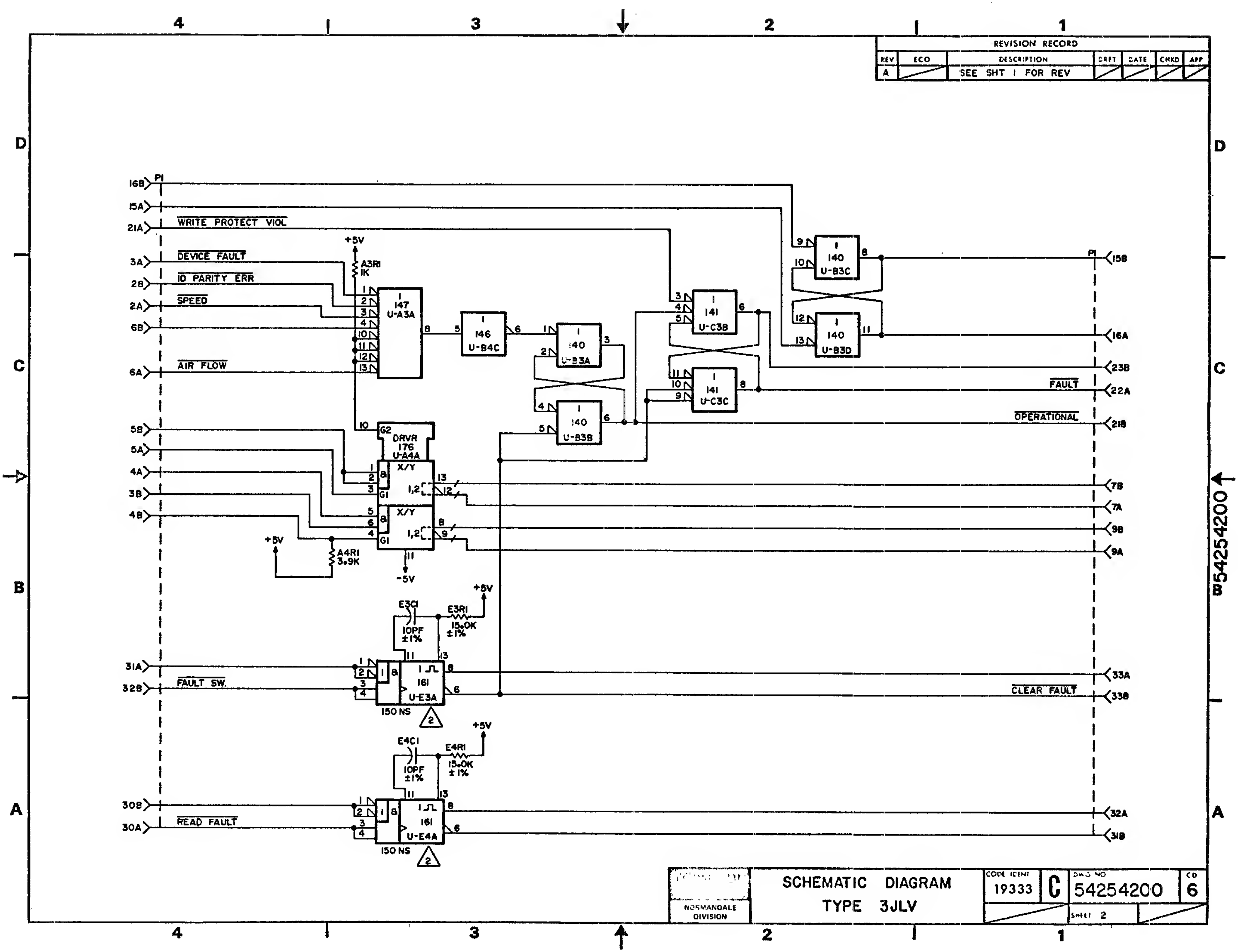
SCHEMATIC DIAGRAM
DEVICE CLOCK & FAULT GATING
TYPE 3JLV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54254200	6

SHEET 1 OF 3

54254200

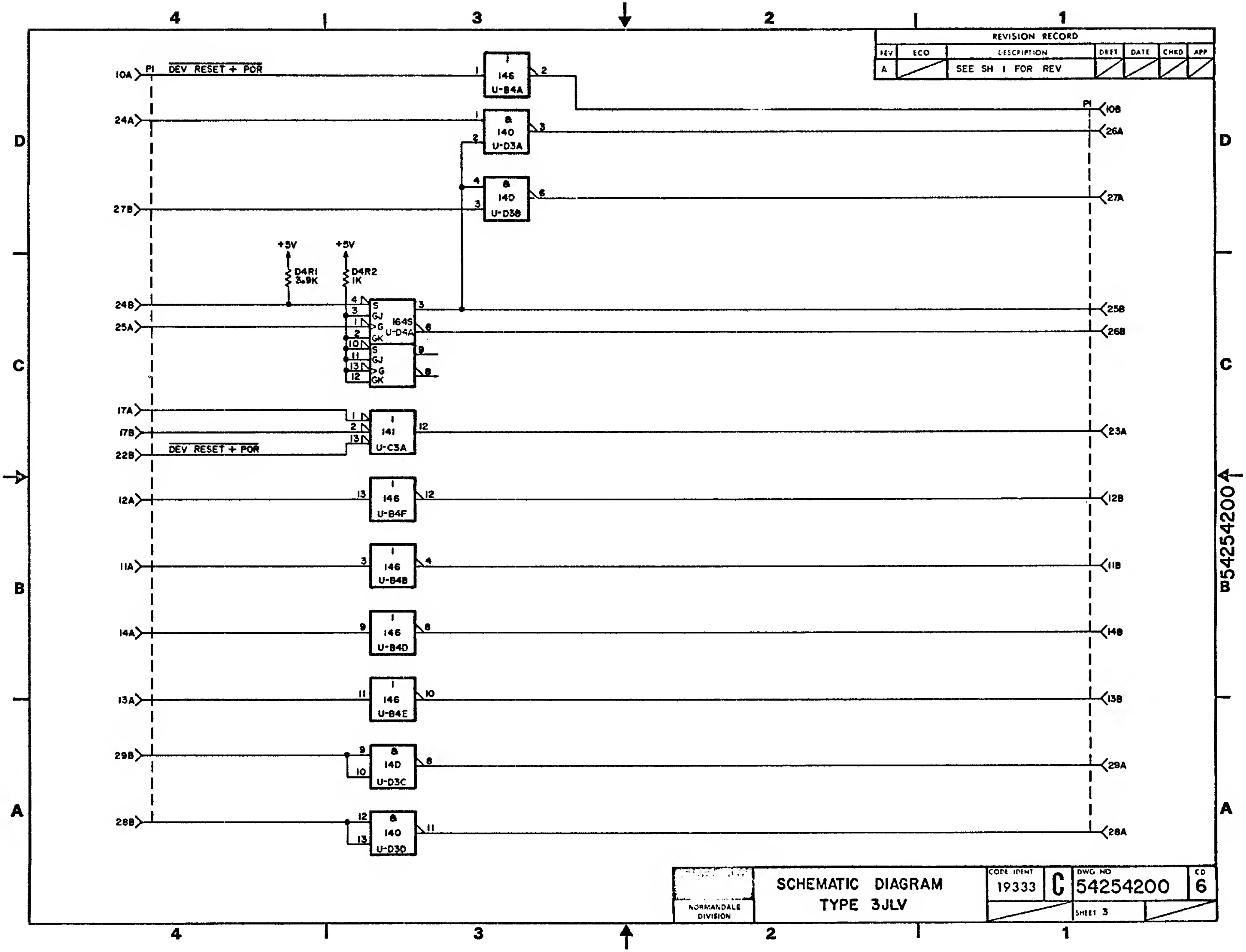
HP D-E



70629100 E

54254200

NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JLV	CODE IDENT 19333	C	DWG NO 54254200	CD 6
			SHEET 2



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				

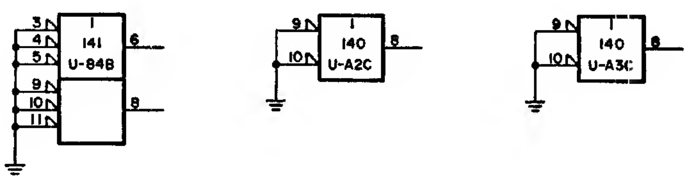
NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JLV	CODE IDENT 19333	C	DWG NO 54254200	CD 6
				SHEET 3	

54254200 B

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED		[illegible]		[illegible]

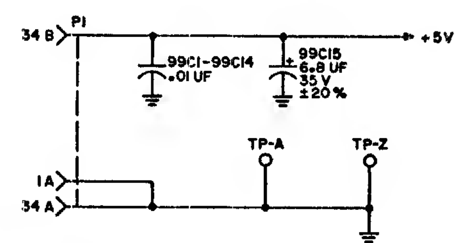
SPARE GATES



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL DIODES, GERMANIUM, 11801200.

2. DELAY TIME FOR REF ONLY.



REFERENCE DRAWINGS
COMP ASSY 54254500

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON 8R388

DWN	[illegible]	8-9-73
CHK	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
MFG	[illegible]	[illegible]
APPR	[illegible]	[illegible]

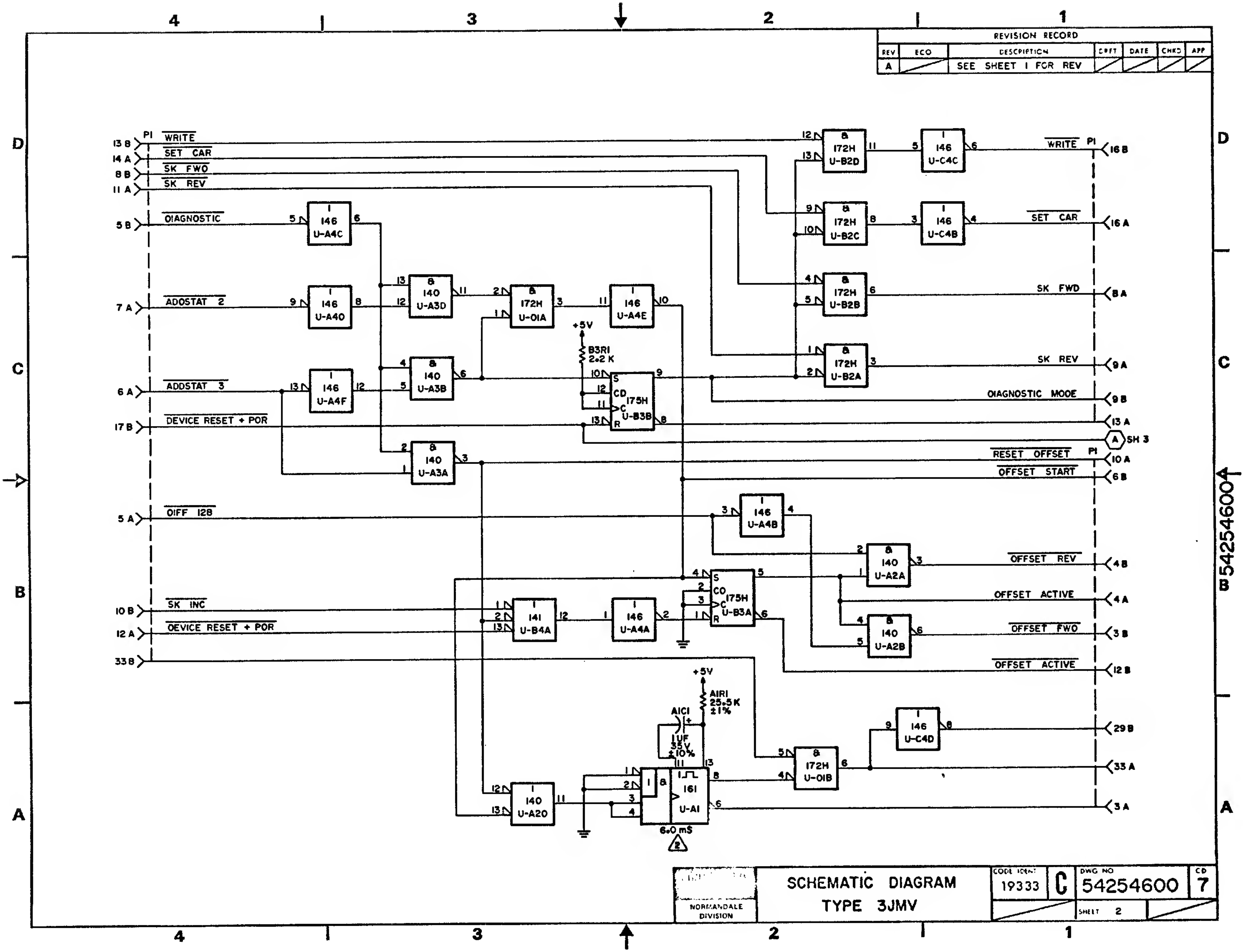
TITLE
SCHEMATIC DIAGRAM DIAGNOSTIC AND OFFSET TYPE 3JMV

CODE IDENT		DRAWING NUMBER	CO
19333	C	54254600	7

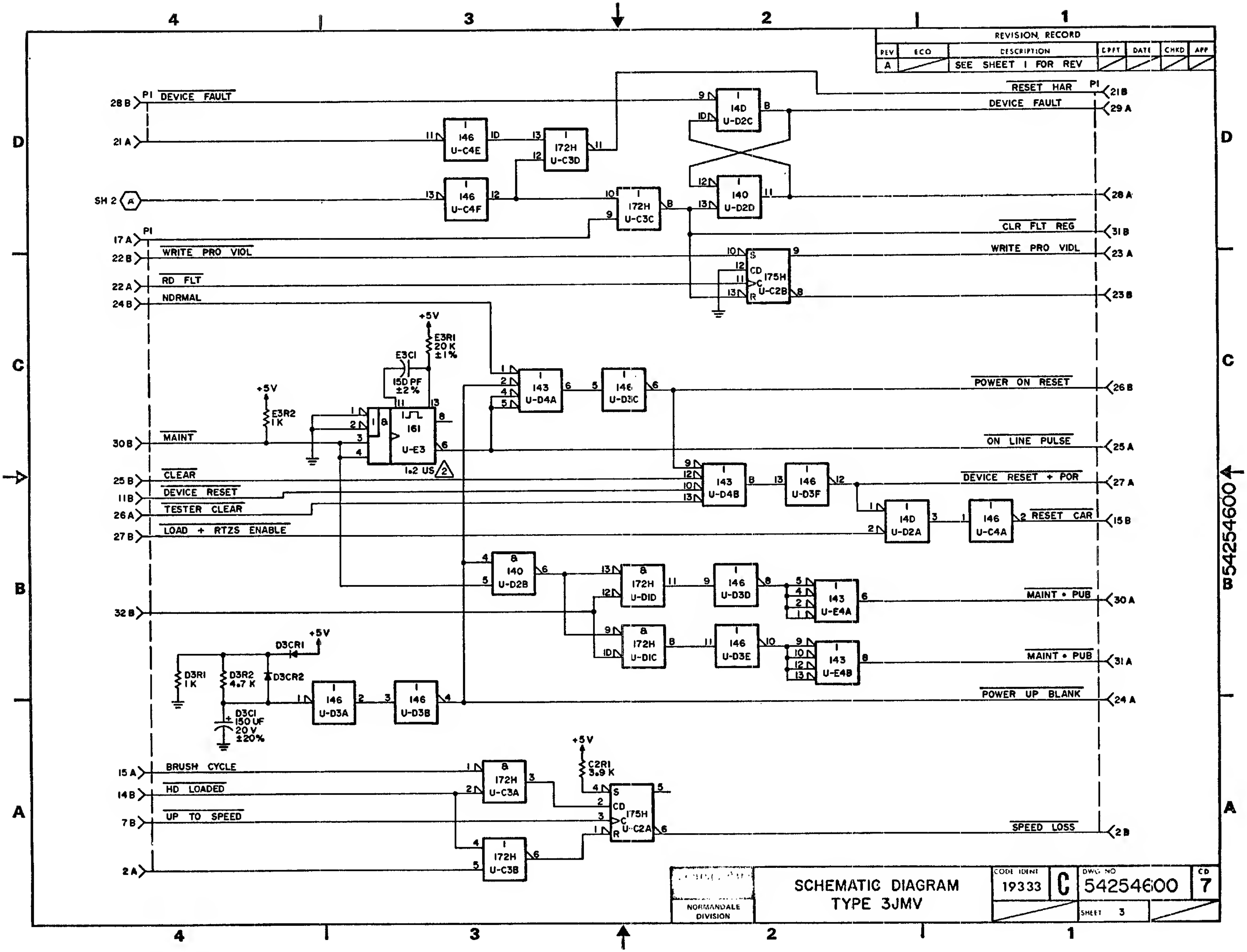
SHEET 1 OF 3

54254600A

HPD-E


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
WRITE
SET CAR
SK FWD
SK REV
DIAGNOSTIC
ADDSTAT 2
ADDSTAT 3
DEVICE RESET + POR
DIFF 128
SK INC
DEVICE RESET + POR
DIAGNOSTIC MODE
RESET OFFSET
OFFSET START
OFFSET REV
OFFSET ACTIVE
OFFSET FWD
OFFSET ACTIVE
SH 3
+5V
B3R1 2.2 K
A1R1 25.5K ±1%
A1C1 1UF 35V ±10%
6.0 mS
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 3JMV
CODE IDENT 19333
C
DWG NO 54254600
7
SHEET 2
54254600

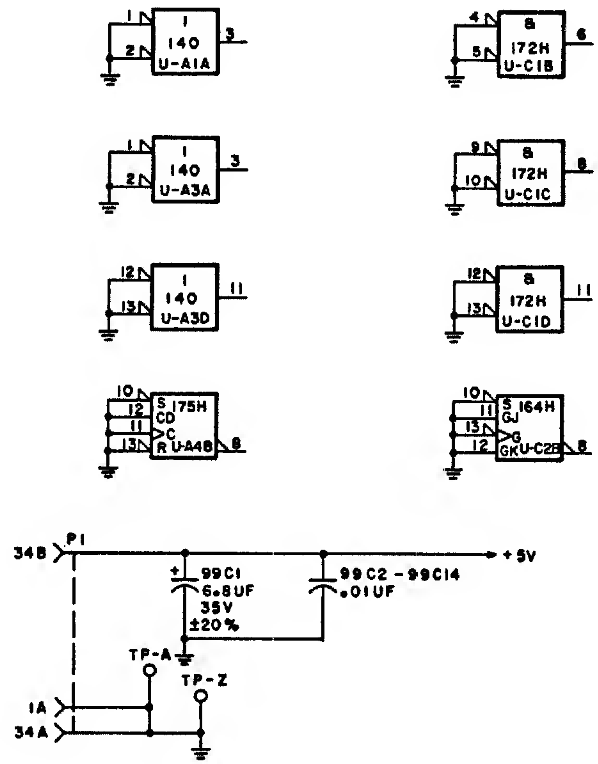
70629100 E



4-171

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED		4-6-73		CR

REVISION RECORD — SHEET REVISION STATUS



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V
   ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 TO +5V.
2. DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASSY : 54254900

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

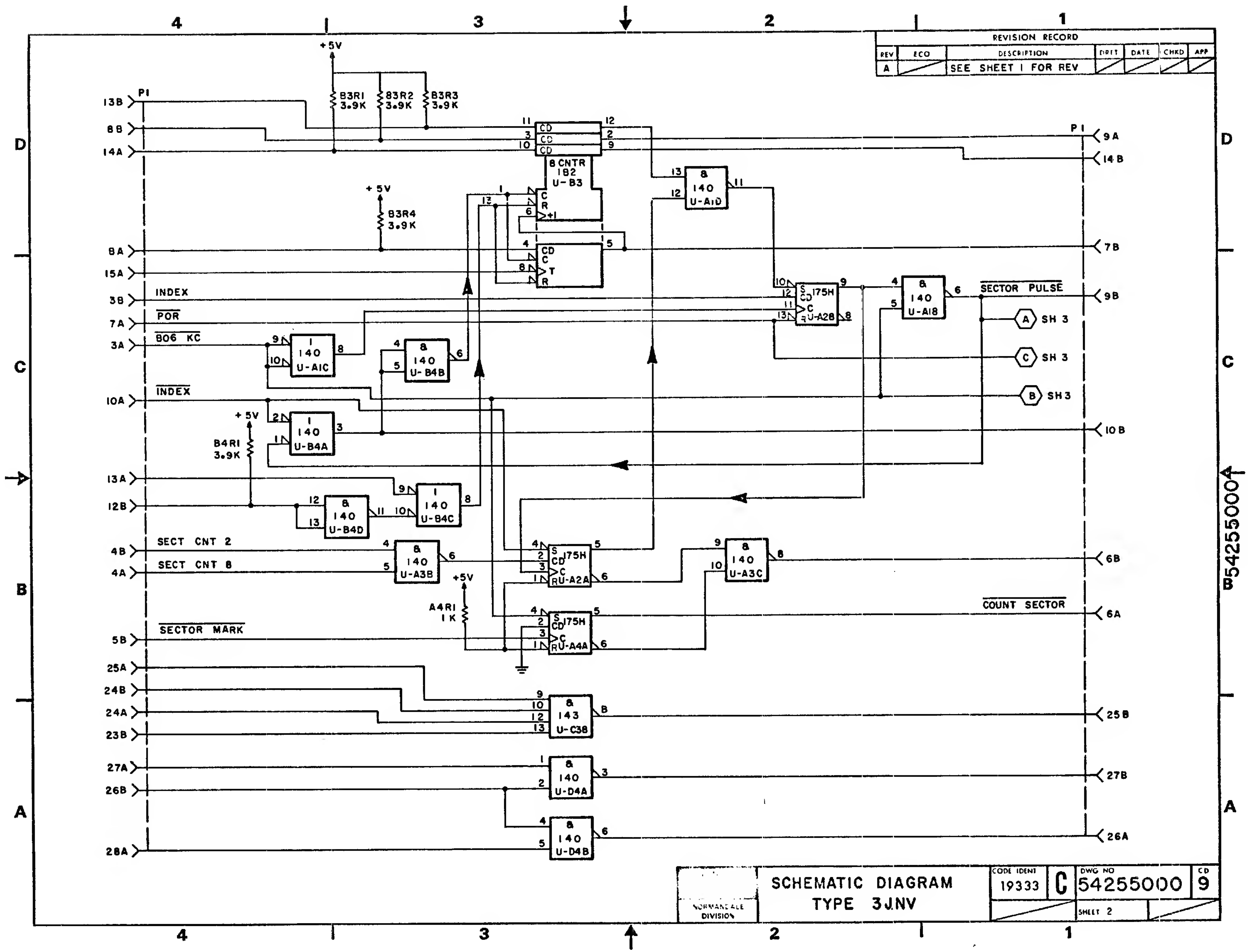
FIRST USED ON BR388

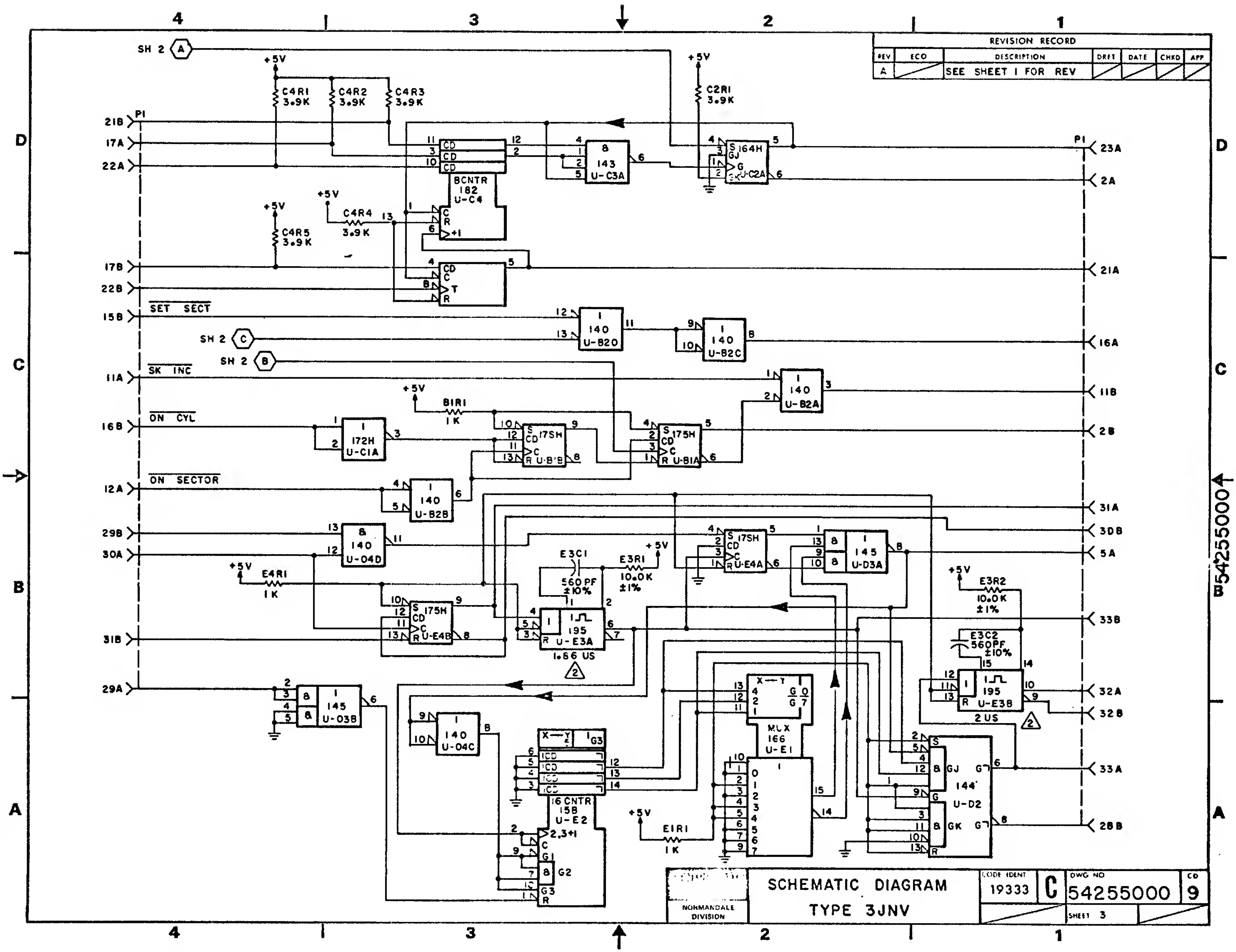
TITLE: SCHEMATIC DIAGRAM INDEX / SECTOR TYPE 3JNV

CODE IDENT 19333 — C — DRAWING NUMBER 54255000 — CD 9

SHEET 1 OF 3

70629100 E

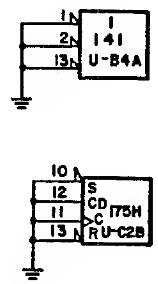

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
+5V
B3R1 3.9K
B3R2 3.9K
B3R3 3.9K
B3R4 3.9K
B4R1 3.9K
A4R1 1K
8 CNTR 182 U-B3
INDEX
POR
806 KC
INDEX
SECT CNT 2
SECT CNT 8
SECTOR MARK
SECTOR PULSE
COUNT SECTOR
SH 3
175H U-A2B
175H U-A2A
175H U-A4A
140 U-A1C
140 U-B4B
140 U-B4A
140 U-B4D
140 U-B4C
140 U-A3B
140 U-A1D
140 U-A18
140 U-A3C
143 U-C38
140 U-D4A
140 U-D4B
SCHEMATIC DIAGRAM
TYPE 3JNV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54255000
CD 9
SHEET 2
B54255000A


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
SH 2 A
SH 2 C
SH 2 B
+5V
C4R1 3.9K
C4R2 3.9K
C4R3 3.9K
C4R4 3.9K
C4R5 3.9K
C2R1 3.9K
B1R1 1K
E4R1 1K
E1R1 1K
E3C1 560 PF ±10%
E3R1 10.0K ±1%
E3C2 560PF ±10%
E3R2 10.0K ±1%
P1
21B
17A
22A
17B
22B
SET SECT
15B
SK INC
11A
ON CYL
16B
ON SECTOR
12A
29B
30A
31B
29A
23A
2A
21A
16A
11B
2B
31A
30B
5A
33B
32A
32B
33A
28B
BCNTR 182 U-C4
143 U-C3A
164H U-C2A
140 U-B2D
140 U-B2C
140 U-B2A
172H U-C1A
175H U-B'B
175H U-B1A
140 U-B2B
140 U-04D
175H U-E4B
195 U-E3A
1.66 US
175H U-E4A
145 U-D3A
195 U-E3B
2 US
145 U-03B
140 U-04C
16 CNTR 158 U-E2
MUX 166 U-E1
144 U-D2
SCHEMATIC DIAGRAM
TYPE 3JNV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54255000
CD 9
SHEET 3
54255000

70629100 E

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23060	RELEASED		9-16-73		ck

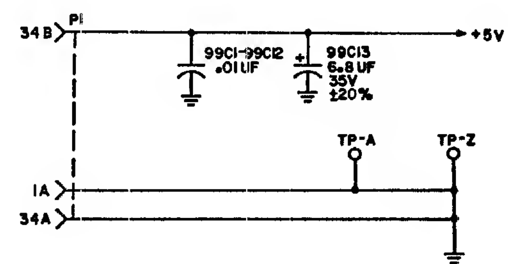
SPARES



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
   ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.

2. DELAY TIME FOR REFERENCE ONLY.



54255400

REFERENCE DRAWINGS			
COMPONENT ASSY. 54255300			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: BR388

DWN / CHK / ENGR / MFG / APPR

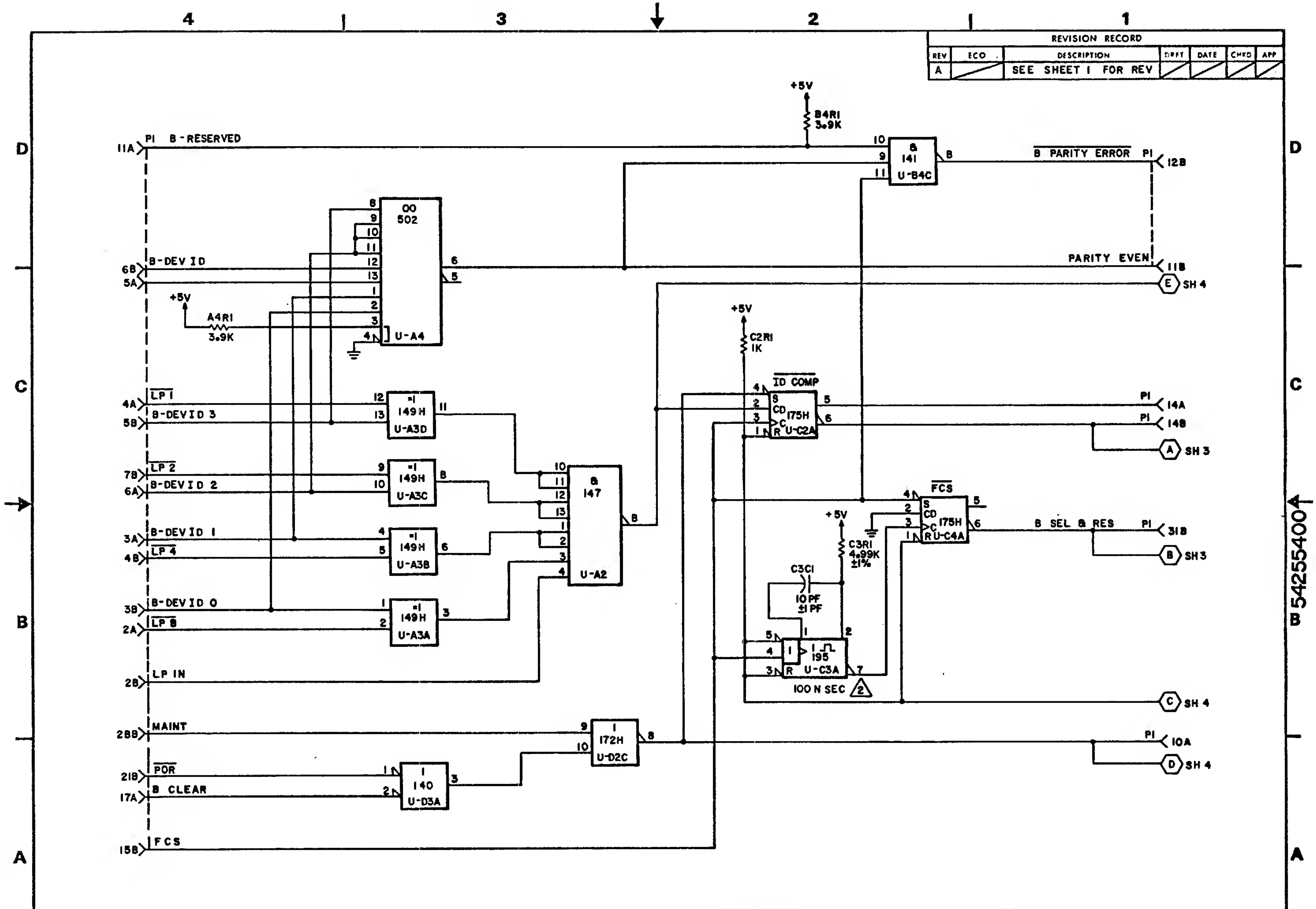
TITLE: SCHEMATIC DIAGRAM DIALOG TYPE 3JPV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54255400	1

SHEET 1 OF 4

4-175

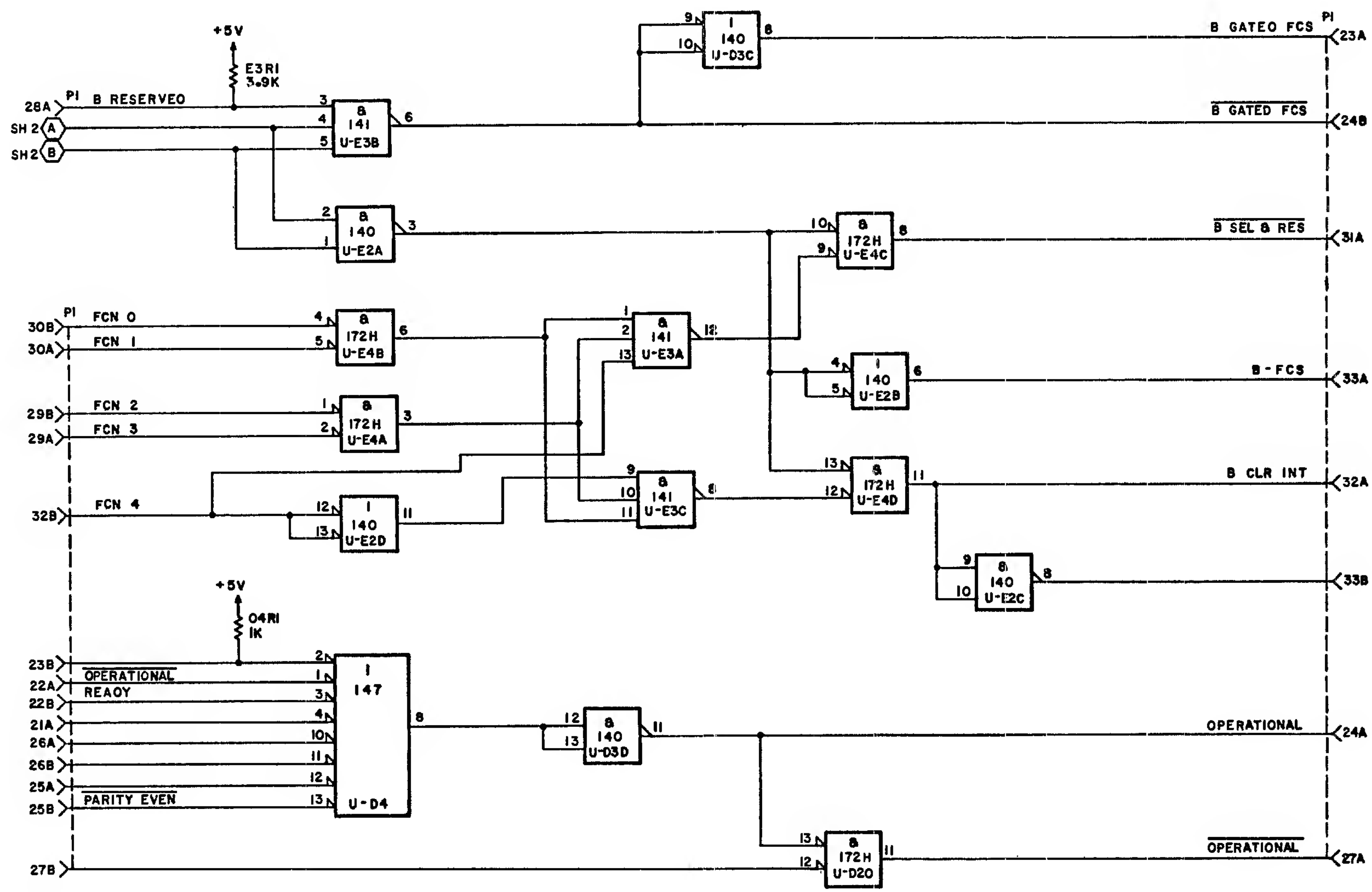
4-176



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JPV	CODE IDENT 19333	C	DWG NO 54255400 · CD 1 · SHEET 2

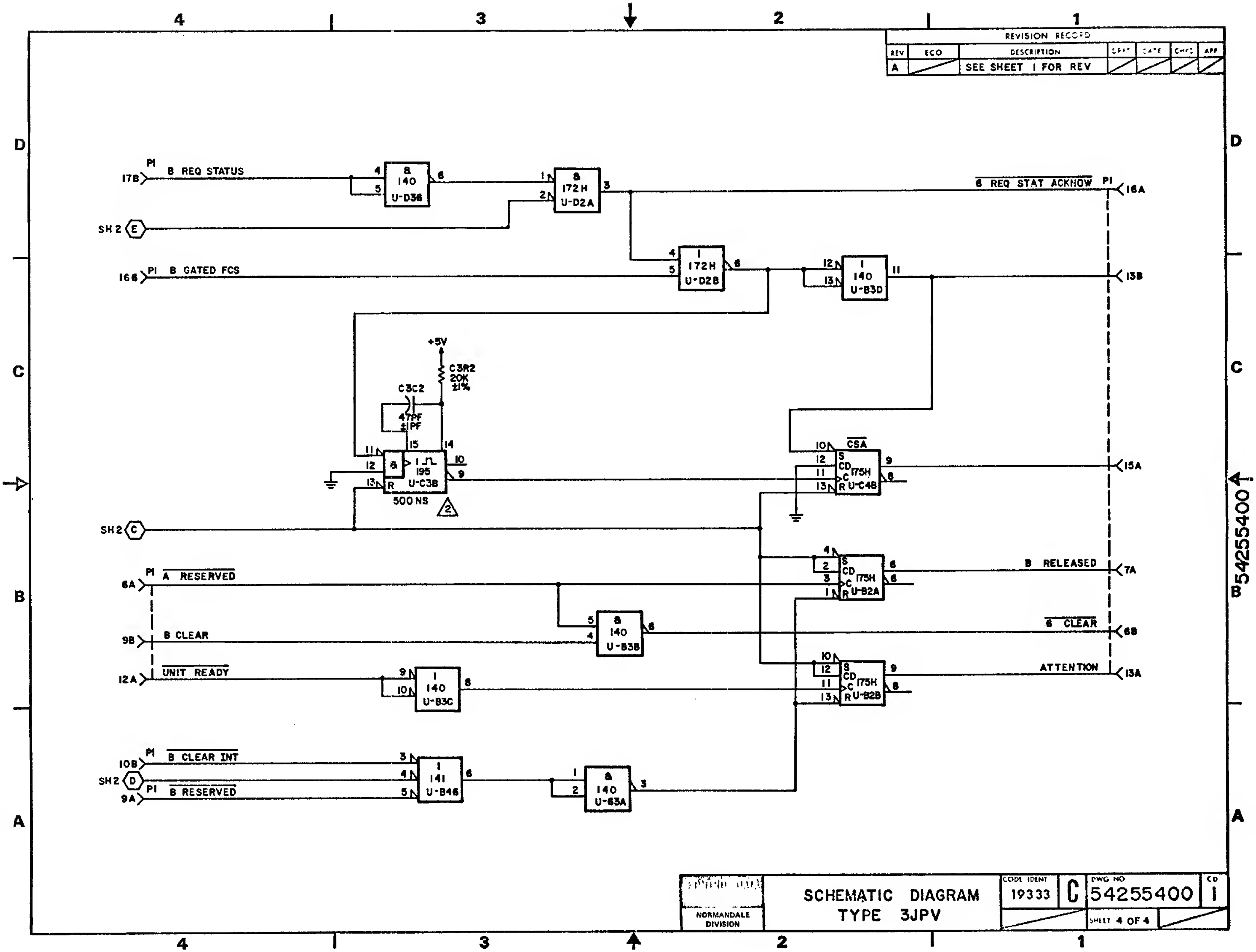
70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	CHKD (?)	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JPV	CODE IDENT 19333	C	DWG NO 54255400	CD 1
				SHEET 3	

54255400



SCHEMATIC DIAGRAM
TYPE 3JPV

NORMANDALE DIVISION

CODE IDENT 19333 C DWG NO 54255400 CD 1

SHEET 4 OF 4

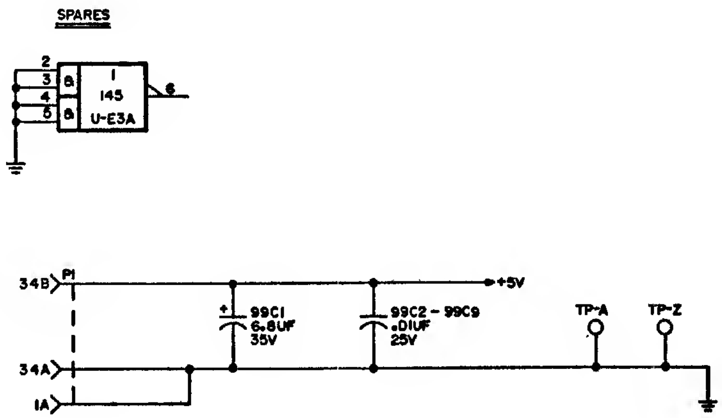
54255400

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED		[illegible]		[illegible]

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS	
COMP ASSY: 54255700	
COMPONENTS, EXCEPT AS NOTED	

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	BR3B8	
DWN	MON BAKER	8-8-73
CHK	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
MFG	[illegible]	[illegible]
APPR	[illegible]	[illegible]

TITLE

SCHEMATIC DIAGRAM MISCELLANEOUS TYPE 3JQV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54255800	2

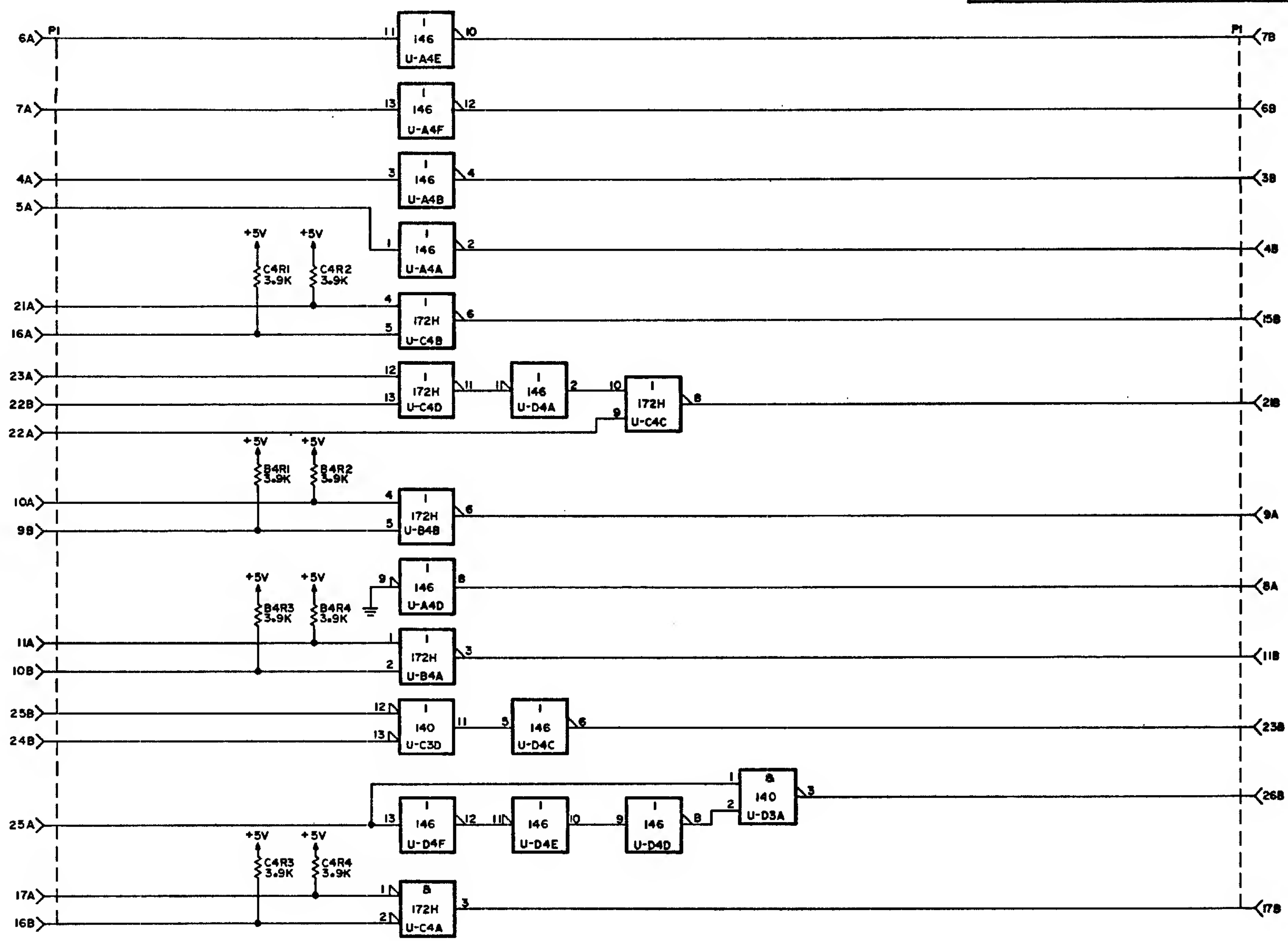
SHEET 1 OF 3

54255800

HPD-E

4-180

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				



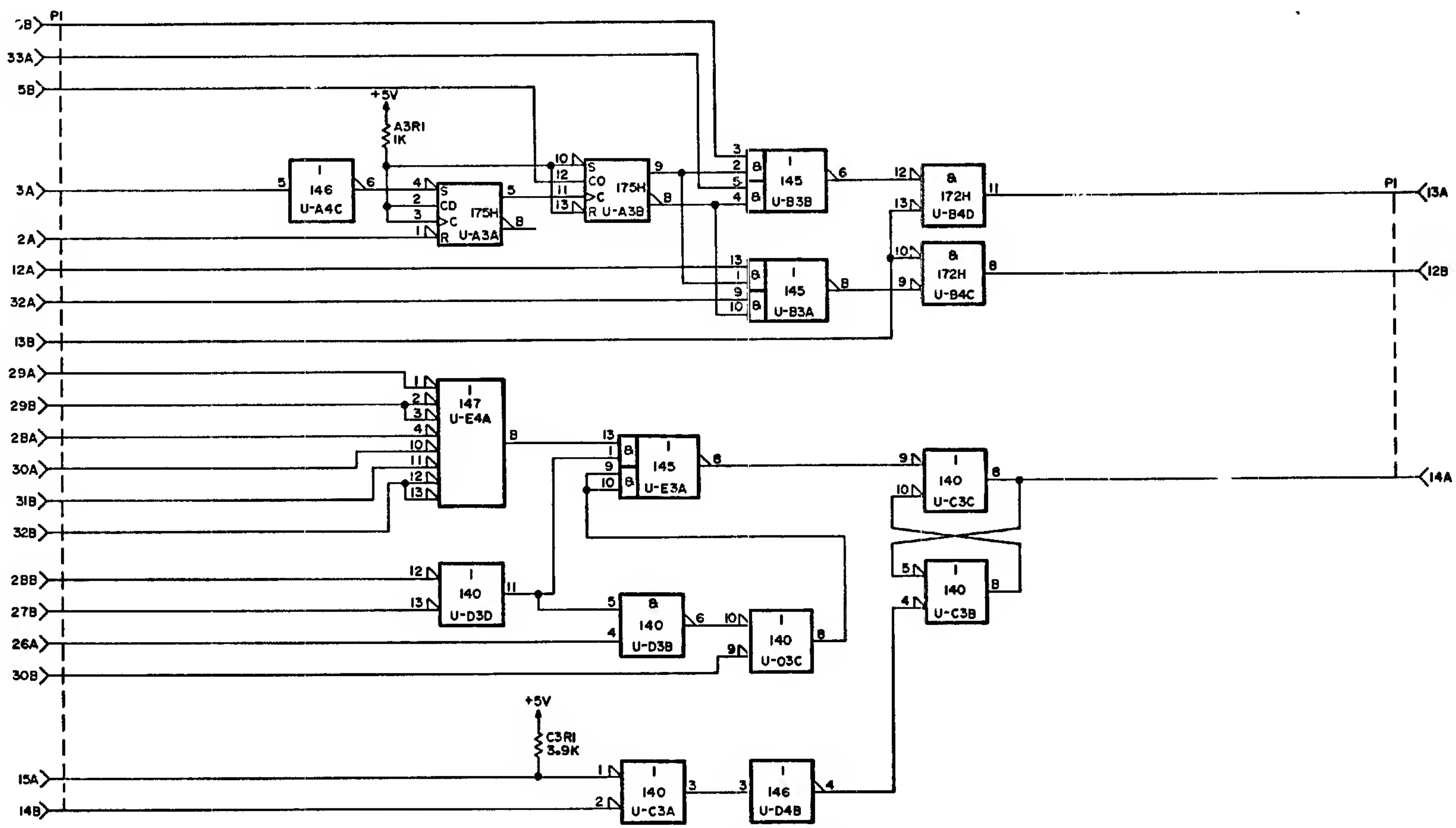
NORMANDALE DIVISION	SCHEMATIC DIAGRAM MISCELLANEOUS TYPE 3JQV	CODE IDENT 19333	C	DWG NO 54255800	CD 2
				SHEET 2	

54255800

70629100 E

70629100 E

REVISION RECORD						
LTR	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				



SCHEMATIC DIAGRAM
MISCELLANEOUS TYPE 3JQV

NORMANDALE DIVISION

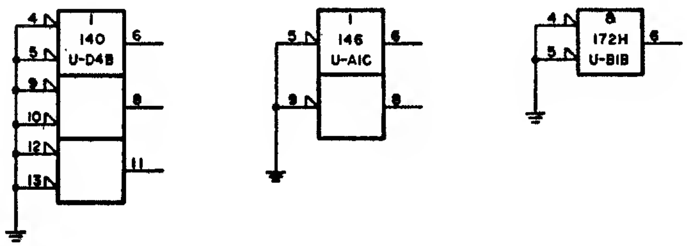
CODE IDENT 19333 | C | DWG NO 54255800 | CD 2

SHEET 3

54255800

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED		[illegible]		[illegible]

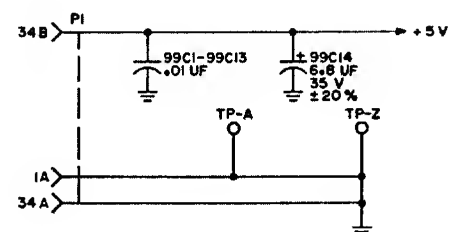
SPARE GATES



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5 V.

2. DELAY TIME FOR REF ONLY.



REFERENCE DRAWINGS
COMP ASSY 54256100

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: BR3BB

DWN	[illegible]	8-17-73
CHK	[illegible]	[illegible]
ENGR	[illegible]	8-17-73
MFG	[illegible]	[illegible]
APPR		

TITLE: SCHEMATIC DIAGRAM SERIALIZER / DESERIALIZER TYPE 3JRV

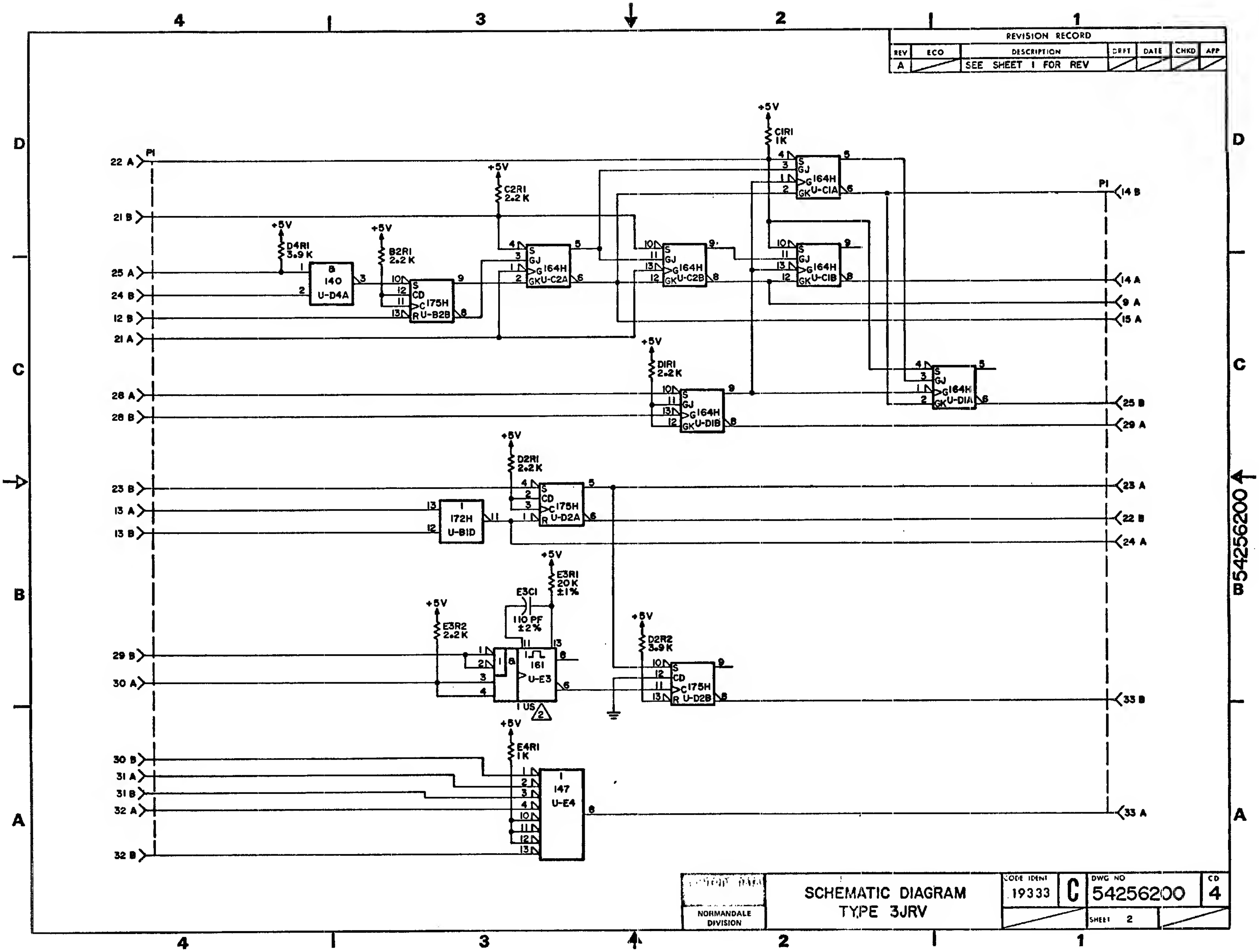
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54256200	4

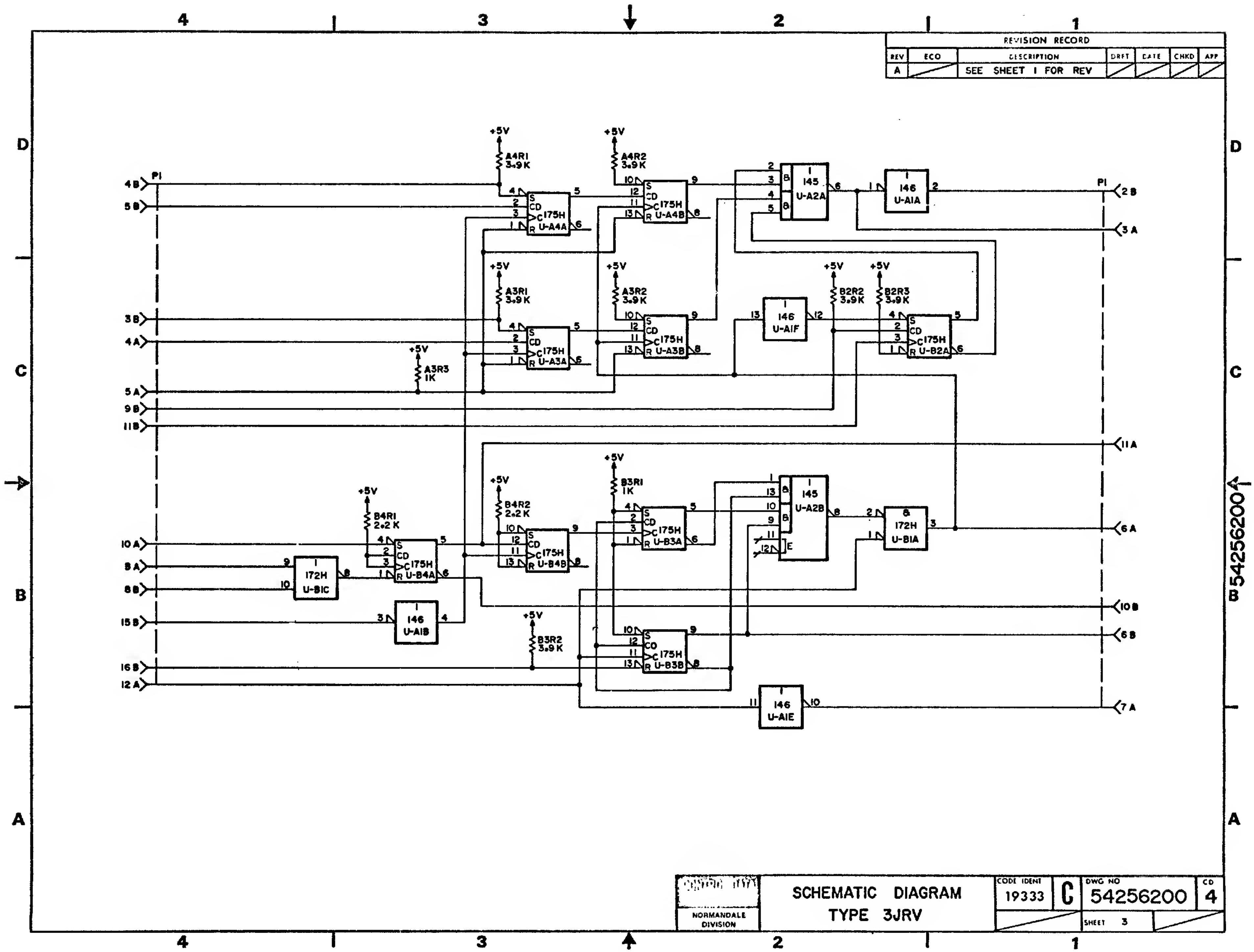
SHEET 1 OF 3

HFD-E

54256200

70629100 E


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
TYPE 3JRV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54256200
CD 4
SHEET 2
54256200

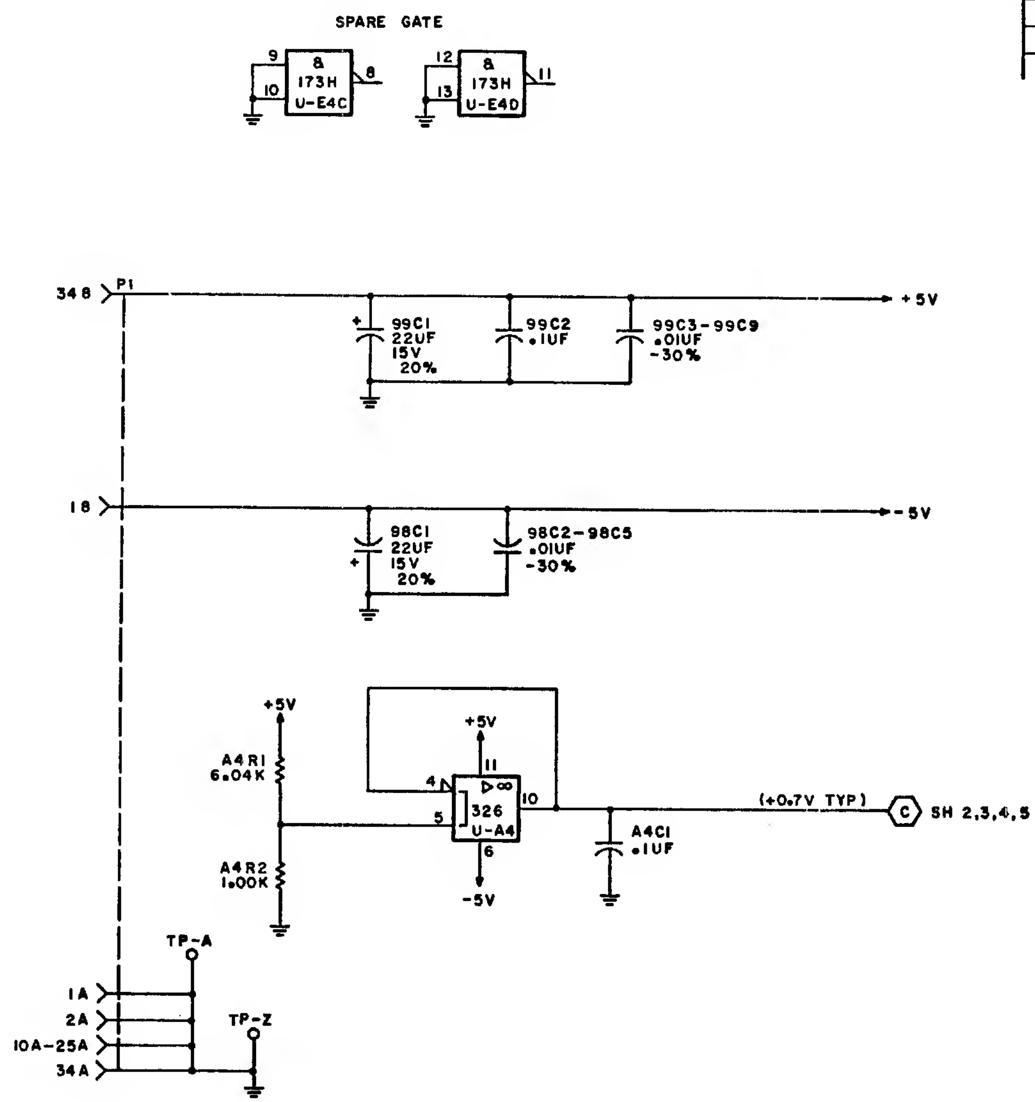

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
SCHEMATIC DIAGRAM
TYPE 3JRV
NORMANDALE DIVISION
CODE IDENT 19333
C
DWG NO 54256200
CD 4
SHEET 3
54256200

70629100 E

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	EFFT	DATE	CHKD	APP
A	[illegible]	RELEASED	[illegible]	[illegible]	[illegible]	[illegible]



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310.
   ALL DIODES, GEMANIUM, 11801200
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.

2. IC TYPE 162 HAS PIN 13 TO -5V.

REFERENCE DRAWINGS			
COMP ASSY: 54256500			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR3B8	
DWN	[illegible]	7-24-73
CHK	[illegible]	8-2-73
ENGR	[illegible]	8-7-73
MFG	[illegible]	8-13-73
APPR		

TITLE SCHEMATIC DIAGRAM RECEIVER/TRANSMITTER TYPE 3JSV

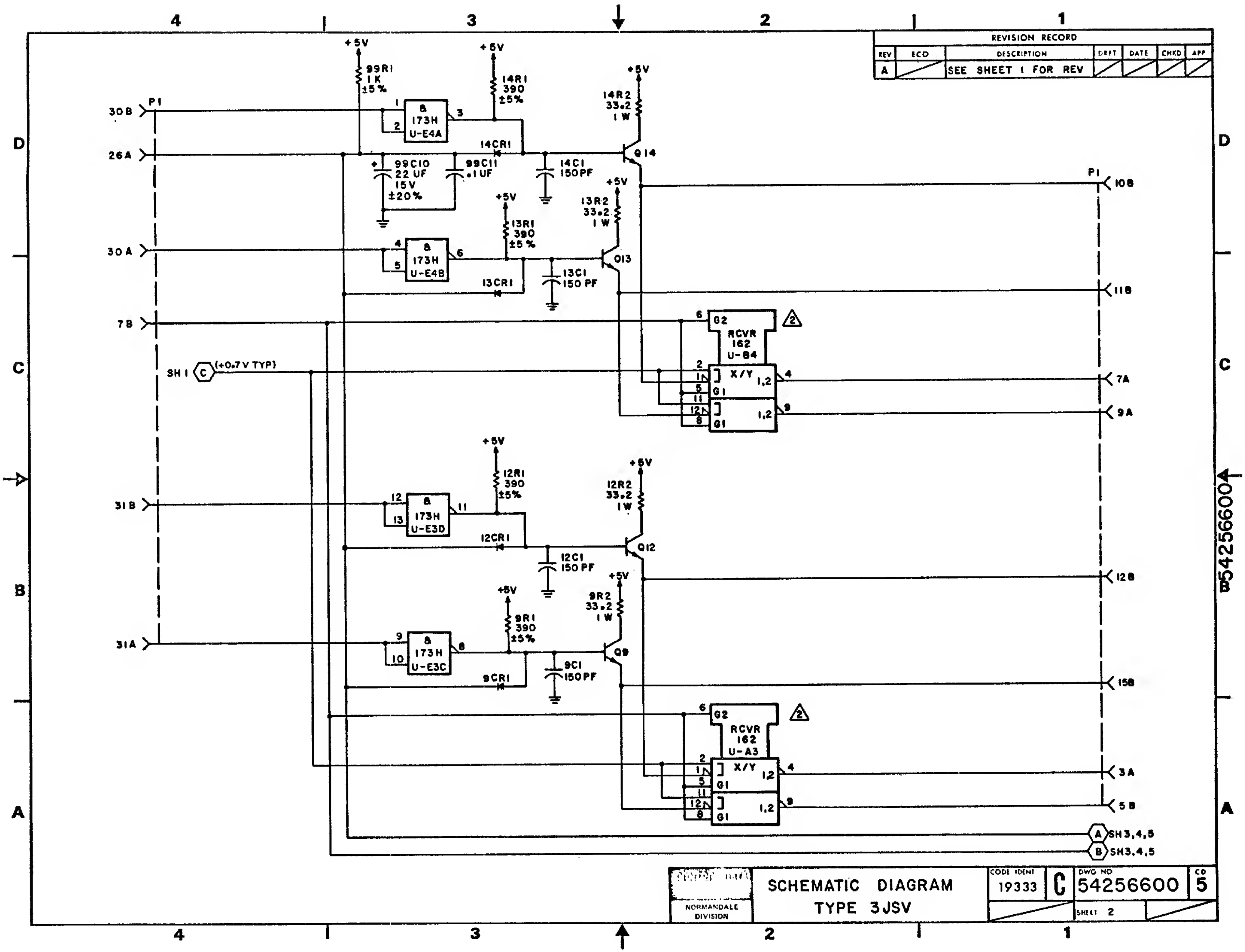
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54256600	5

SHEET 1 OF 5

54256600

HPD-C

4-186



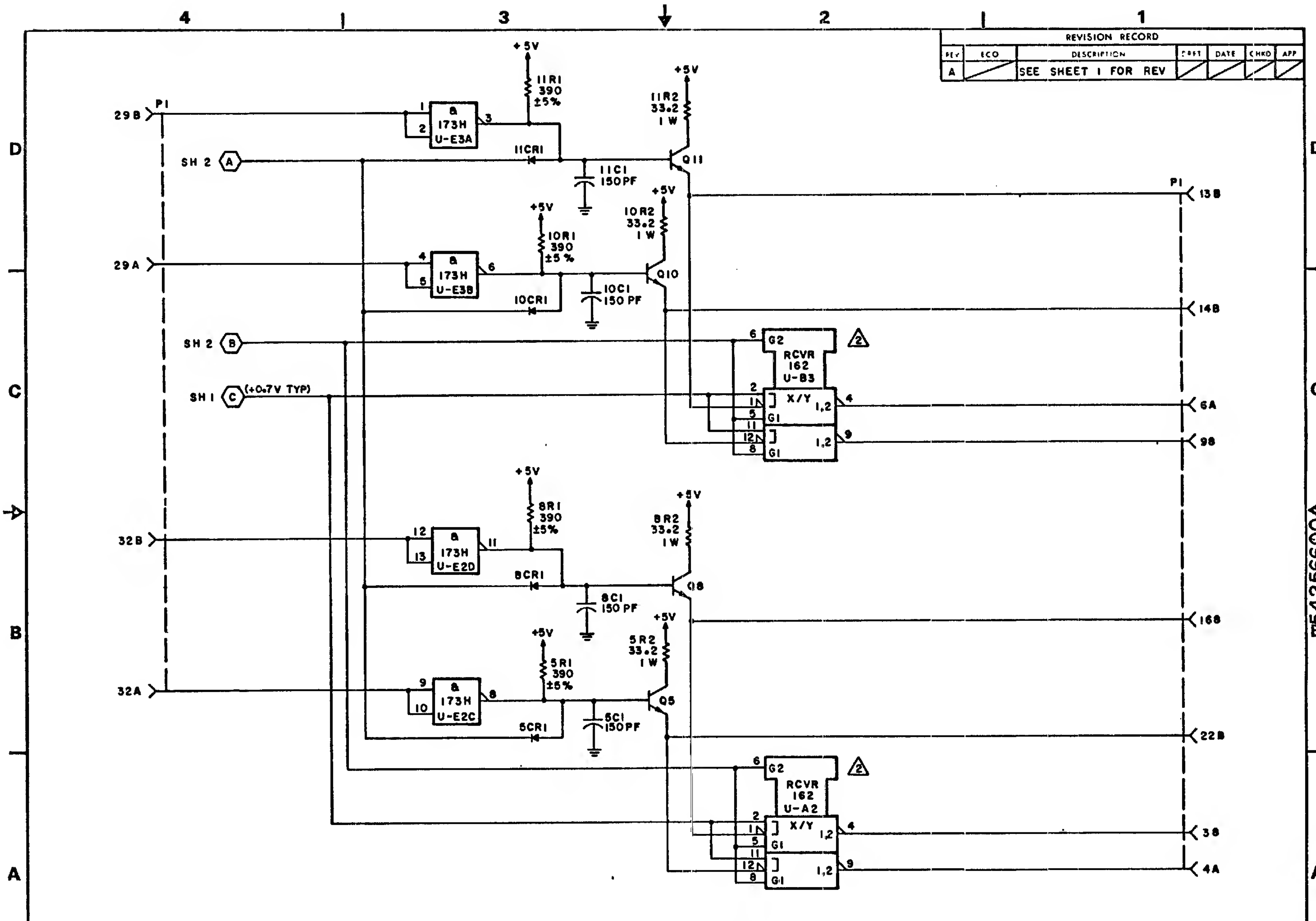
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TYPE 3JSV

CODE IDENT		DWG NO	CD
19333	C	54256600	5
		SHEET 2	

70629100 E

70629100 E



REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

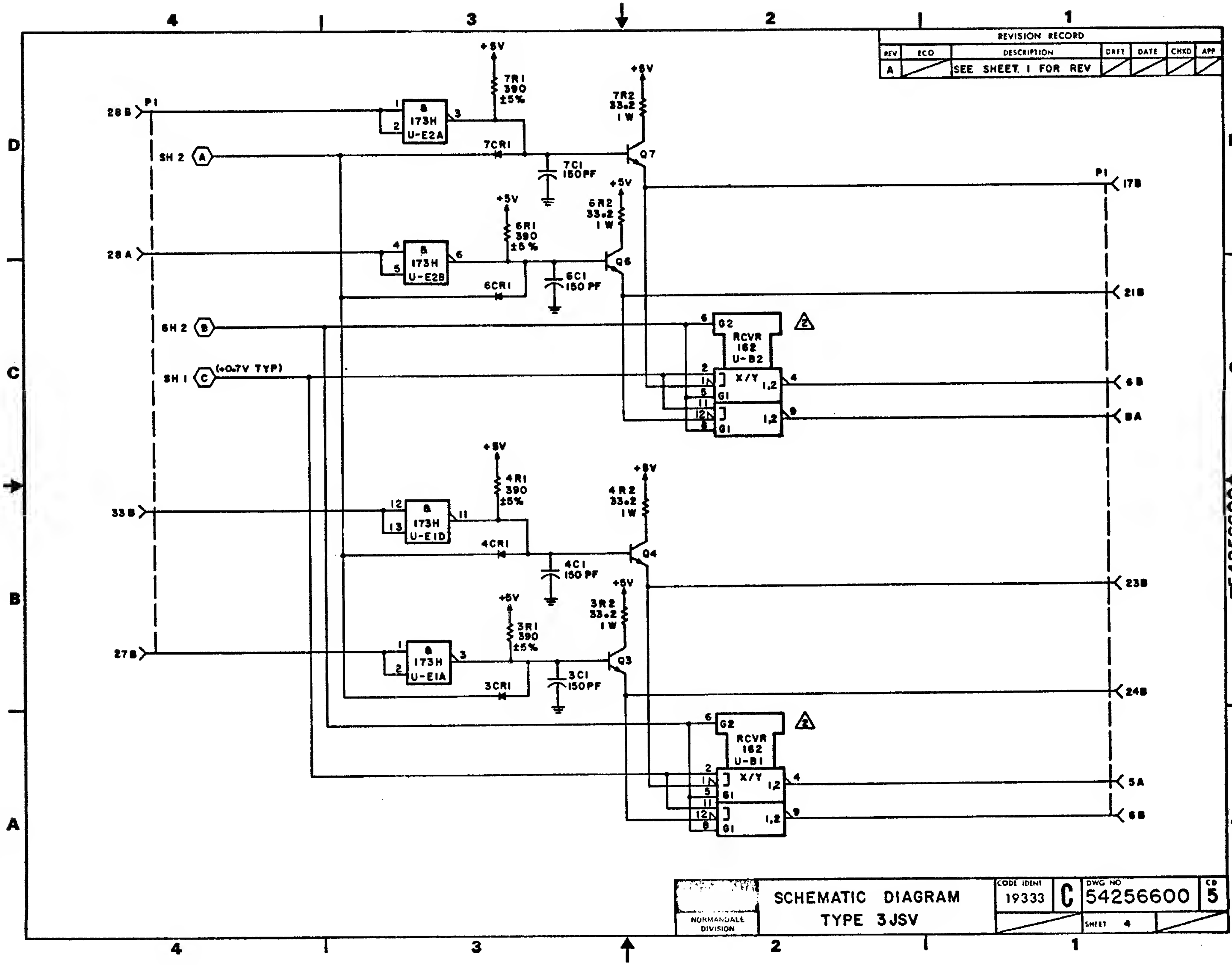
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TYPE 3JSV

CODE IDENT		DWG NO	CD
19333	C	54256600	5

SHEET 3

54256600A



SCHEMATIC DIAGRAM
TYPE 3JSV

NORMANDALE DIVISION

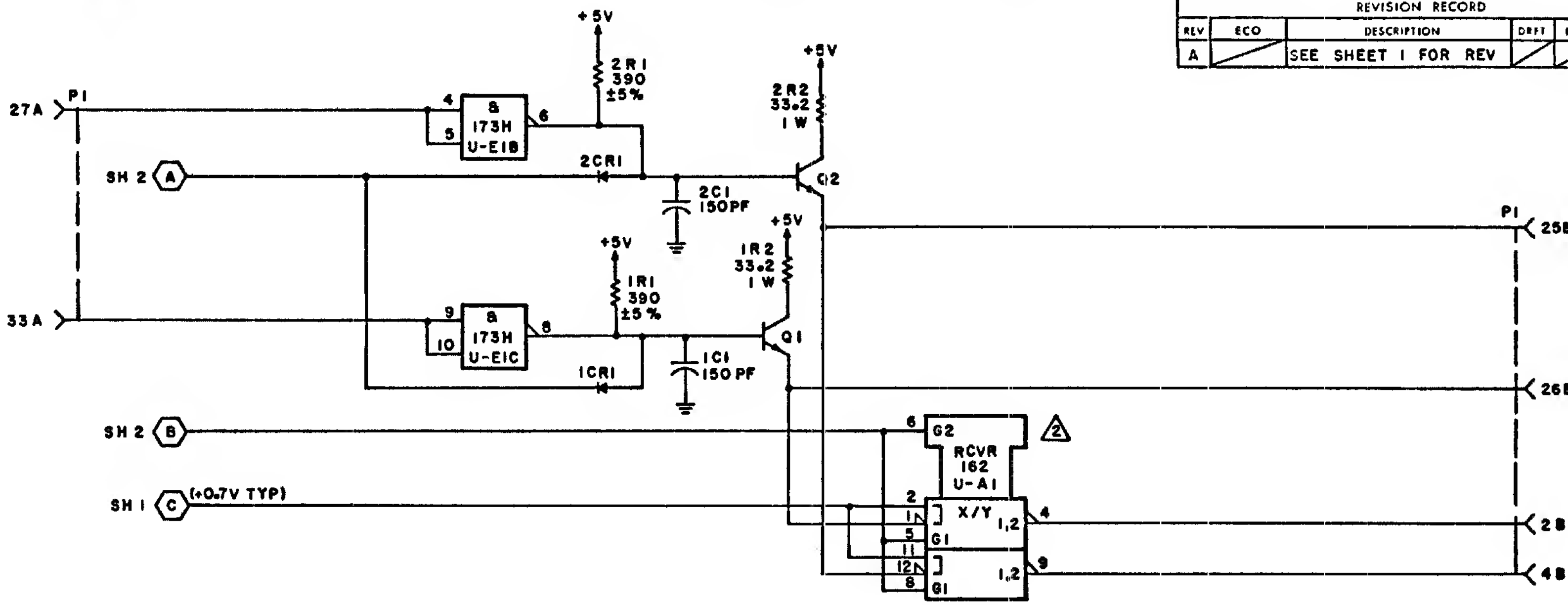
CODE IDENT	SIZE	DWG NO	CD
19333	C	54256600	5

SHEET 4

54256600

70629100 E

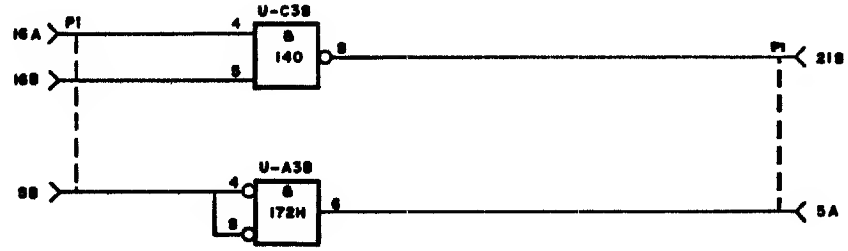
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



54256600A

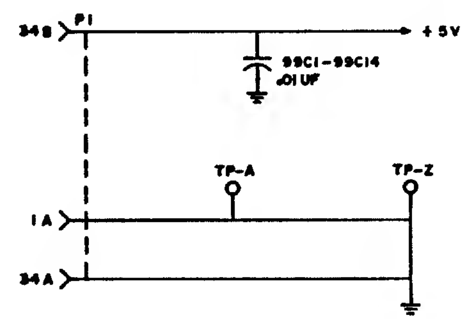
NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JSV	CODE IDENT 19333	C	DWG NO 54256600	CD 5
				SHEET 5	

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED				



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
2. IC'S U-C1, U-D1 AND U-E1 HAVE PIN 5 CONNECTED TO +5V AND PIN 12 CONNECTED TO GROUND.



B54259000

REFERENCE DRAWINGS
COMPONENT ASSY 54258900

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-3?%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

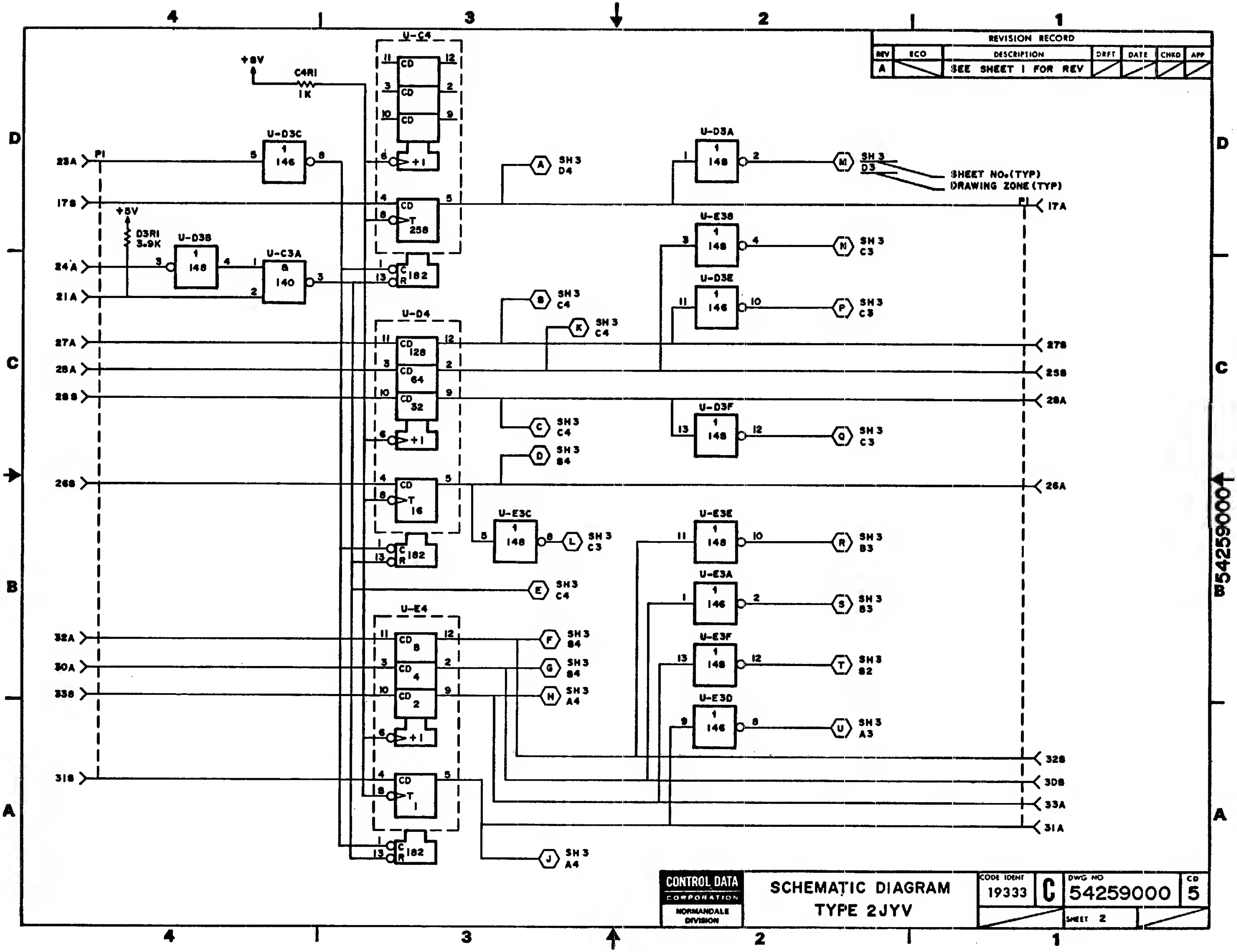
FIRST USED ON	8R3A88	
DWN	R. KONECNY	9-22-72
CHK	[illegible]	10-6-72
ENGR	[illegible]	10/6/72
MFG	[illegible]	10-12-72
APPR	[illegible]	10-12-72

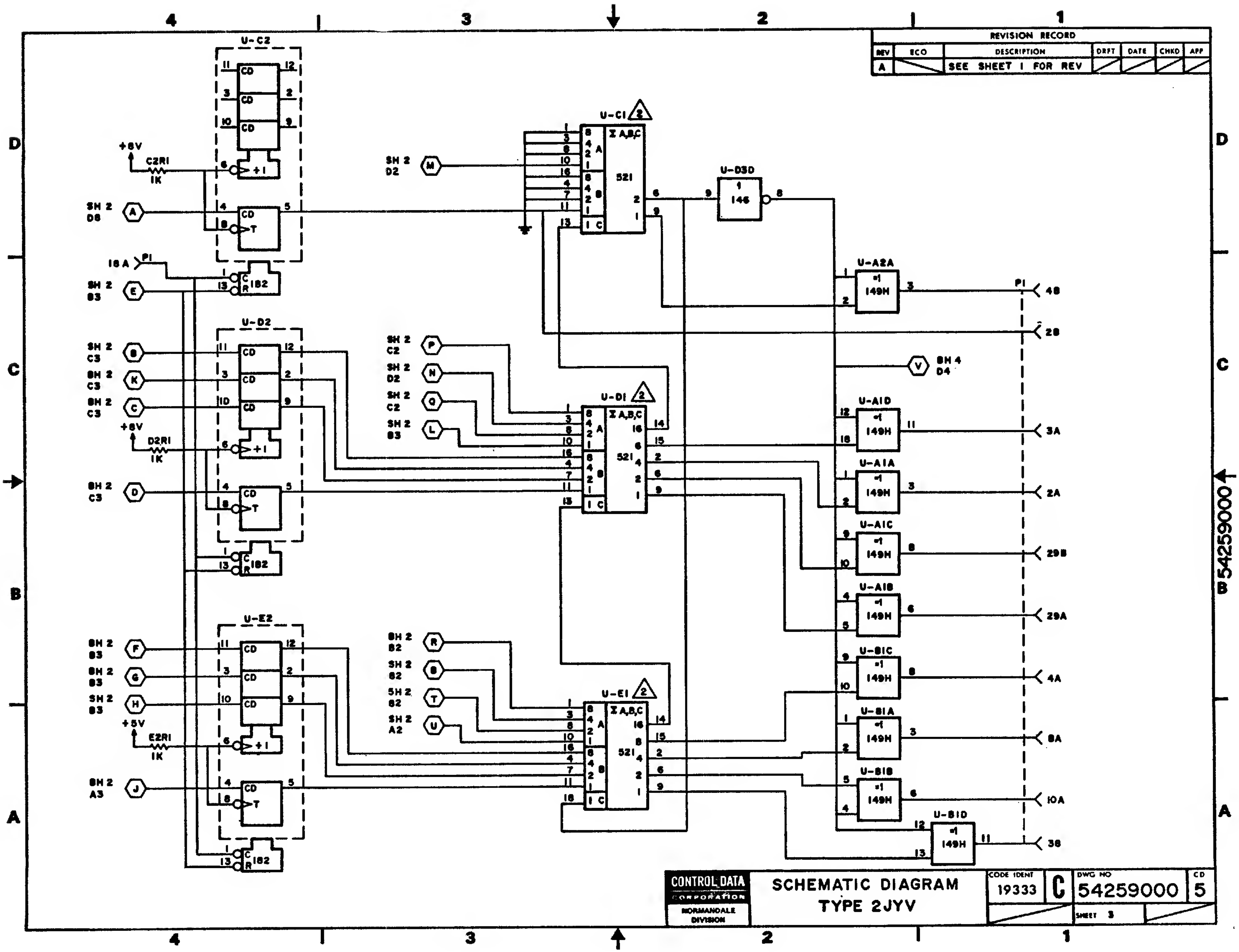
TITLE
SCHEMATIC DIAGRAM DIFFERENCE ADDER TYPE 2JYV

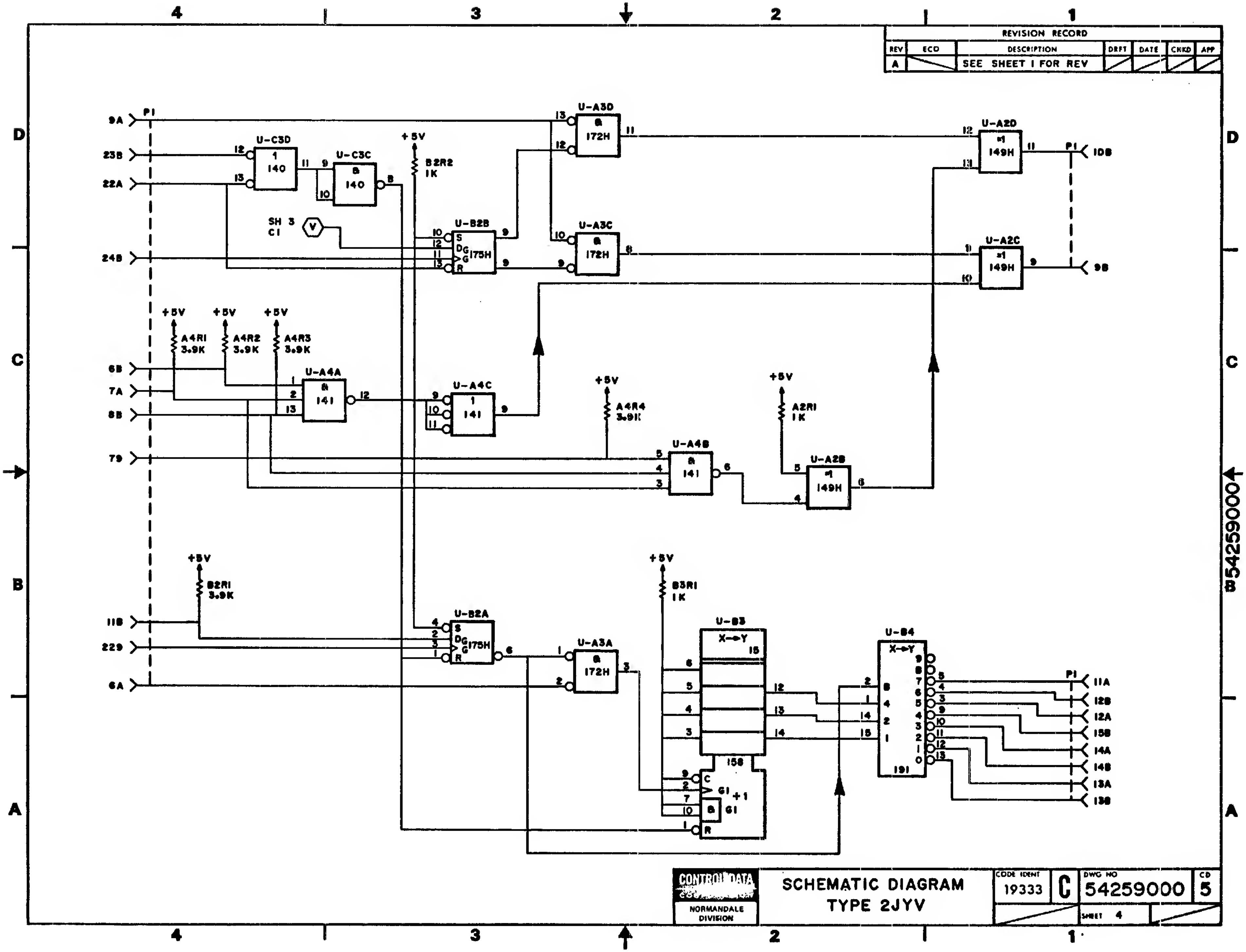
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54259000	5

SHEET 1 OF 4

HPD


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1 FOR REV
CONTROL DATA CORPORATION
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2JYV
CODE IDENT 19333
C
DWG NO 54259000
CD 5
SHEET 2
54259000


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
U-C2
U-D2
U-E2
U-C1
U-D1
U-E1
U-D3D
146
521
182
149H
U-A2A
U-A1D
U-A1A
U-A1C
U-A1B
U-B1C
U-B1A
U-B1B
U-B1D
+5V
C2R1 1K
D2R1 1K
E2R1 1K
16A
P1
SH 2 D2
SH 2 D3
SH 2 B3
SH 2 C3
SH 2 C2
SH 2 B2
SH 2 A3
SH 2 A2
SH 4 D4
48
28
3A
2A
29B
29A
4A
8A
10A
38
CONTROL DATA CORPORATION
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2JYV
CODE IDENT 19333
C
DWG NO 54259000
CD 5
SHEET 3
54259000

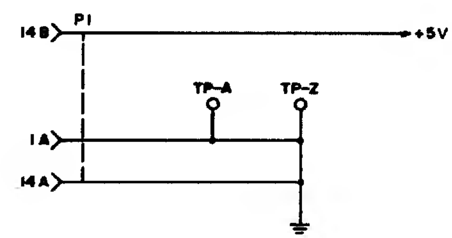

REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CKKD | APP
A | SEE SHEET 1 FOR REV
P1
9A
23B
22A
24B
6B
7A
8B
79
11B
229
6A
10B
9B
11A
12B
12A
15B
14A
14B
13A
13B
U-C3D
140
U-C3C
140
U-B2B
175H
U-A3D
172H
U-A3C
172H
U-A2D
149H
U-A2C
149H
SH 3
C1
+5V
B2R2
1K
A4R1
3.9K
A4R2
3.9K
A4R3
3.9K
U-A4A
141
U-A4C
141
A4R4
3.9K
U-A4B
141
A2R1
1K
U-A2B
149H
B2R1
3.9K
U-B2A
175H
U-A3A
172H
B3R1
1K
U-B3
X→Y
158
U-B4
X→Y
191
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE 2JYV
CODE IDENT
19333
C
DWG NO
54259000
CD
5
SHEET 4
54259000 B

4-194

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED	[illegible]	[illegible]		[illegible]

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
AND PIN 14 CONNECTED TO +5V.
ALL TRANSISTORS SNPN 2N3569 PN 50210811

54120601



REFERENCE DRAWINGS			
COMP ASSY: 54120501			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

USED ON: BR 301

DWN	[illegible]	5-10-73
CHK	[illegible]	5-17-73
ENGR	[illegible]	[illegible]
MFG	[illegible]	
APPR	[illegible]	

TITLE
SCHEMATIC DIAGRAM LAMP & RELAY DRIVER TYPE 3PBV

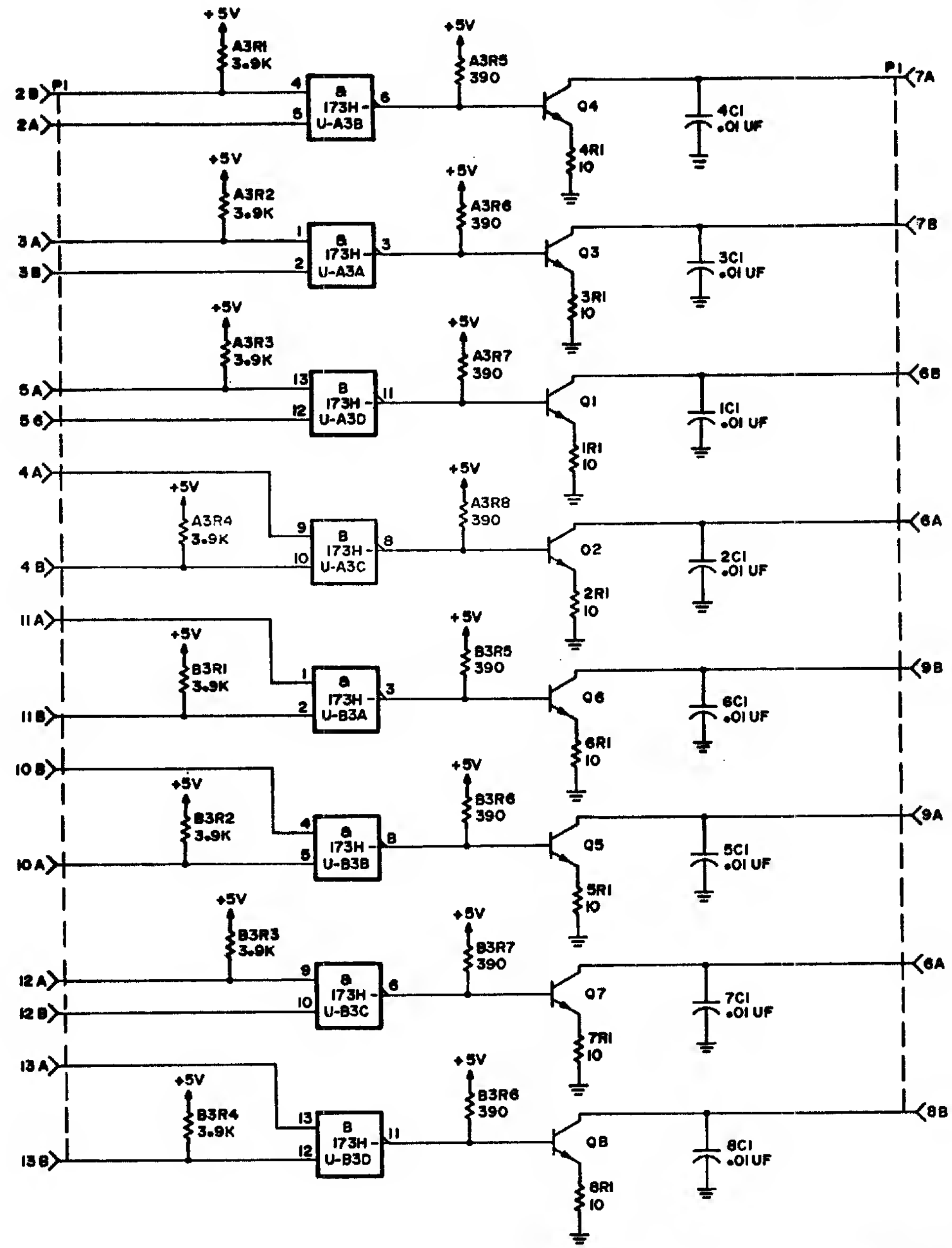
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54120601	7

SHEET 1 OF 2

70629100 F

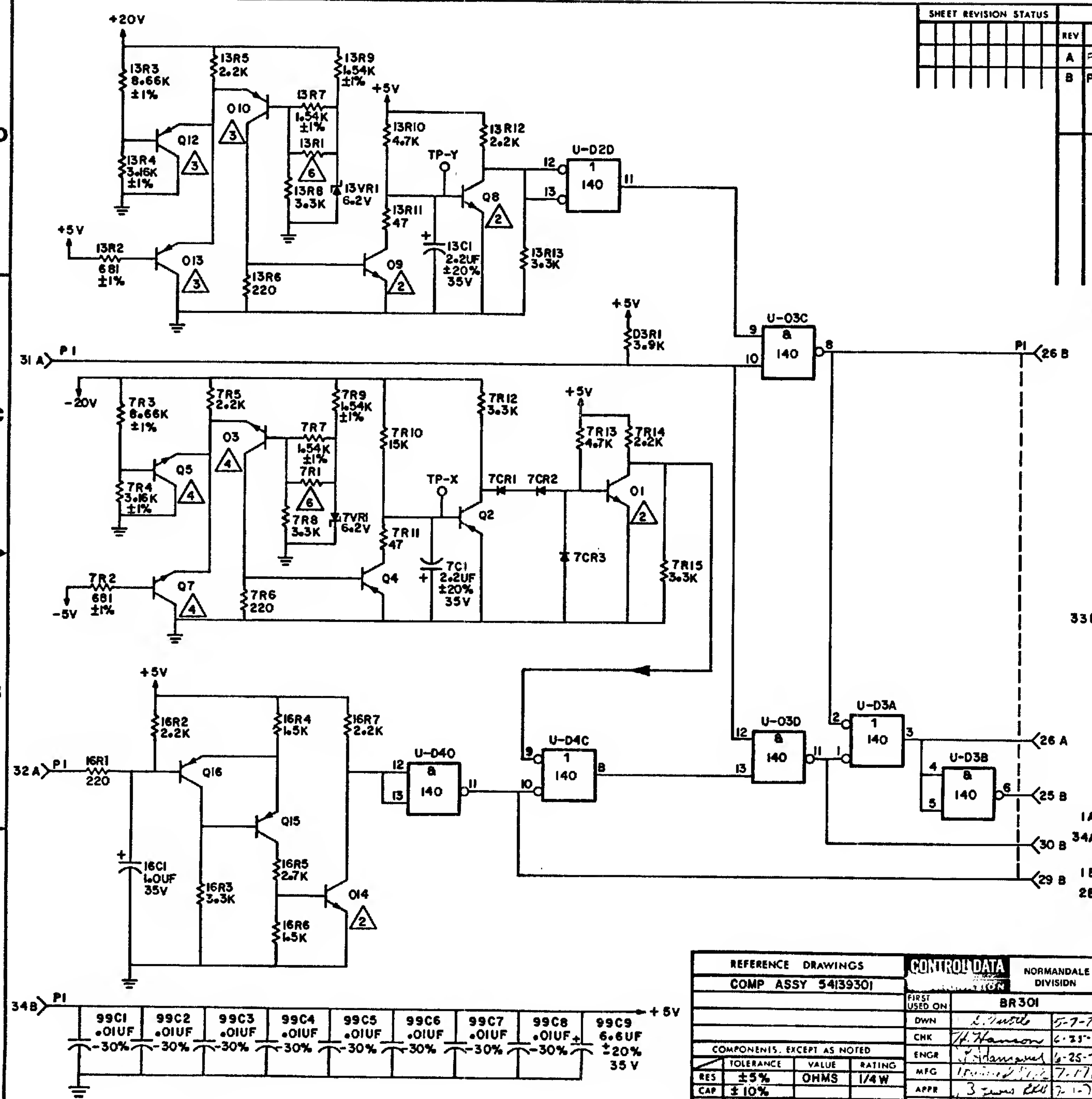
70629100 F

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA CORPORATION NORMANDALE DIVISION	SCHEMATIC DIAGRAM LAMP & RELAY DRIVER TYPE 3PBV	CODE IDENT 19333	C	DWG NO 54120601	CD 7
				SHEET 2	

54120601



33B
P1
+20V
99C10 6.6UF ±20% 35V
TP-A TP-Z
1A
34A
1 B
-5V
2B
-20V
98C1 6.8UF ±20% 35V

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED			7/12/71	
	B	PE30060	TYPE WAS 1QZV-ASSY WAS 54139300-PIN 17A ADDED AS INPUT TO U-C4A	CC	7/30/71		I-NR

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   ALL DIODES, SILICON, 92115021.
2. TRANSISTOR, SNPN, 2N3646, 50210310.
3. TRANSISTOR, SPNP, 2N4250, 50211411.
4. TRANSISTOR, SNPN, 2N3565, 50210710.
5. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
6. RESISTORS 13R1 AND 7R1 TO BE SELECTED IN PRODUCTION PER RECOMMENDED ENGINEERING TEST PROCEDURE FROM A VALUE RANGE OF 100Ω TO 6.81K ±1%.
7. DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS
COMP ASSY 54139301

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	± 10%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR301	
DWN	[signature]	5-7-71
CHK	H. Hanson	6-23-71
ENGR	[signature]	6-25-71
MFG	[signature]	7-1-71
APPR	[signature]	7-1-71

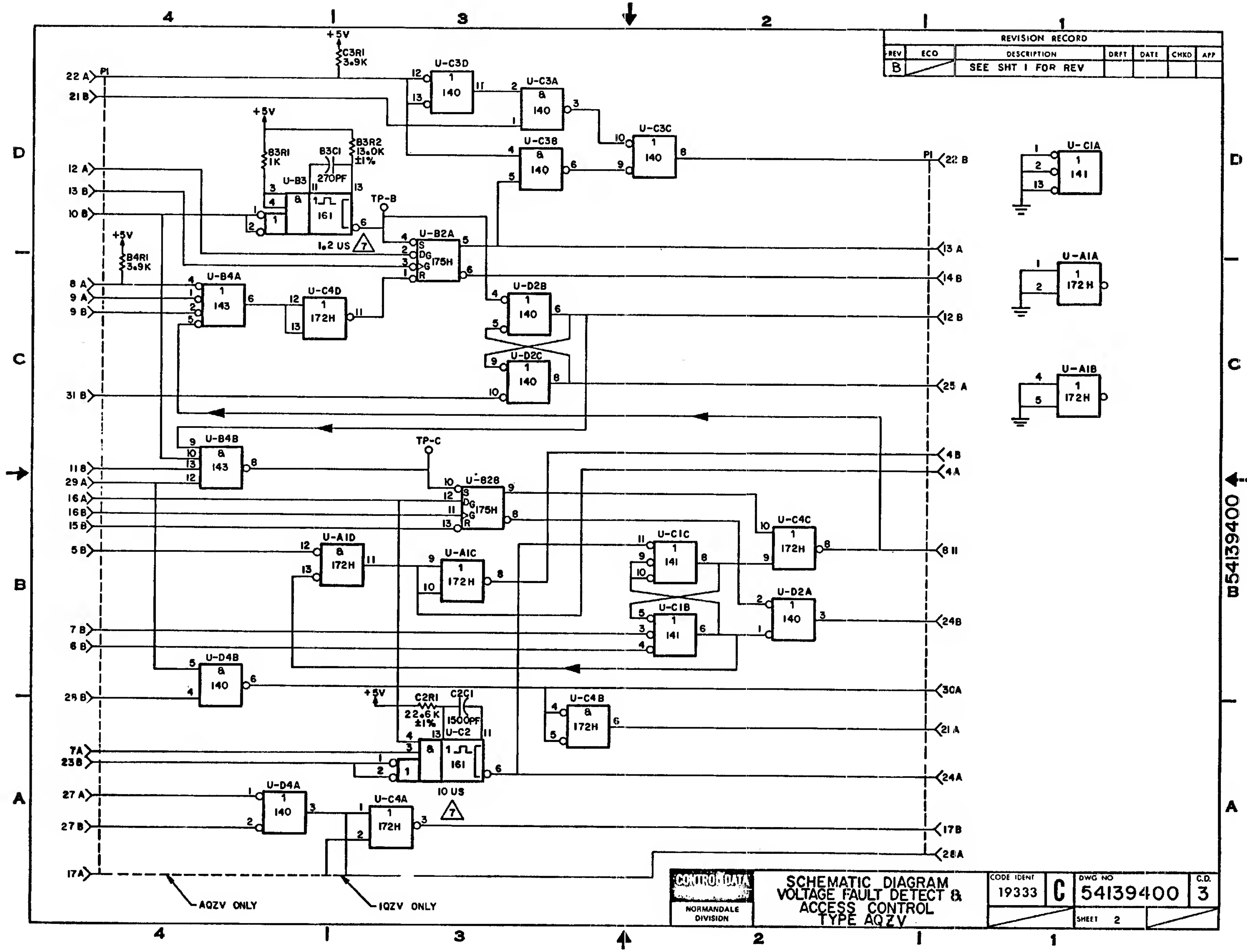
TITLE: SCHEMATIC DIAGRAM VOLTAGE FAULT DETECT & ACCESS CONTROL TYPE AQZV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54139400	3

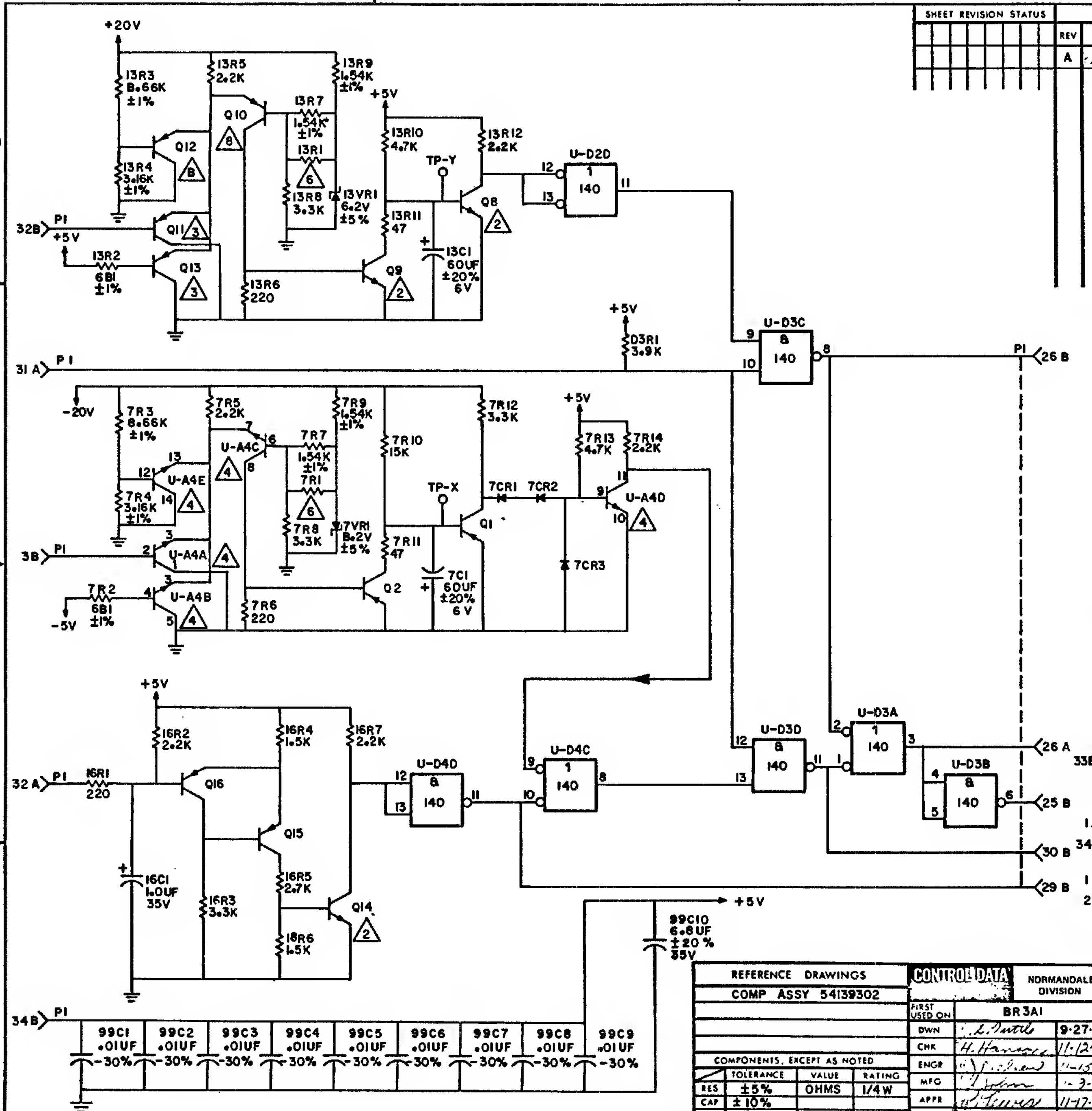
SHEET 1 OF 2

54139400

70629100 E



4-197



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED		11-22-71		[illegible]

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SPNP, 2N4258, 50211510.
   ALL DIODES, SILICON, 92115021.
2. TRANSISTOR, SNPN, 2N3646, 50210310.
3. TRANSISTOR, SPNP, 2N4916, 50211612 MATCHED PAIR.
4. TRANSISTOR, ARRAY, RCA CA3045.
5. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V, EXCEPT CA3045.
6. RESISTORS 13R1 AND 7R1 TO BE SELECTED IN PRODUCTION PER RECOMMENDED ENGINEERING TEST PROCEDURE FROM A VALUE RANGE OF 100Ω TO 6.81K ±1%.
7. DELAY TIME FOR REFERENCE ONLY.
8. TRANSISTOR, SPNP, 2N4916, 50211610.

REFERENCE DRAWINGS
COMP ASSY 54139302

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON: BR3A1

DWN	[signature]	9-27-71
CHK	H. Hanson	11-12-71
ENGR	[signature]	11-15-71
MFG	[signature]	11-3-71
APPR	[signature]	11-17-71

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

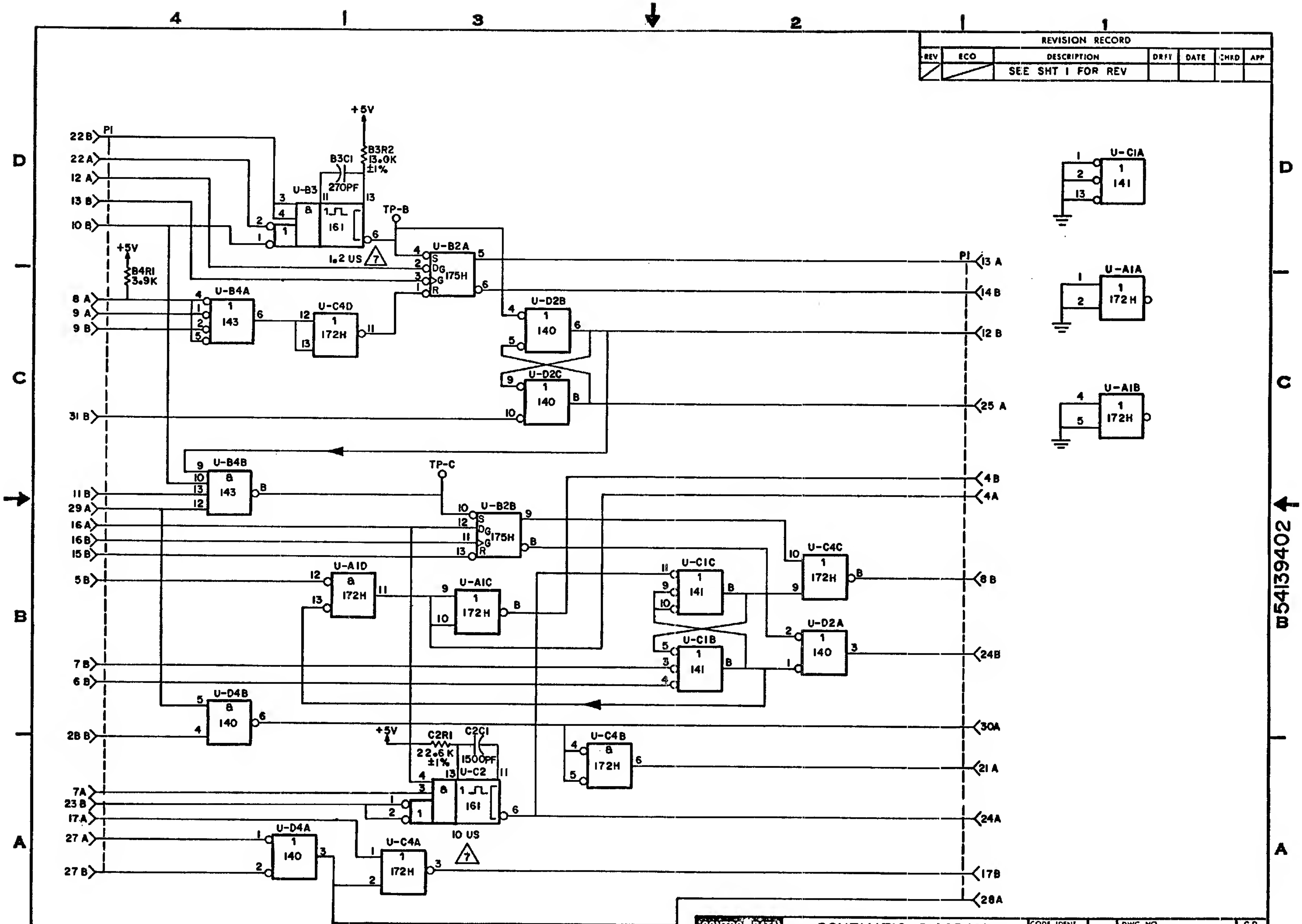
TITLE: SCHEMATIC DIAGRAM VOLTAGE FAULT DETECT & ACCESS CONTROL TYPE BQZV

CODE IDENT 19333 C DRAWING NUMBER 54139402 C.D. 9

SHEET 1 OF 2

54139402

HPD



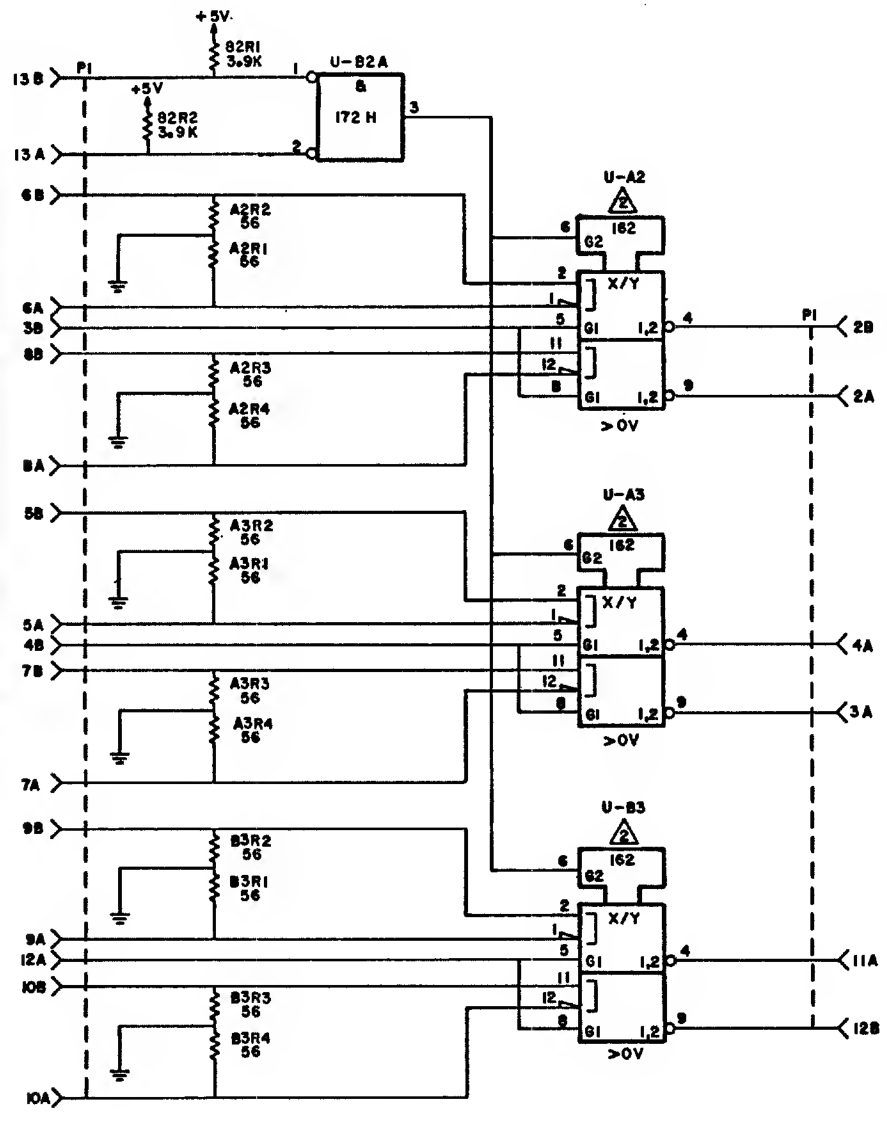
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHT 1 FOR REV				

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
VOLTAGE FAULT DETECT &
ACCESS CONTROL
TYPE BQZV

CODE IDENT		DWG NO	C.D.
19333	C	54139402	9
		SHEET 2	

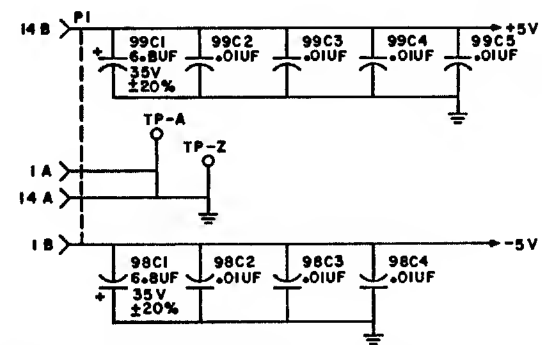
SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23000	RELEASED			3/41	[illegible]

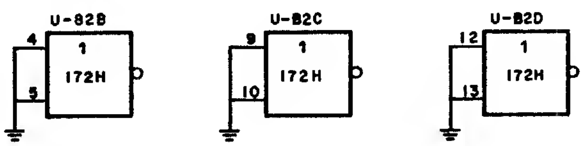


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL I.C'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.

2. I.C. A2, A3, AND B3 HAVE PIN 13 CONNECTED TO -5V.





REFERENCE DRAWINGS	CONTROL DATA CORPORATION	NORMANDALE DIVISION
COMPONENT ASSY. 54140901	FIRST USED ON	BR 301
	DWN	E. TIBESAR 4/23/71
	CHK	H. Hanson 6-23-71
COMPONENTS, EXCEPT AS NOTED	ENGR	P Adamaris 6-23-71
	MFG	[illegible] 6-31-71
	APPR	[illegible] 6-30-71

	TOLERANCE	VALUE	RATING
RES	± 5 %	OHMS	1/4 W
CAP	-30 %		

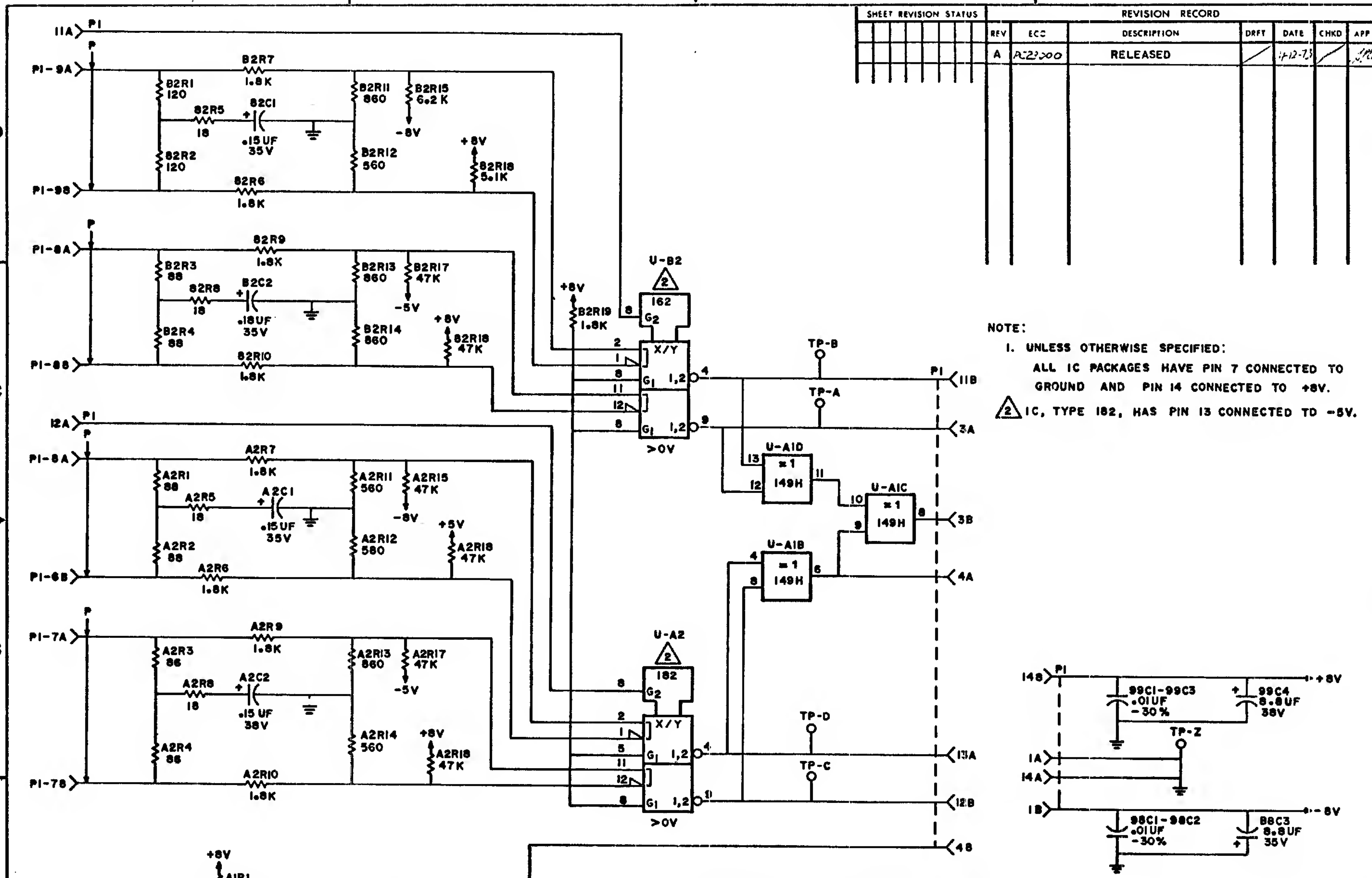
TITLE

SCHEMATIC DIAGRAM RECEIVER TYPE 1RCV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54141001	5

SHEET 1 OF 1

54141001



SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	AC23300	RELEASED		4-12-73		

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.

2. IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.

REFERENCE DRAWINGS	
COMP ASSY	54144101

COMPONENTS EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON: BR3A1G

DWN		4-9-73
CHK		4-10-73
ENGR		4-10-73
MFG		4-11-73
APPR		

TITLE: SCHEMATIC DIAGRAM RECEIVER TYPE 3RLV

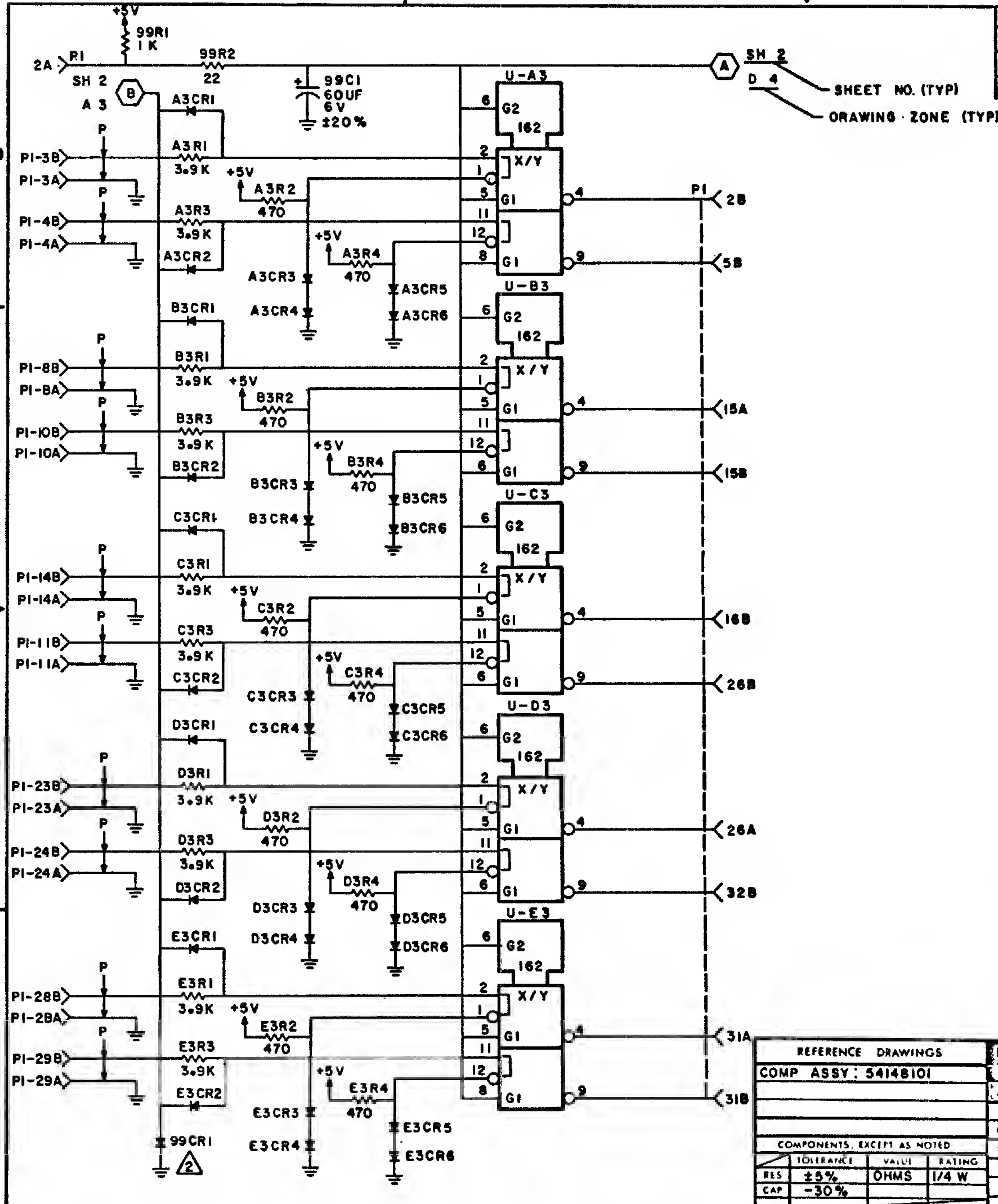
CODE IDENT 19333 — C — DRAWING NUMBER 54144201 — CD 8

SHEET 1 OF 1

B54144201

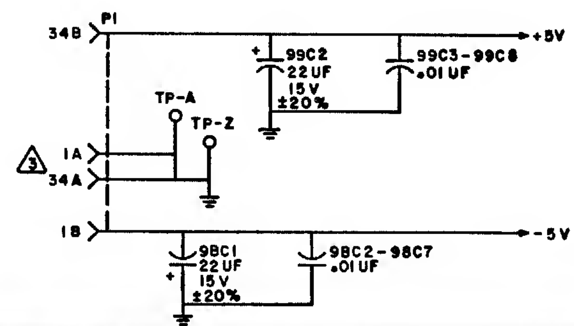
HPD

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	DE23002	RELEASED		6-21-73		



NOTE:

1. UNLESS OTHERWISE SPECIFIED: ALL 14 PIN IC'S HAVE PIN 14 CONNECTED TO +5V; PIN 7 TO GND; AND PIN 13 TO -5V. ALL DIODES, SILICON, 92115021
2. LIGHT EMITTING DIODE, 94256300.
3. ALL UNUSED CONNECTOR PINS ARE TIED TO GND.



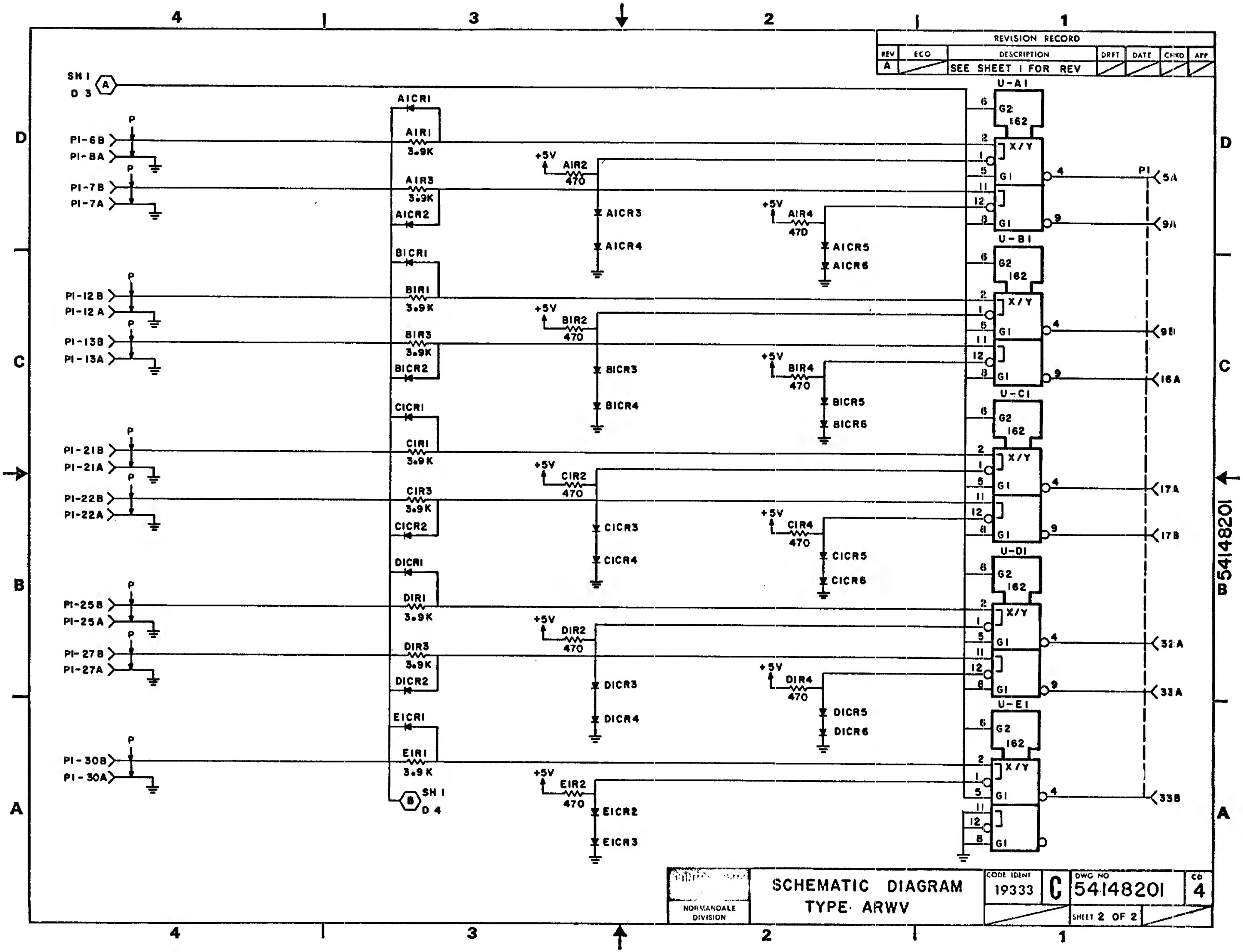
REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY: 54148101	FIRST USED ON	BR501	SCHEMATIC DIAGRAM CHANNEL I/O RECEIVERS TYPE ARWV
	DWN		
	CHK		
COMPONENTS, EXCEPT AS NOTED	ENGR		CODE IDENT 19333 · C · DRAWING NUMBER 54148201 · CD 4
	MFG		
	APPR		SHEET 1 OF 2

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

54148201

HPD-E

70629100 E

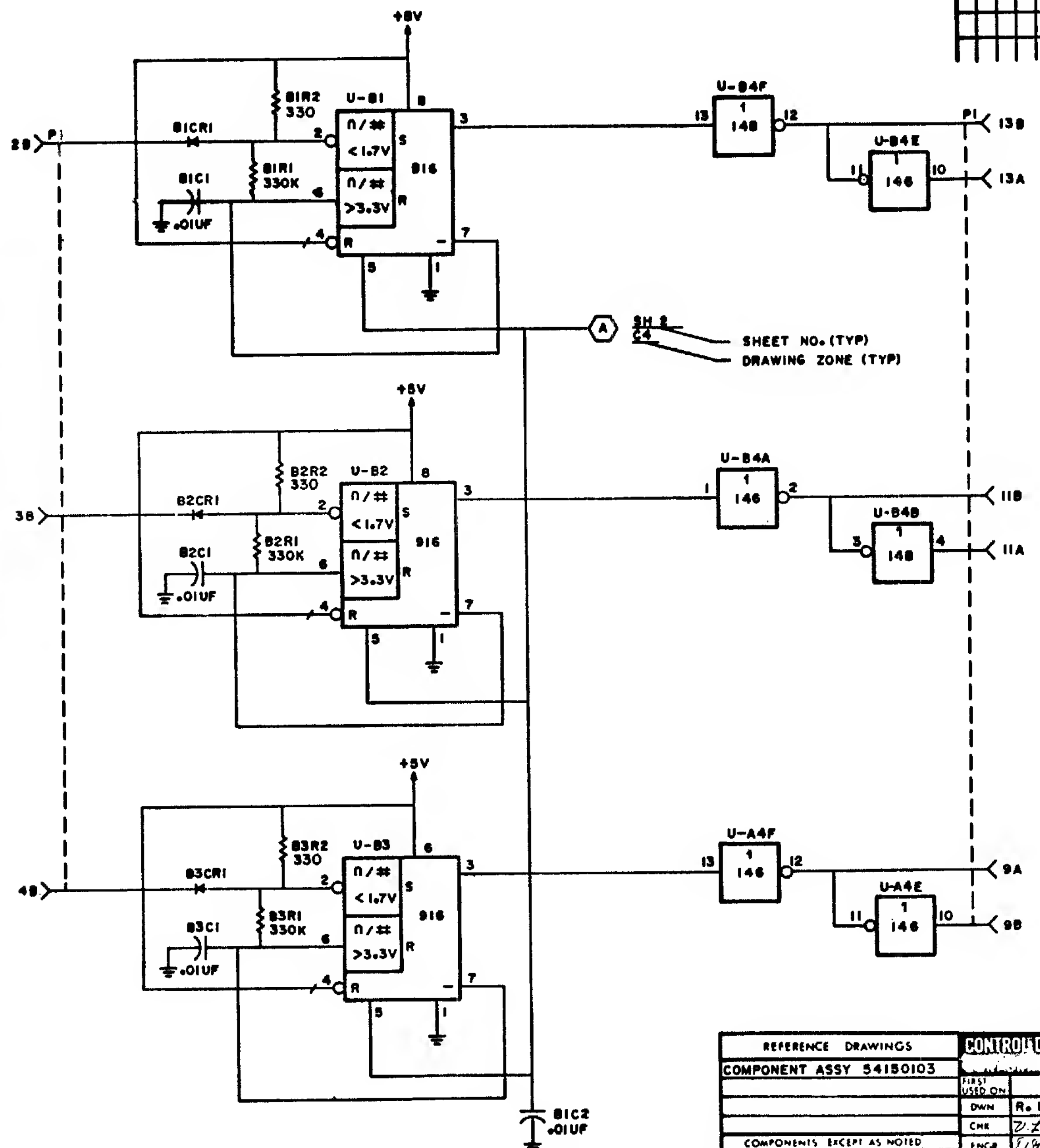


4-203

SHEET REVISION STATUS						

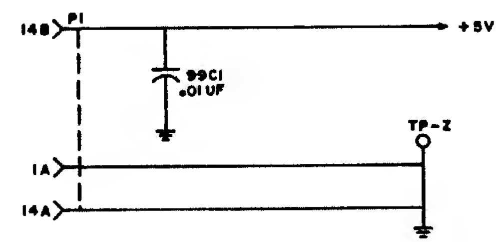
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE43000	RELEASED				



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
   ALL DIODES, GERMANIUM, 11801200.



B54150203

REFERENCE DRAWINGS
COMPONENT ASSY 54150103

COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

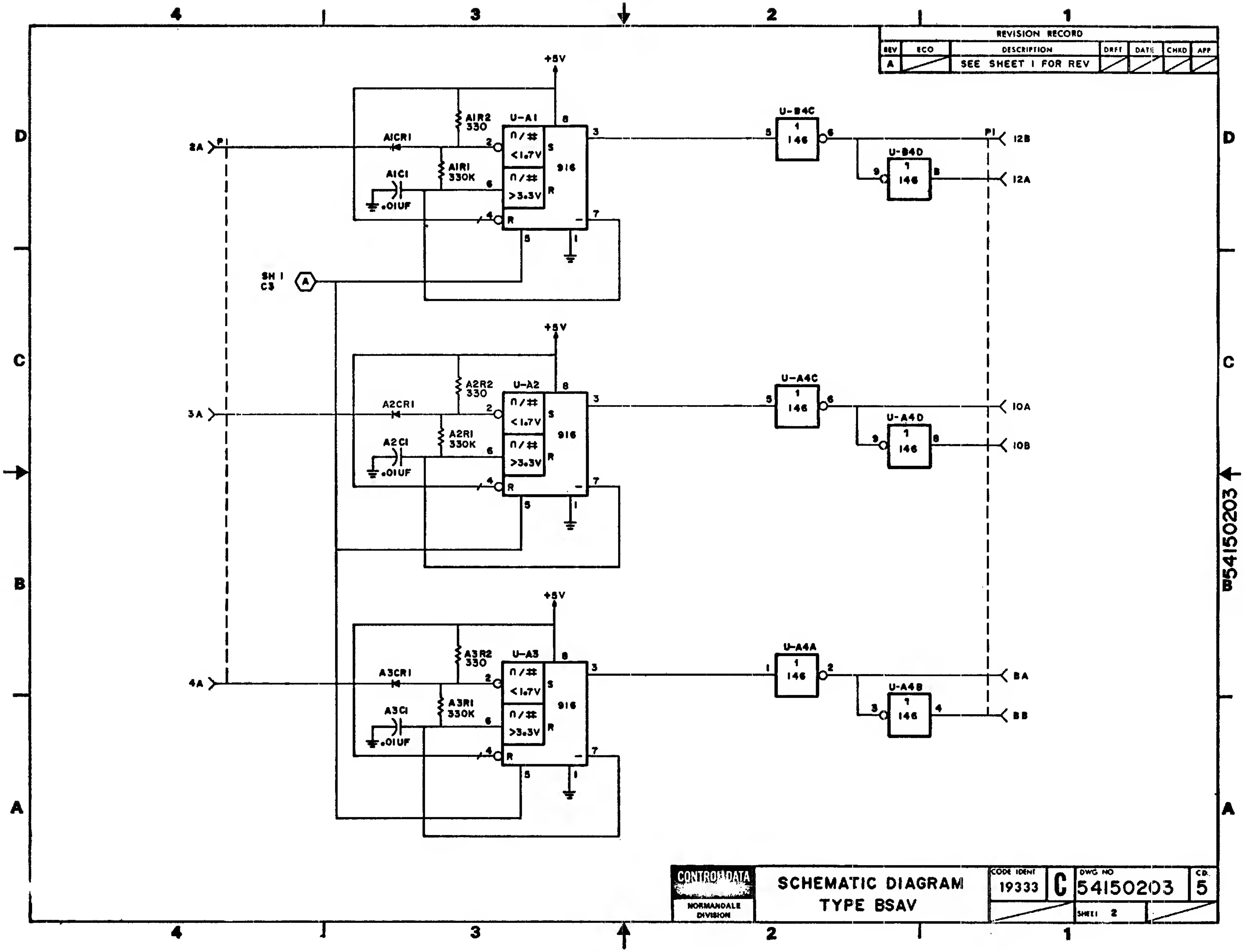
FIRST USED ON	8R302	
DWN	R. KONECNY	2-11-74
CHK	D. L. Rutherford	2-11-74
ENGR		2-11-74
MFG		
APPD		

TITLE: SCHEMATIC DIAGRAM SWITCH RECEIVER TYPE BSAV

CODE IDENT 19333 | C | DWG NO. 54150203 | CO 5

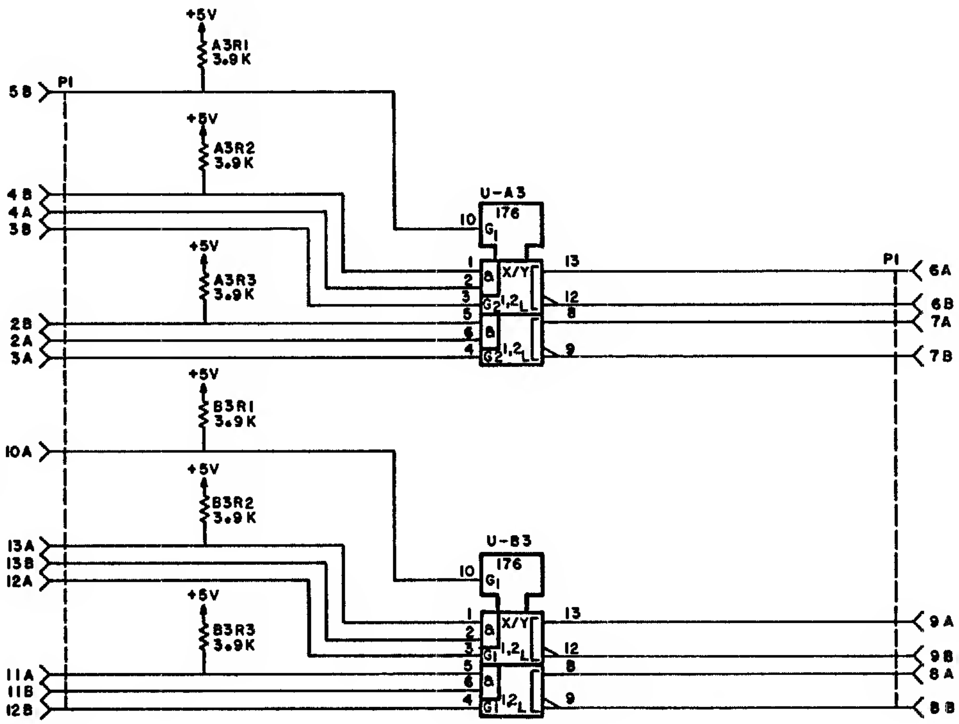
SHEET 1 OF 2

70629100 F

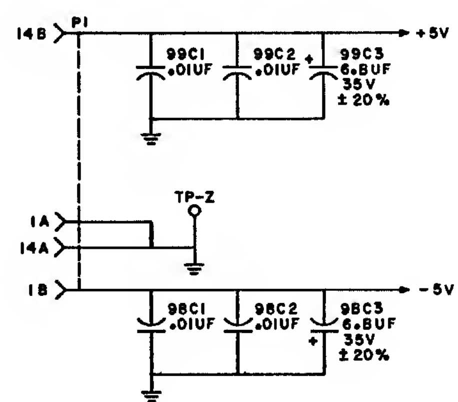

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
A SEE SHEET 1 FOR REV
+5V
A1R2 330
U-A1
A1CR1
A1R1 330K
A1C1
.01UF
2A
P1
916
SH 1 C3
A
U-B4C
146
U-B4D
146
12B
12A
+5V
A2R2 330
U-A2
A2CR1
A2R1 330K
A2C1
.01UF
3A
916
U-A4C
146
U-A4D
146
10A
10B
+5V
A3R2 330
U-A3
A3CR1
A3R1 330K
A3C1
.01UF
4A
916
U-A4A
146
U-A4B
146
8A
8B
<1.7V
>3.3V
54150203
CONTROL DATA
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
TYPE BSAV
CODE IDENT 19333
C
DWG NO 54150203
CD. 5
SHEET 2

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE23003	RELEASED				

REVISION RECORD



NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   ALL IC'S HAVE PIN 7 CONNECTED TO GND; PIN 11 CONNECTED TO -5V; AND PIN 14 CONNECTED TO +5V.



54161001

REFERENCE DRAWINGS
COMP ASSY: 54160901

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	- 30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR301
DWN	7-14-71
CHK	7-28-71
ENGR	7-28-71
MFG	8-4-71
APPR	8-4-71

TITLE
SCHEMATIC DIAGRAM TRANSMITTER TYPE 1TCV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54161001	0

SHEET 1 OF 1

HPD

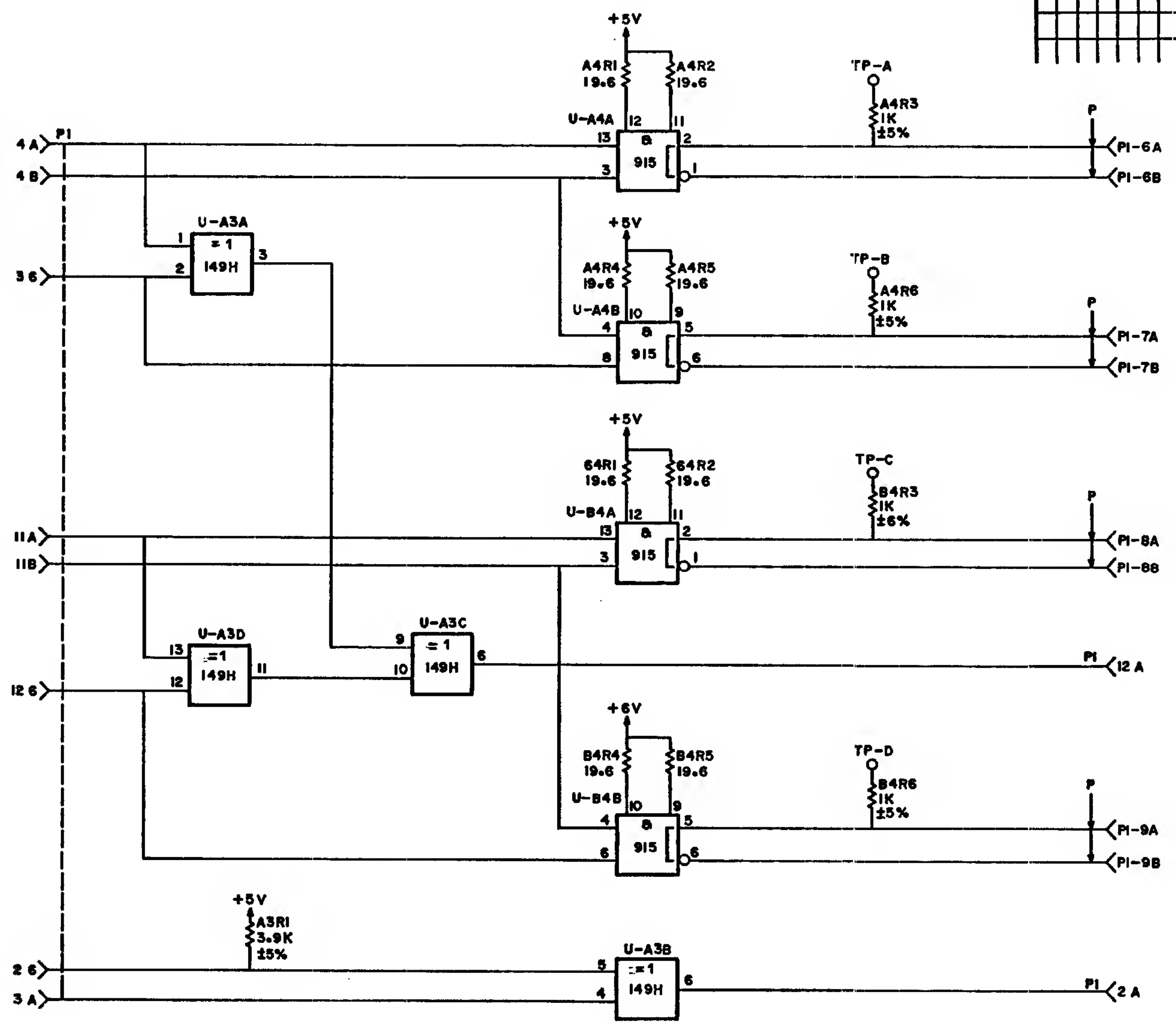
70629100 E

70629100 E

SHEET REVISION STATUS							

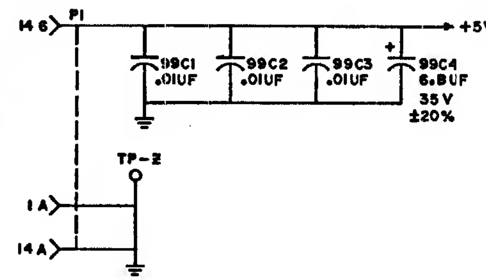
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PEC3000	RELEASED		3-22-72		PIR



NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



54164200

REFERENCE DRAWINGS
COMP ASSY 54164100

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±1 %	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR3AIG	
DWN	D. G. TUTTLE	1-20-72
CHK	[signature]	2-26-72
ENGR	[signature]	3-15-72
MFG	[signature]	3-20-72
APPR	[signature]	3-20-72

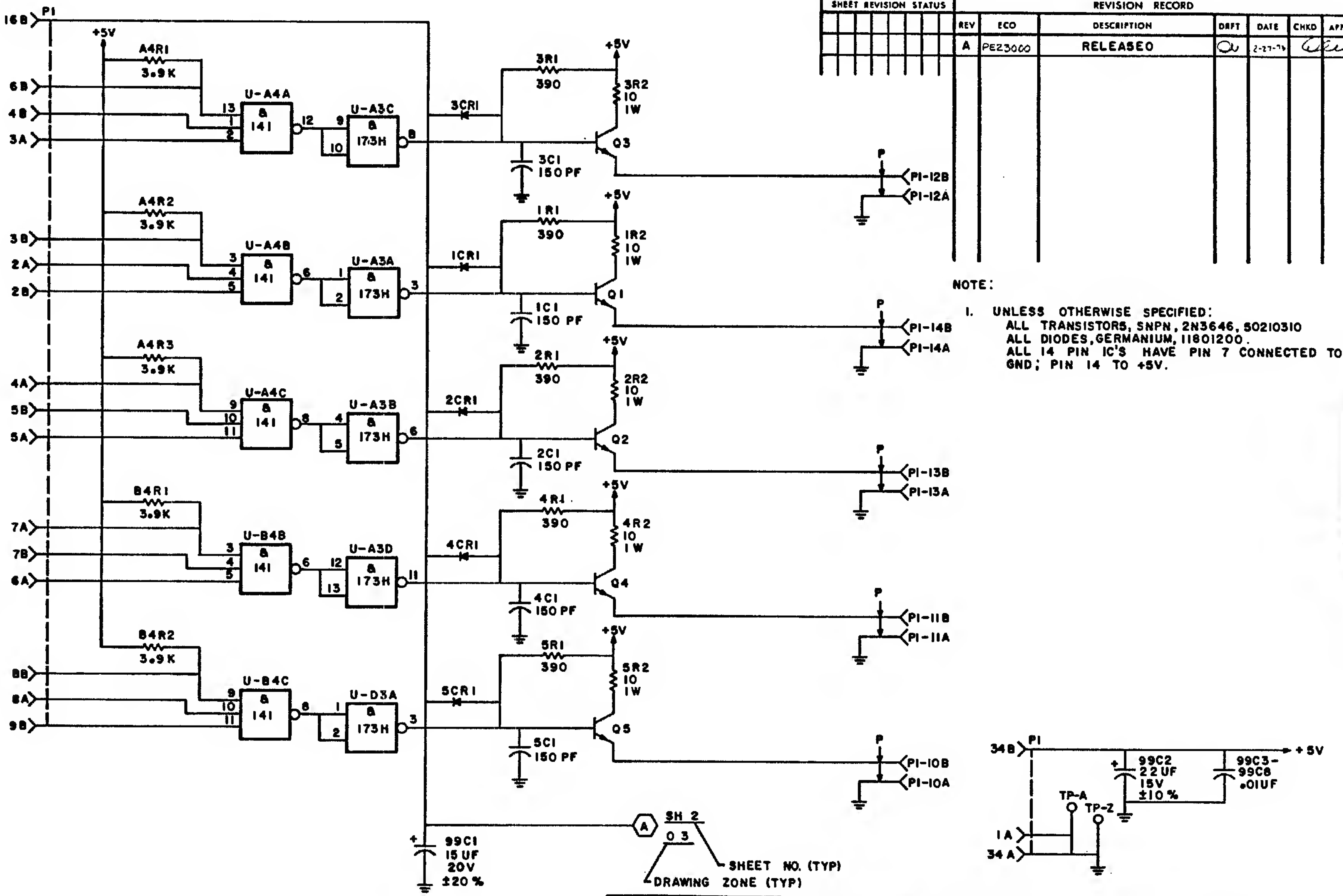
TITLE

SCHEMATIC DIAGRAM TRANSMITTER TYPE 2TLV

CODE IDENT	SIZE	DRAWING NUMBER	C.D.
19333	C	54164200	5

SHEET 1 OF 1

HPD



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, GERMANIUM, 11801200.
   ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V.

SHEET REVISION STATUS						

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		2-27-73		

REFERENCE DRAWINGS	
COMP ASSY: 54168100	

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR501
DWN	2-23-73
CHK	2-26-73
ENGR	2-26-73
MFG	2-23-73
APPR	2-27-73

TITLE

SCHEMATIC DIAGRAM CHANNEL I/O TRANSMITTERS TYPE 3TWV

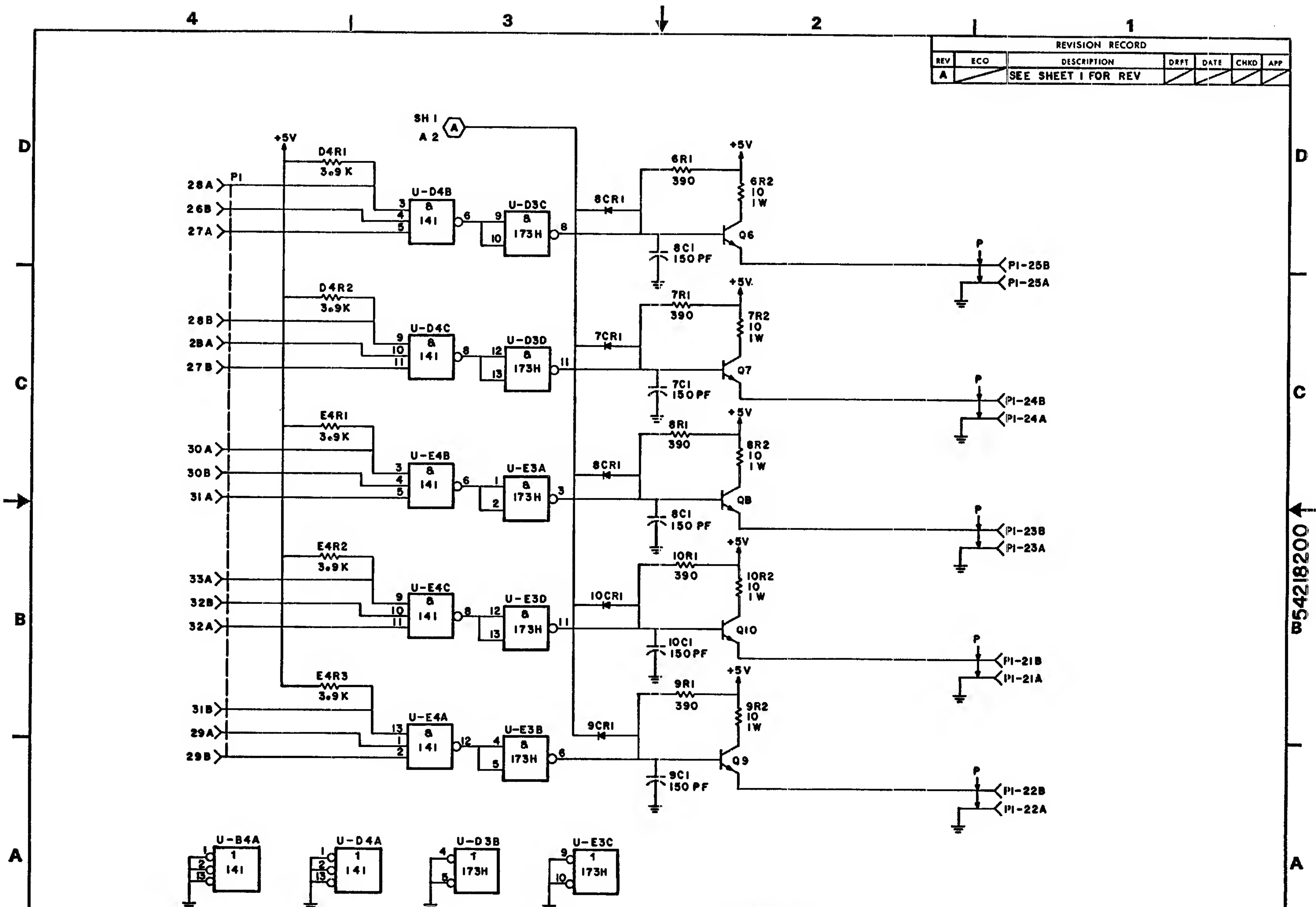
CODE IDENT		DRAWING NUMBER	CO
19333	C	54168200	1

SHEET 1 OF 2

HPD-E

54168200

70629100 E

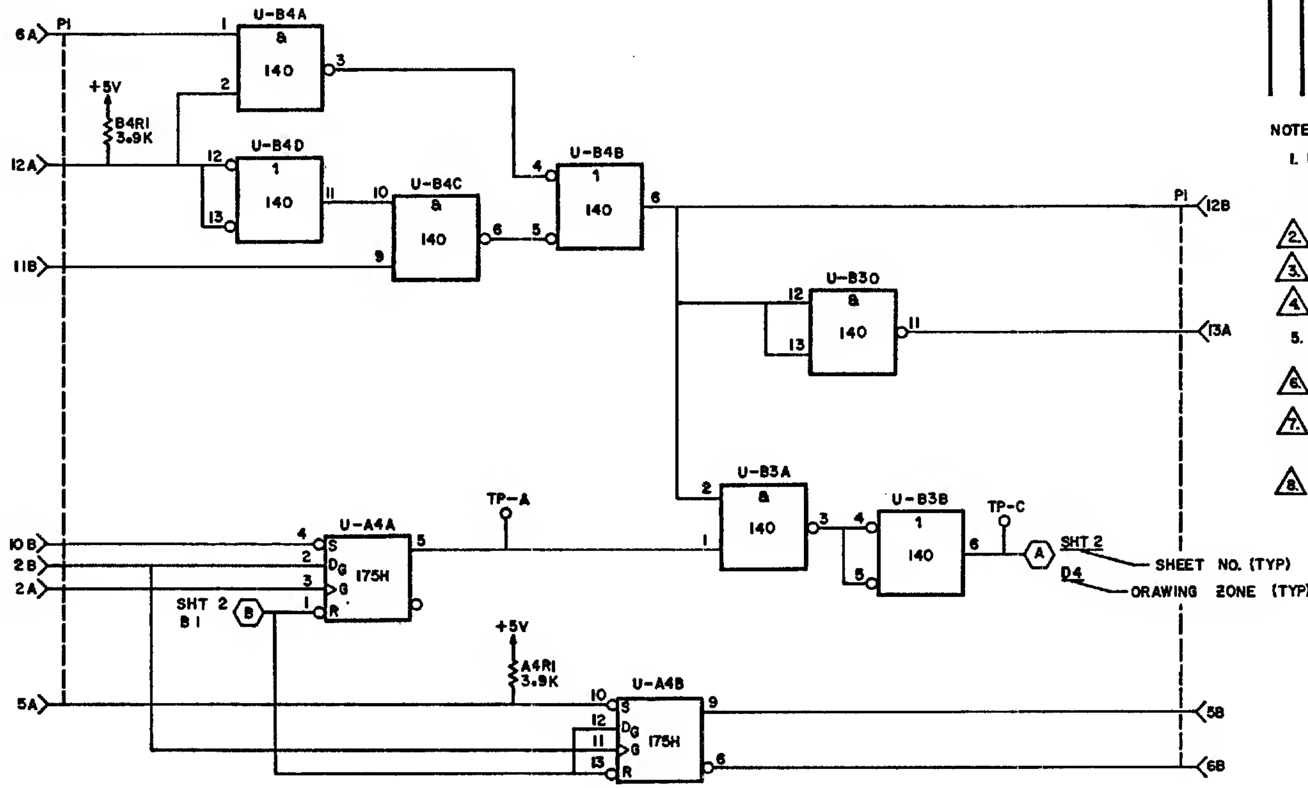


CONTROL DATA NORMANDALE DIVISION

SCHEMATIC DIAGRAM
TYPE 3TWV

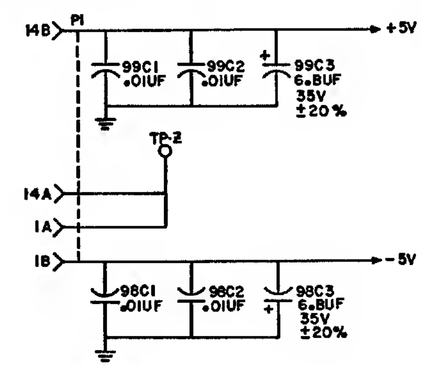
CODE IDENT		DWG NO	CD
19333	C	54168200	1
		SHEET 2	

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	#E23000	RELEASED			[illegible]	[illegible]



NOTE:

1. UNLESS OTHERWISE SPECIFIED;
   ALL TRANSISTORS, SNPN, 2N3646, 50210310
   ALL DIODES, SILICON, 92115021
2. TRANSISTOR, SPNP, 2N4916, 50211610.
3. TRANSISTOR, SNPN, 2N3568, 50210810.
4. DIODE, ZENER, 50240108.
5. ALL I.C. HAVE PIN 7 CONNECTED TO +5V, PIN 14 CONNECTED TO GRD.
6. VALUE OF A3R1 TO BE SELECTED IN PRODUCTION TO GIVE A PULSE OF 55US ± 7US AT OUTPUT PIN 3B.
7. VALUE OF 10R1 TO BE SELECTED IN PRODUCTION TO DETECT A SPEED OF 3000 R.P.M. ± 300 RPM WHEN PIN 9A IS GROUNDED.
8. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS			
COMP ASSY 54170900			
COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	±5%	1/4W	OHMS
CAP	-30V	—	—

CONTROL DATA — NORMANDALE DIVISION

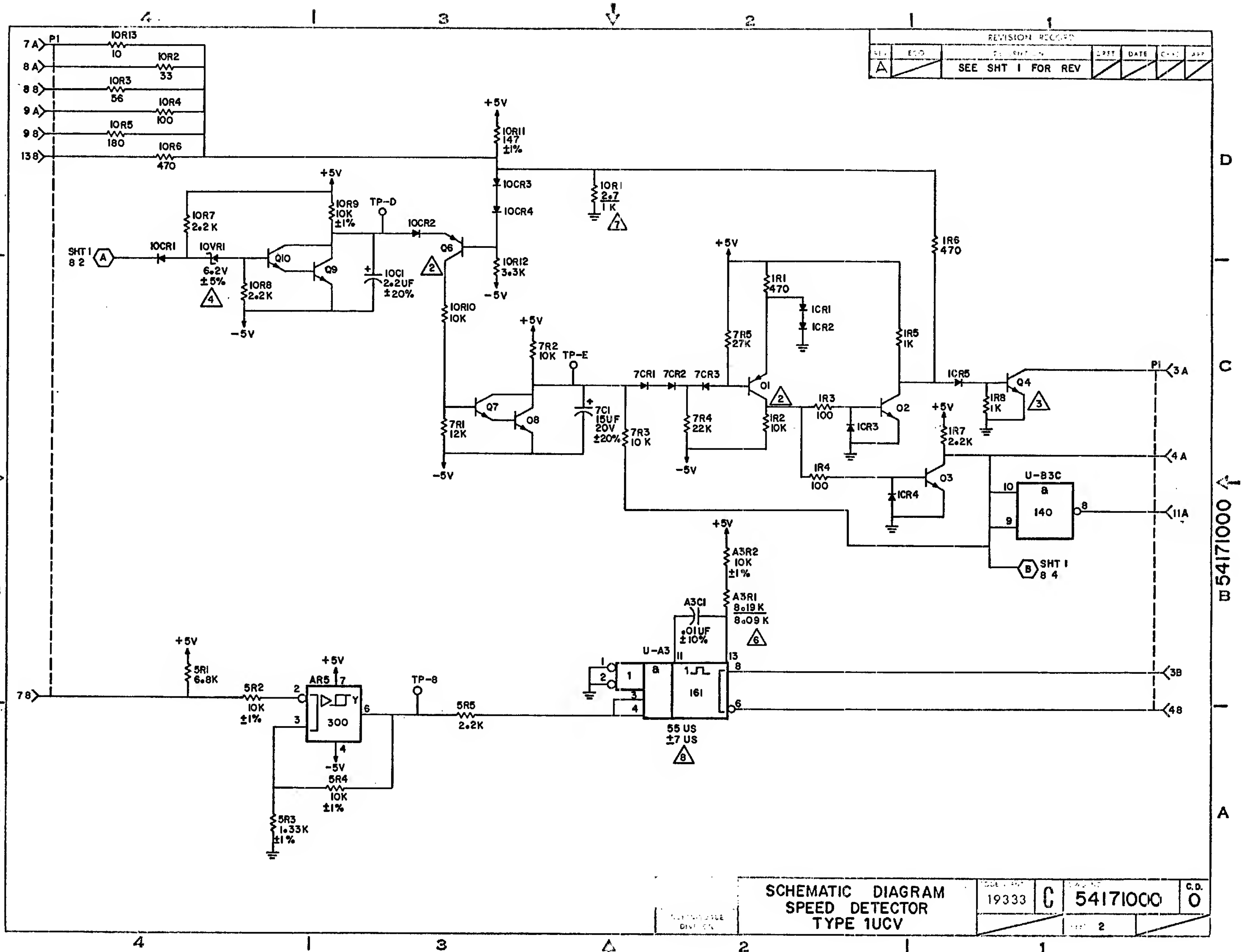
FIRST USED ON	BR301	
DWN	O. G. TUTTLE	4-22-71
CHK	H. Hanson	[illegible]
ENGR	[illegible]	[illegible]-17-71
MFG	[illegible]	[illegible]
APPR	[illegible]	[illegible]

TITLE: SCHEMATIC DIAGRAM SPEED DETECTOR TYPE 1UCV

CODE IDENT		DRAWING NUMBER	C.D.
19333	C	54171000	0

SHEET 1 OF 2

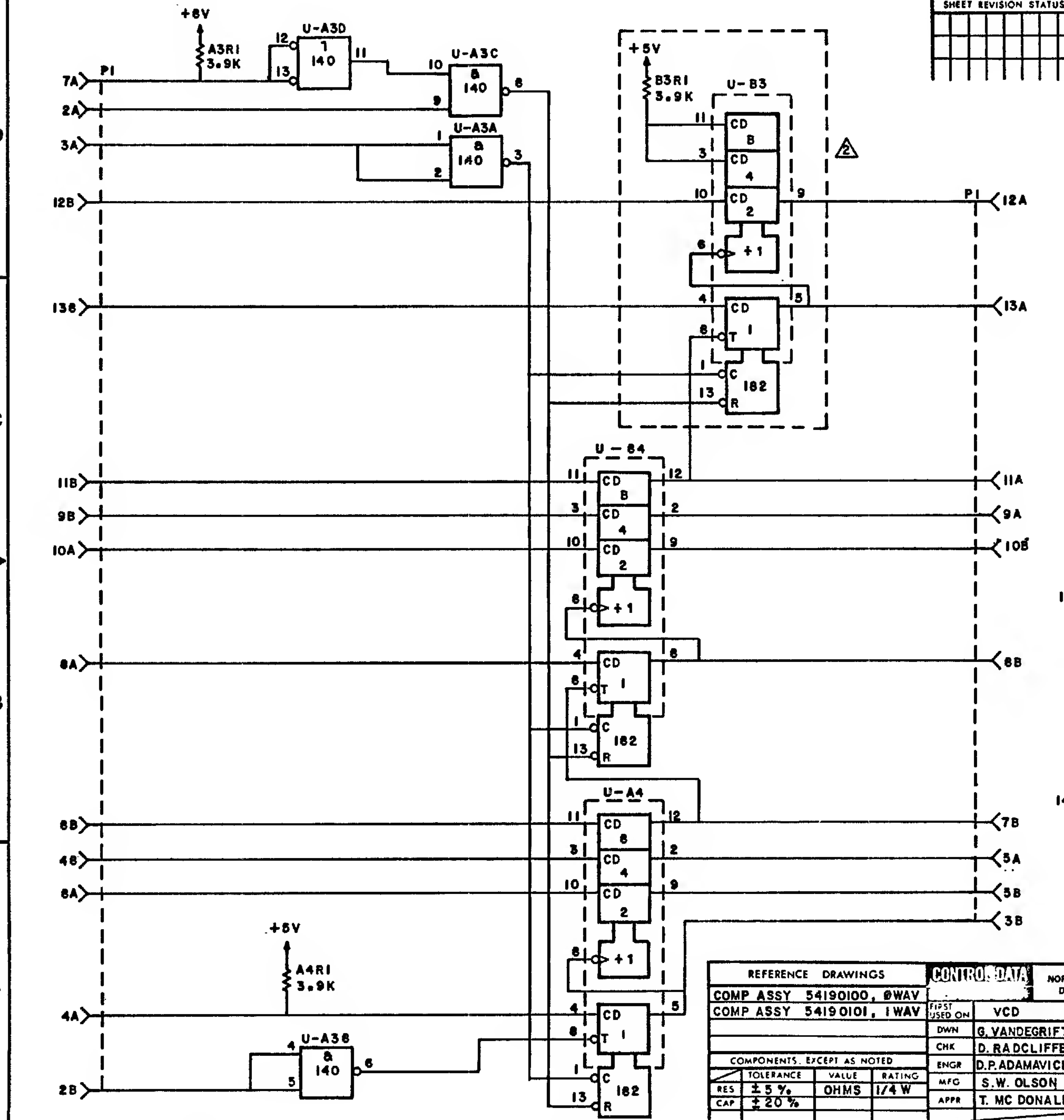
54171000


REVISION RECORD
A SEE SHT 1 FOR REV
P1 7A 8A 8B 9A 9B 13B
10R13 10 10R2 33 10R3 56 10R4 100 10R5 180 10R6 470
+5V 10R11 147 ±1%
10CR3 10CR4
10R1 2.7 1K
10R7 2.2K 10R9 10K ±1% TP-D 10CR2
SHT 1 8 2 A 10CR1 10VR1 6.2V ±5% Q10 Q9 10C1 2.2UF ±20% Q6
10R8 2.2K -5V
10R12 3.3K -5V
10R10 10K
+5V 7R2 10K TP-E
7CR1 7CR2 7CR3
Q7 Q8 7C1 15UF 20V ±20% 7R3 10K 7R4 22K
7R1 12K -5V
+5V 1R1 470 1CR1 1CR2 7R5 27K 1R5 1K 1R6 470
Q1 1R2 10K 1R3 100 1CR3 Q2
1CR5 Q4 1R8 1K P1 3A
+5V 1R7 2.2K
1R4 100 Q3 1CR4 4A
U-B3C 10 9 140 8 11A
SHT 1 8 4 B
+5V A3R2 10K ±1% A3R1 8.19K 8.09K
A3C1 .01UF ±10%
U-A3 1 2 3 4 11 13 8 6 161 55 US ±7 US 3B 4B
7B +5V 5R1 6.8K 5R2 10K ±1%
+5V AR5 2 3 7 6 4 300 Y -5V
TP-8 5R5 2.2K
5R4 10K ±1%
5R3 1.33K ±1%
SCHEMATIC DIAGRAM
SPEED DETECTOR
TYPE 1UCV
19333 C 54171000 0
SHEET 2
54171000 B

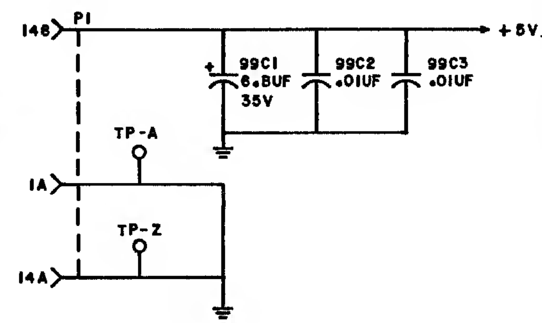
SHEET REVISION STATUS					

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				RJ
B	PE 29122	ADDED 1WAV	EMP	3-18-71	CEC	II
C	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE				III



NOTE:
1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC
2. COMPONENTS SHOWN INSIDE DOTTED LINE, USED ON ØWAV ONLY



REFERENCE DRAWINGS
COMP ASSY 54190100, ØWAV
COMP ASSY 54190101, 1WAV

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	G. VANDEGRIFT	4-15-70
CHK	D. RADCLIFFE	5-28-70
ENGR	D.P. ADAMAVICH	8-5-70
MFG	S.W. OLSON	8-26-70
APPR	T. MC DONALD	9-27-70

TITLE SCHEMATIC DIAGRAM TEN BIT COUNTER TYPE ØWAV / 1WAV

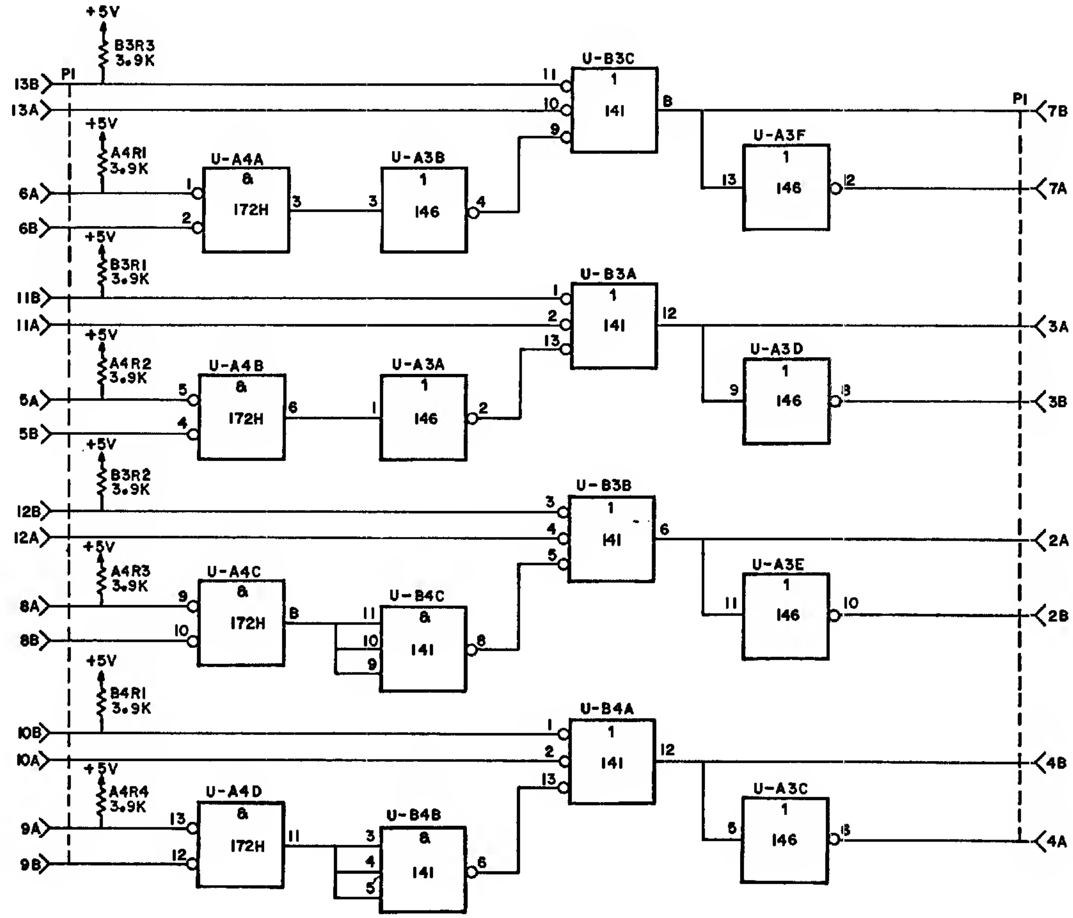
CODE IDENT 19333 | C | DRAWING NUMBER 54190200 | CD 3

SHEET 1 OF 1

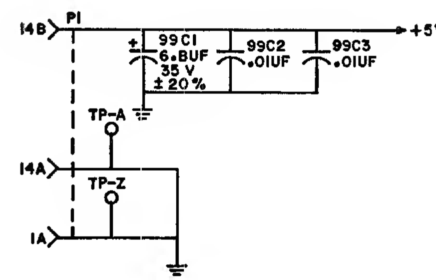
54190200

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	[illegible]	RELEASED			[illegible]	[illegible]



NOTE:
1. ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.



54190601

REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION
COMPONENT ASS'Y 54190501	FIRST USED ON	BR301
	DWN	R. BOCHE 4-19-71
	CHK	H. [illegible] 5-27-71
	ENGR	[illegible] 5-27-71
	MFG	[illegible] -15-71
	APPR	[illegible] 6-11-71

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

TITLE: SCHEMATIC DIAGRAM 4-BIT INPUT STEERING TYPE 1WBV

CODE IDENT 19333 | C | DRAWING NUMBER 54190601 | C.D. 2

SHEET 1 OF 1

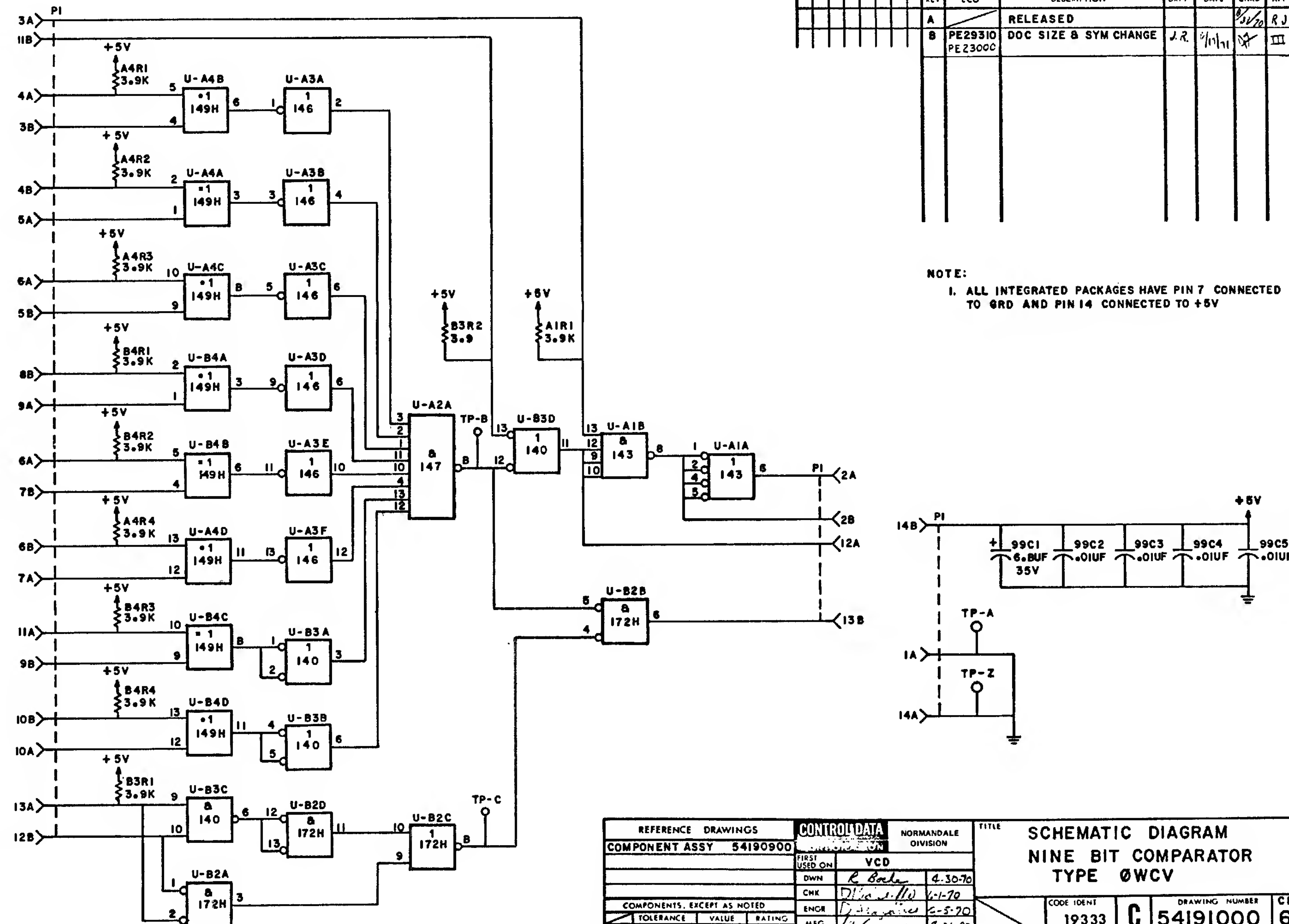
SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED			8/31/70	RJ
B	PE29310 PE23000	DOC SIZE & SYM CHANGE	J.R.	5/11/71		III

NOTE:

1. ALL INTEGRATED PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V



REFERENCE DRAWINGS	
COMPONENT ASSY	54190900

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD
DWN	R. Boele 4-30-70
CHK	1-1-70
ENGR	6-5-70
MFG	7-21-70
APPR	7-27-70

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

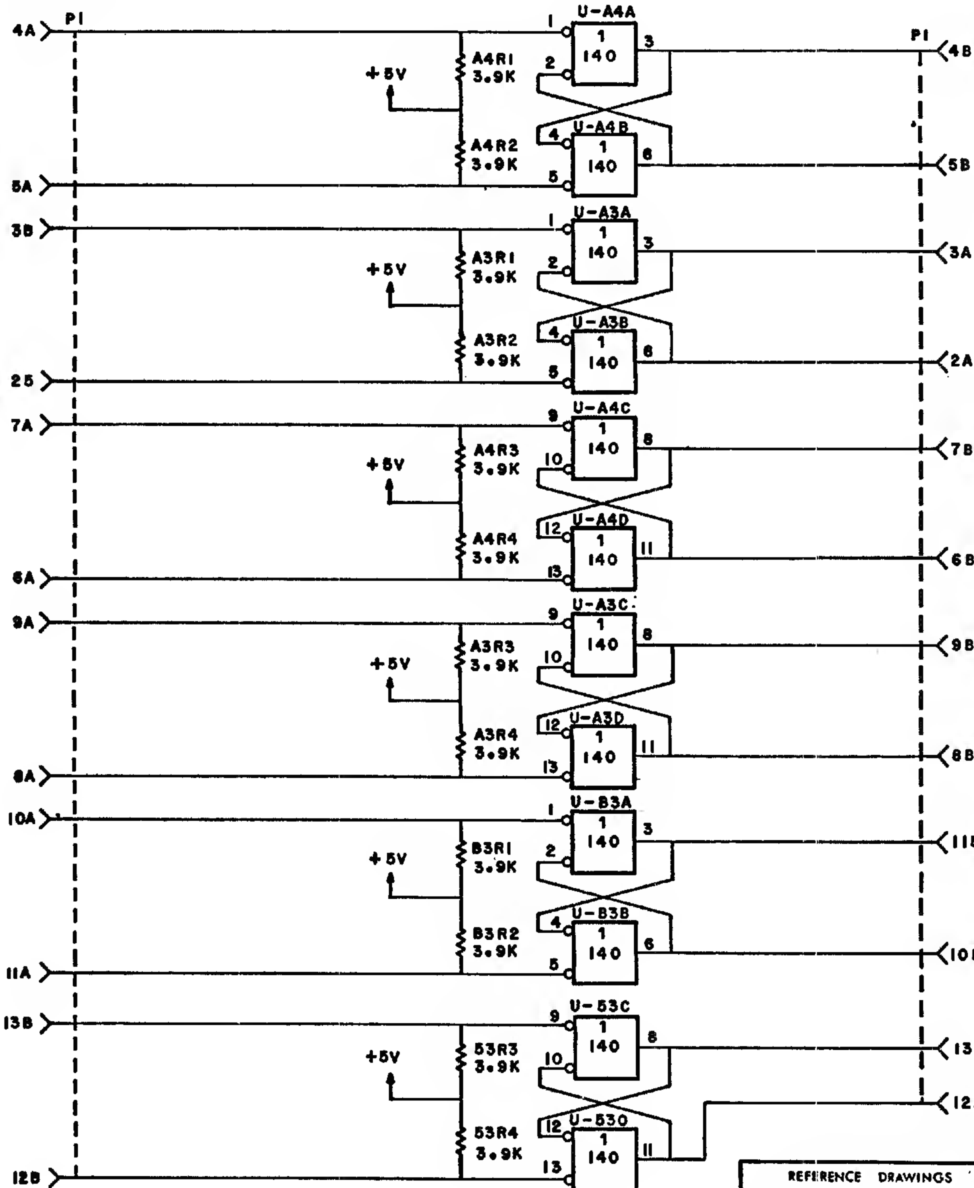
TITLE: SCHEMATIC DIAGRAM NINE BIT COMPARATOR TYPE ØWCV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54191000	6

SHEET 1 OF 1

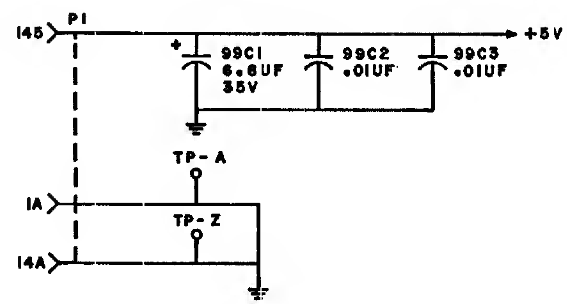
54191000

SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				RJ
B	PE29310 PE23000	DOC SIZE & SYMBOL CHANGE	J.R.	4/17/71		III



NOTE:

1. ALL INTEGRATED PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V



REFERENCE DRAWINGS	
COMP ASSY	54191300

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5 %	OHMS	1/4 W
CAP	±20 %		

CONTROL DATA NORMANDALE DIVISION

FIRST USED ON	VCO	
DWN	J. E. MATTSON	4-8-70
CHK	R. BOCHE	6-5-70
ENGR	D.P. ADAMAVICH	8-5-70
MFG	S.W. OLSON	8-26-70
APPR	T. MC DONALD	8-27-70

TITLE

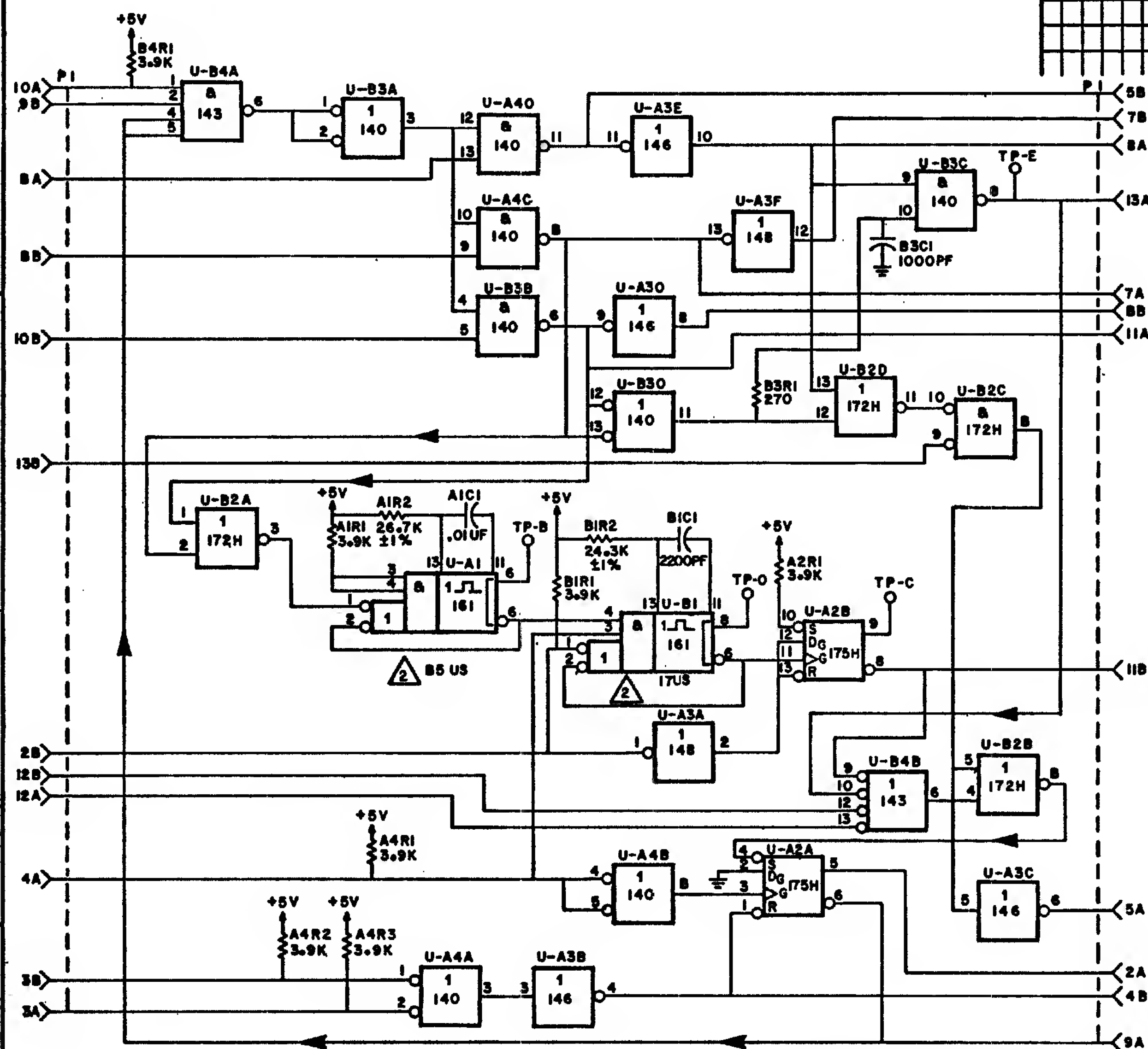
SCHEMATIC DIAGRAM FAULT REGISTER TYPE ØWDV

CODE IDENT		DRAWING NUMBER	CD
19333	C	54191400	8

SHEET 1 OF 1

54191400

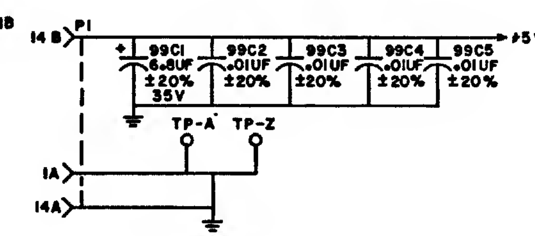
SHEET REVISION STATUS	REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	FE23000	RELEASED		5-9-72		



NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2 DELAY TIME FOR REF ONLY.



REFERENCE DRAWINGS	
COMP ASSY	54191710

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	8R301	
DWN	R. BOCHE	4-14-72
CHK		4-19-72
ENGR		4-19-72
MFG		5-2-72
APPR		4-21-72

TITLE
SCHEMATIC DIAGRAM
R/W/E ENABLE & FAULT DETECT
TYPE GWEV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54191810	8

SHEET 1 OF 1

HPD

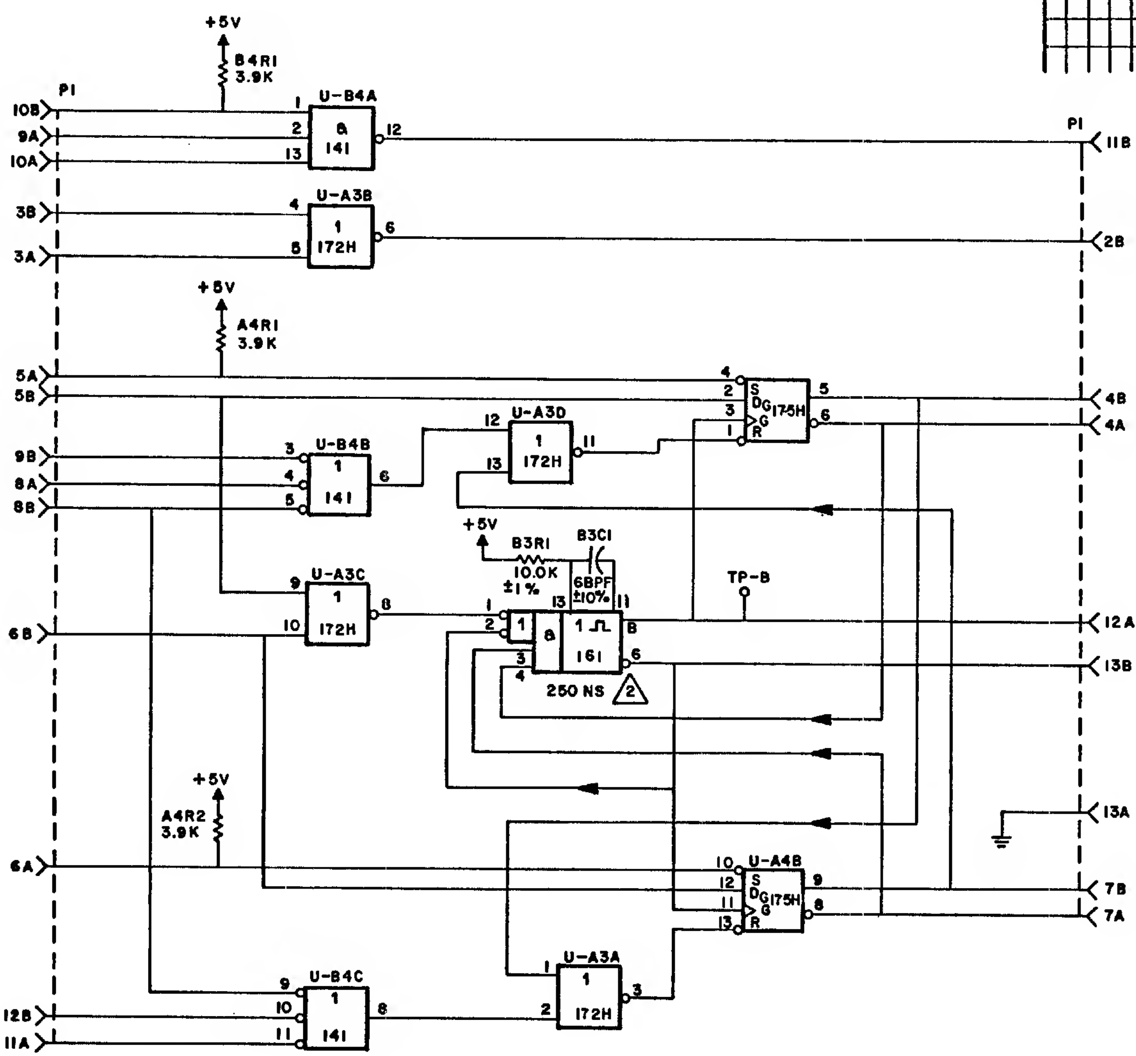
54191810

70629100 E

SHEET REVISION STATUS							

REVISION RECORD

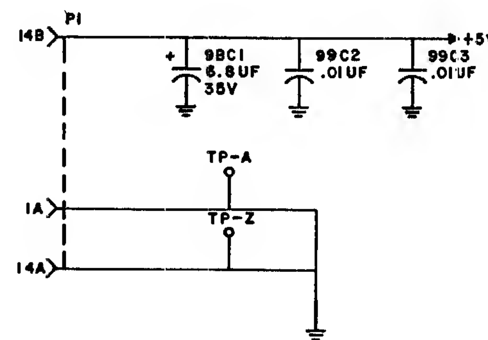
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				RJ
B	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE	JR	4/11/71		



NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V

2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS
COMPONENT ASSY 54192500

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	± 20%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	VCD	
DWN	G. VANDEGRIFT	4·14·70
CHK	D. RADCLIFFE	5·27·70
ENGR	D.P. ADAMAVICH	8·21·70
MFG	S.W. OLSON	9·3·70
APPR	T. MCDONALD	9·27·70

TITLE

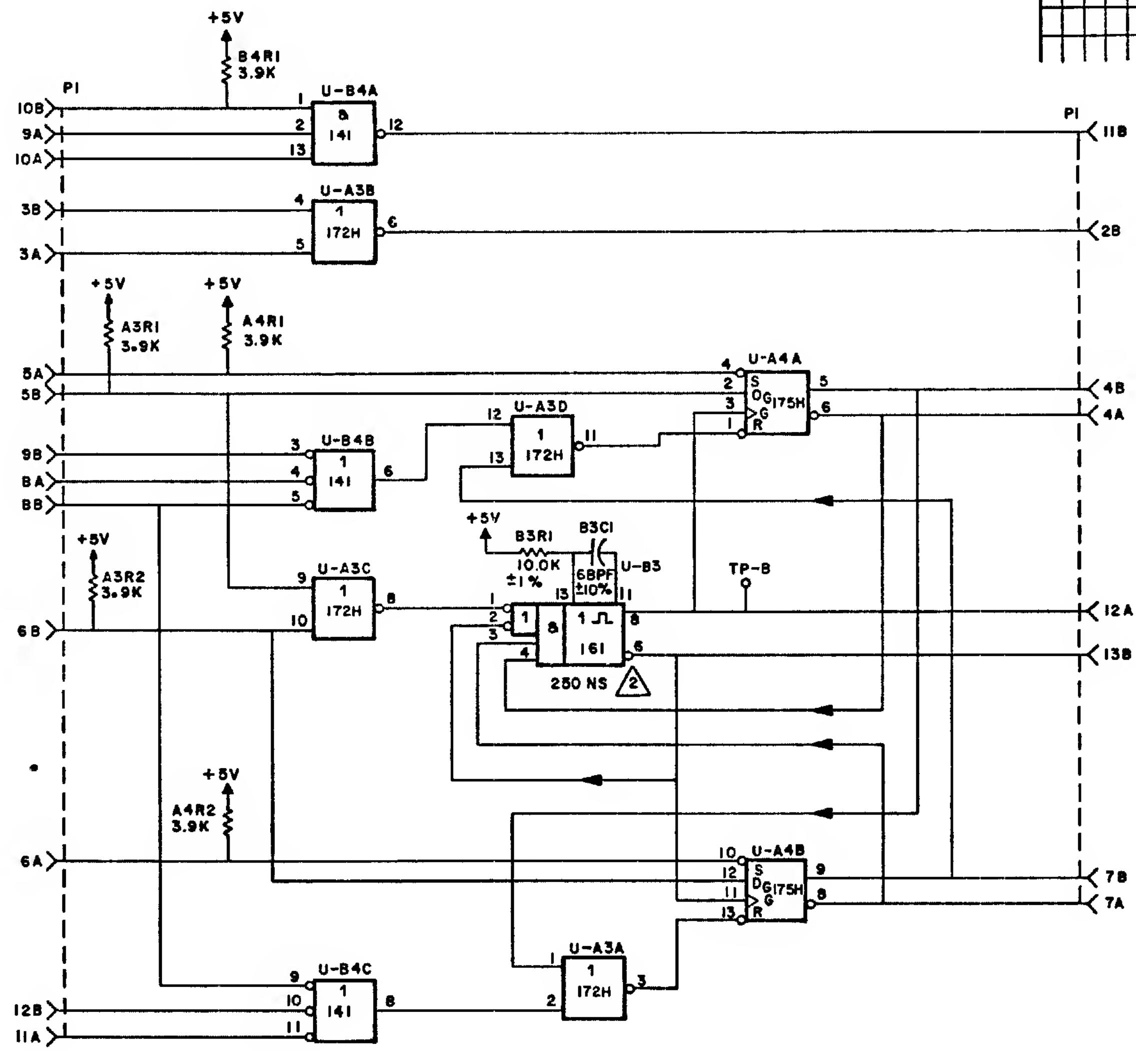
SCHEMATIC DIAGRAM UNIT RESERVE TYPE ØWGV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54192600	2

SHEET 1 OF 1

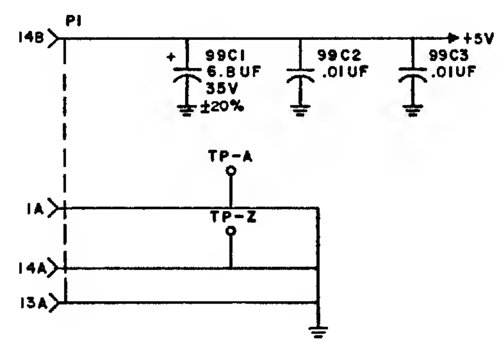
54192600

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	323000	RELEASED		2-3-71		RH



NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS			
COMPONENT ASSY 54192501			
COMPONENTS EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES	± 5%	OHMS	1/4 W
CAP	-30%		

	NORMANDALE DIVISION	
CN	BR3A3	
DWN	Q. MARTIN	11-8-71
CHK		11-19-71
ENGR		11-22-71
MFG		
APPR		

TITLE
SCHEMATIC DIAGRAM UNIT RESERVE TYPE 1WGV

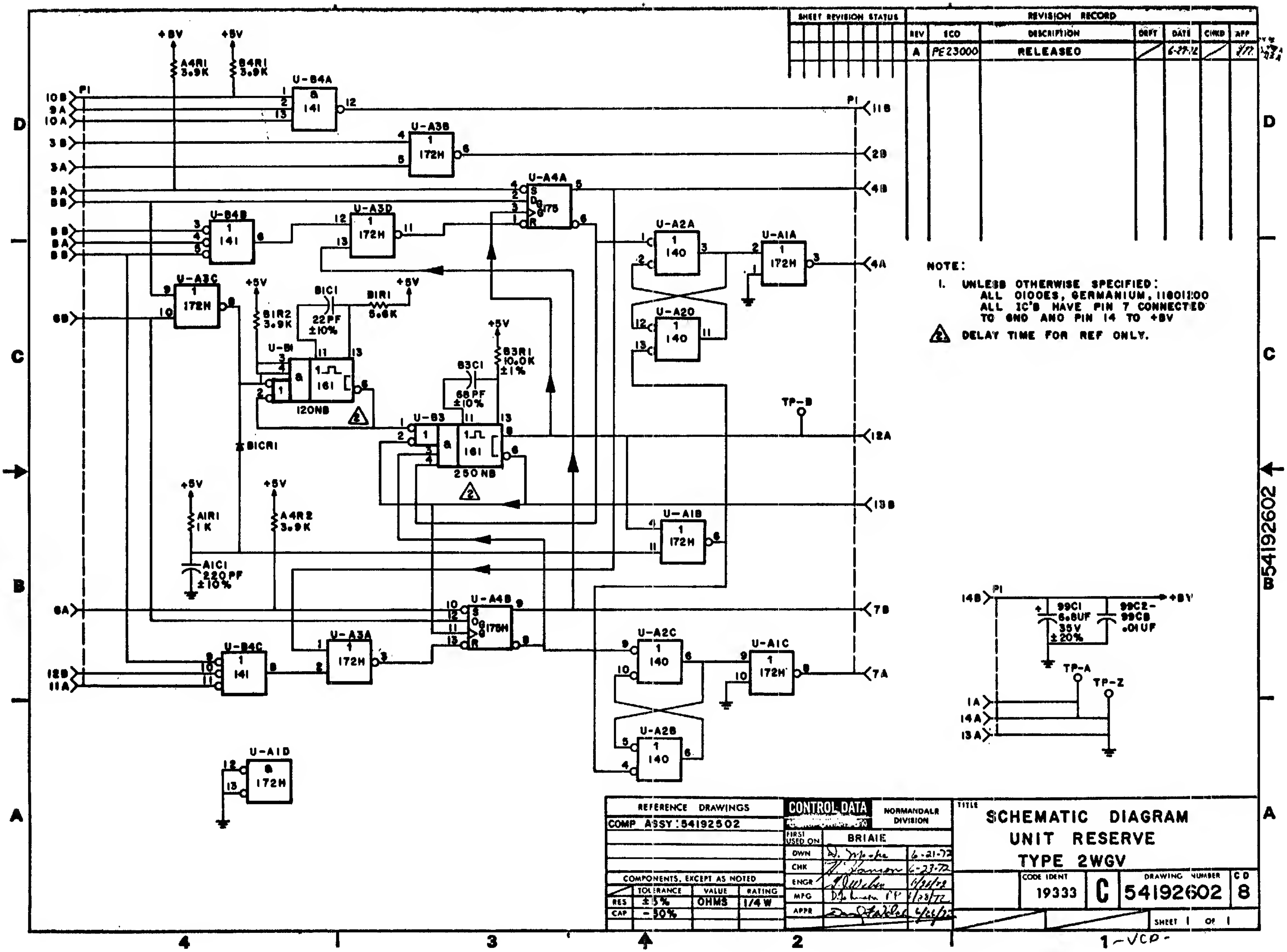
CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54192601	O

SHEET 1 OF 1

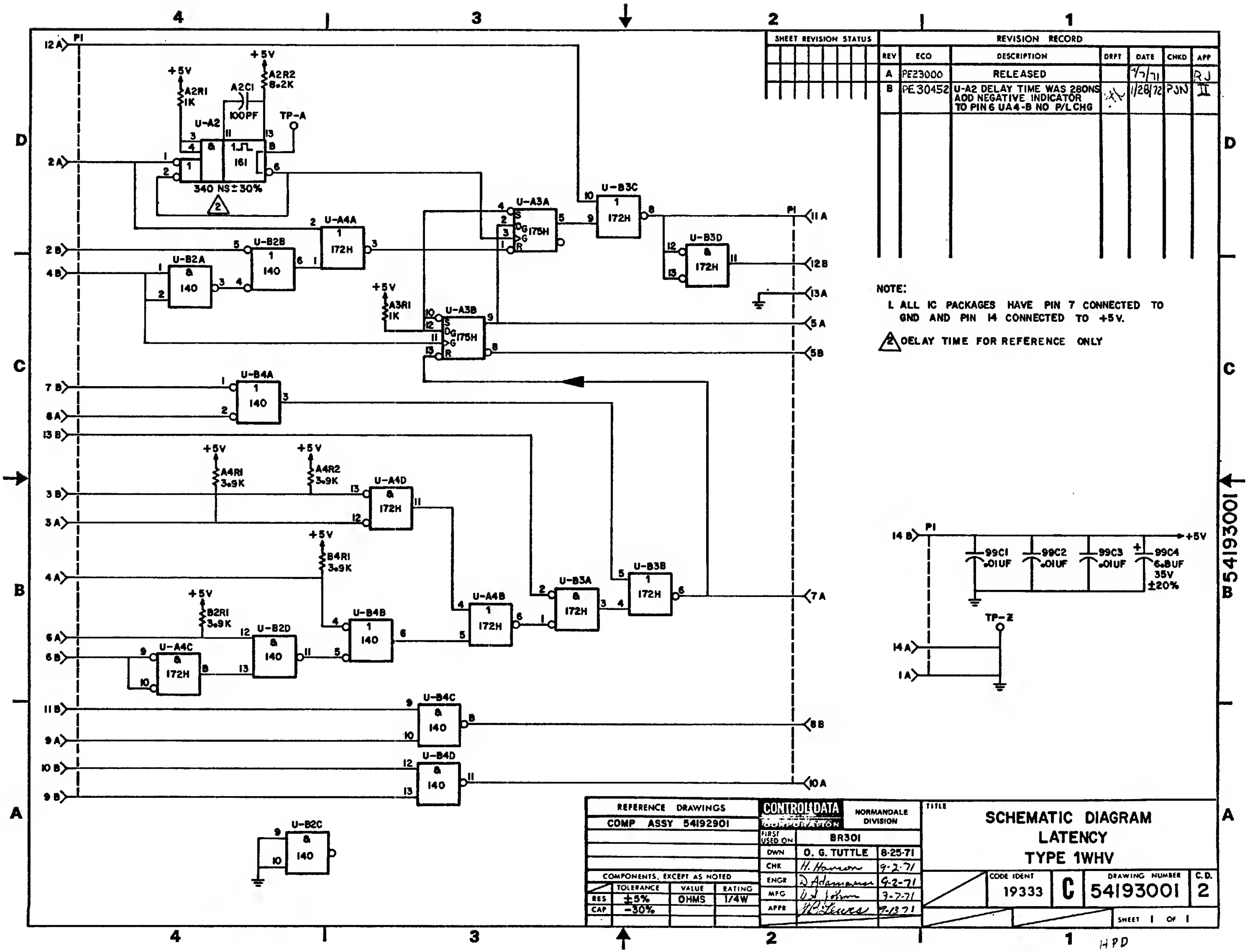
54192601

70629100 E

70629100 E

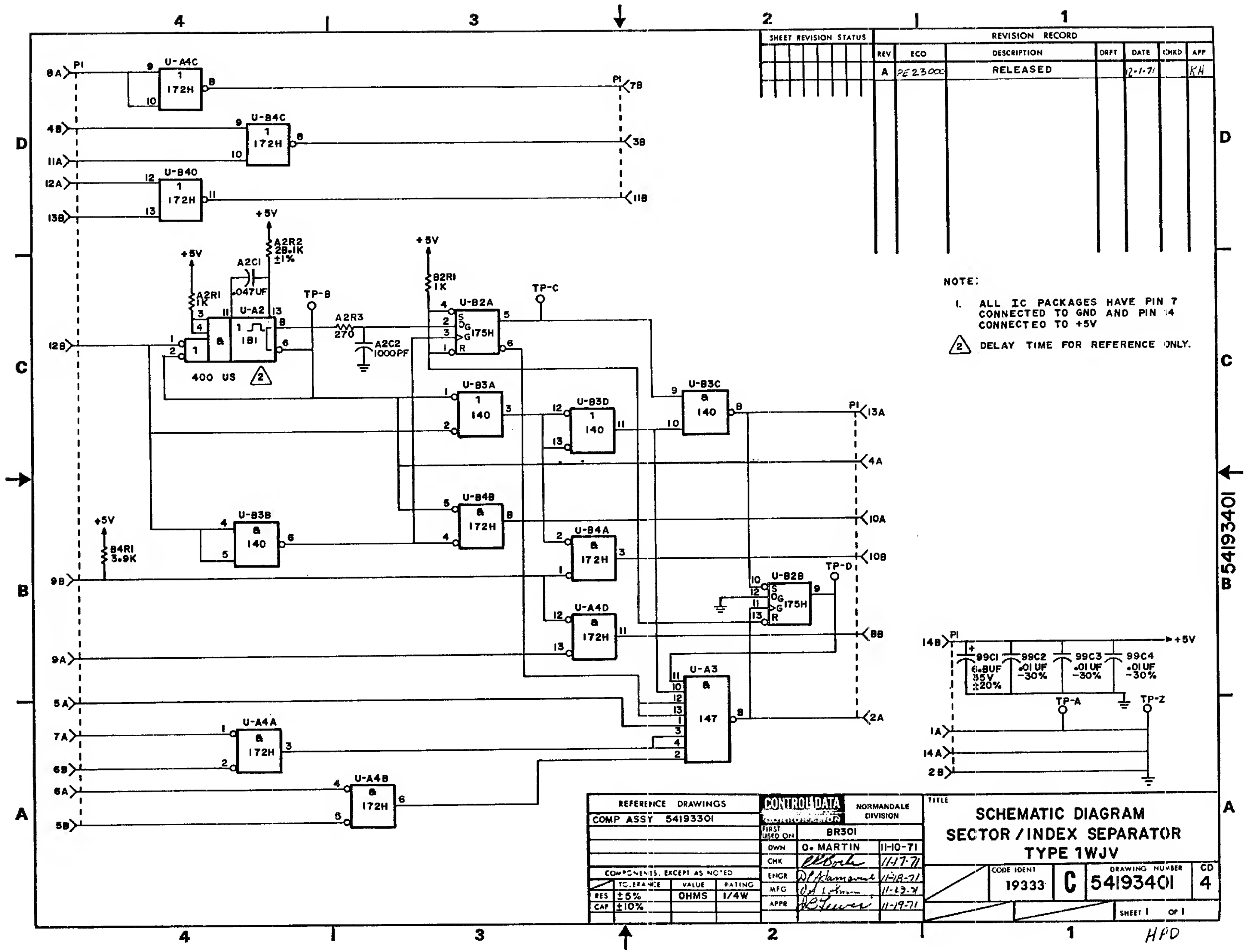

REVISION RECORD
REV | ECO | DESCRIPTION | DATE
A | PE23000 | RELEASED | 6-27-72
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL DIODES, GERMANIUM, 11801200
ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V
2 DELAY TIME FOR REF ONLY.
REFERENCE DRAWINGS
COMP ASSY: 54192502
CONTROL DATA
NORMANDALE DIVISION
FIRST USED ON BRIAIE
COMPONENTS, EXCEPT AS NOTED
TOLERANCE VALUE RATING
RES ±5% OHMS 1/4 W
CAP -30%
SCHEMATIC DIAGRAM
UNIT RESERVE
TYPE 2WGV
CODE IDENT 19333
C
DRAWING NUMBER 54192602
8
SHEET 1 OF 1
54192602

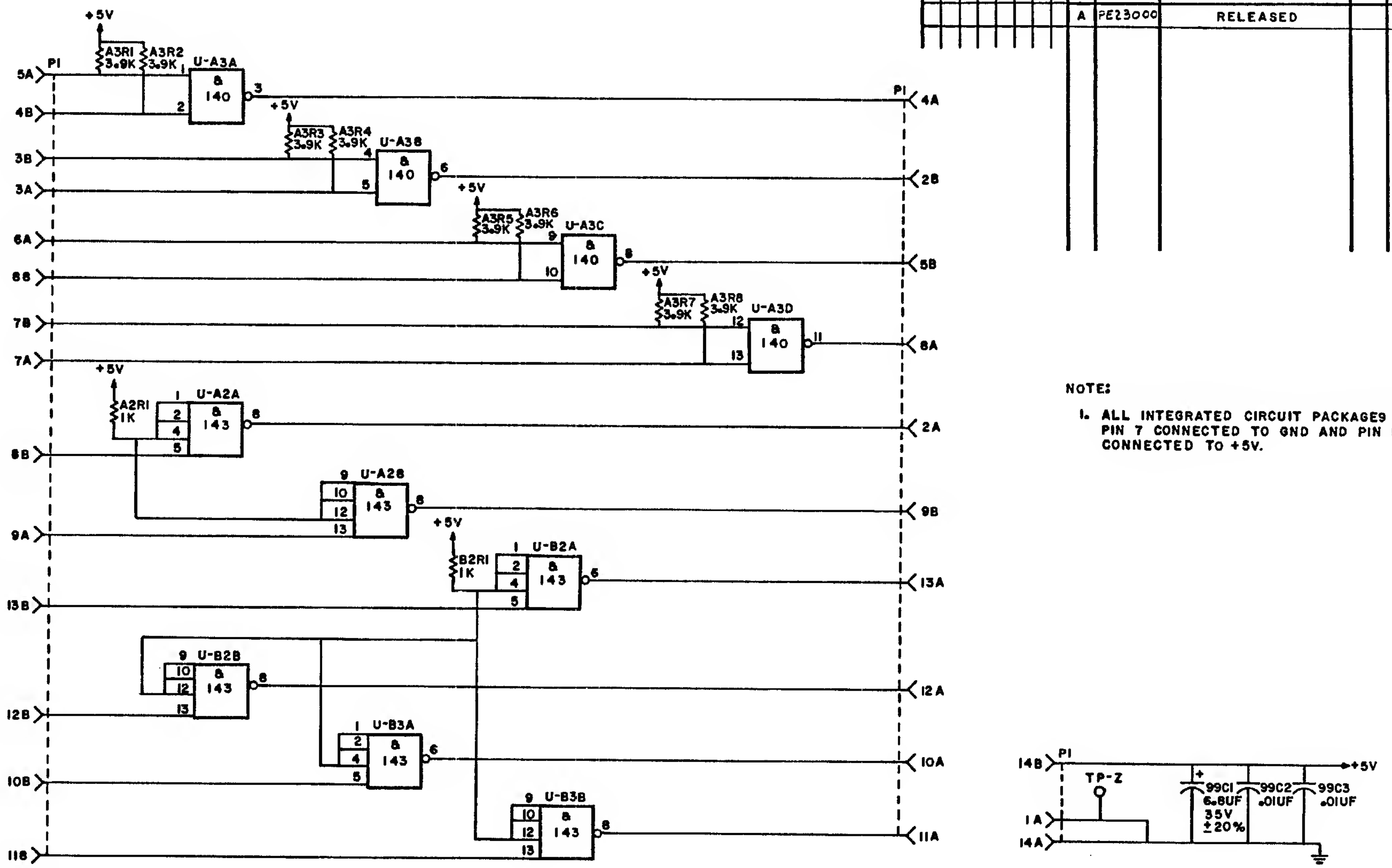
4-220



70629100 E

70629100 E


REVISION RECORD
SHEET REVISION STATUS
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE 23000 | RELEASED | | 12-1-71 | | KH
NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
2 DELAY TIME FOR REFERENCE ONLY.
U-A4C 172H
U-B4C 172H
U-B4D 172H
U-A2 181
400 US
A2R1 1K
A2C1 .047UF
A2R2 28.1K ±1%
A2R3 270
A2C2 1000PF
TP-B
TP-C
TP-D
TP-A
TP-Z
U-B2A 175H
B2R1 1K
U-B3A 140
U-B3D 140
U-B3C 140
U-B3B 140
U-B4B 172H
U-B4A 172H
U-B2B 175H
U-A4D 172H
U-A3 147
U-A4A 172H
U-A4B 172H
B4R1 3.9K
+5V
99C1 6.8UF 35V ±20%
99C2 .01 UF -30%
99C3 .01 UF -30%
99C4 .01 UF -30%
REFERENCE DRAWINGS
COMP ASSY 54193301
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% | OHMS | 1/4W
CAP ±10%
CONTROL DATA CORPORATION
NORMANDALE DIVISION
FIRST USED ON BR301
DWN O. MARTIN 11-10-71
CHK 11-17-71
ENGR 11-18-71
MFG 11-19-71
APPR 11-19-71
TITLE
SCHEMATIC DIAGRAM
SECTOR / INDEX SEPARATOR
TYPE 1WJV
CODE IDENT 19333
C
DRAWING NUMBER 54193401
CD 4
SHEET 1 OF 1
54193401
HPD



NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED				

REFERENCE DRAWINGS
COMPONENT ASSY 54194500

COMPONENTS, EXCEPT AS NOTED

	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA CORPORATION — NORMANDALE DIVISION

FIRST USED ON	BR301	
DWN	Q. MARTIN	6-22-71
CHK		7-1-71
ENGR		7-1-71
MFG		7-9-71
APPR		7-9-71

TITLE

SCHEMATIC DIAGRAM BUFFER TYPE 1WMV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54194600	0

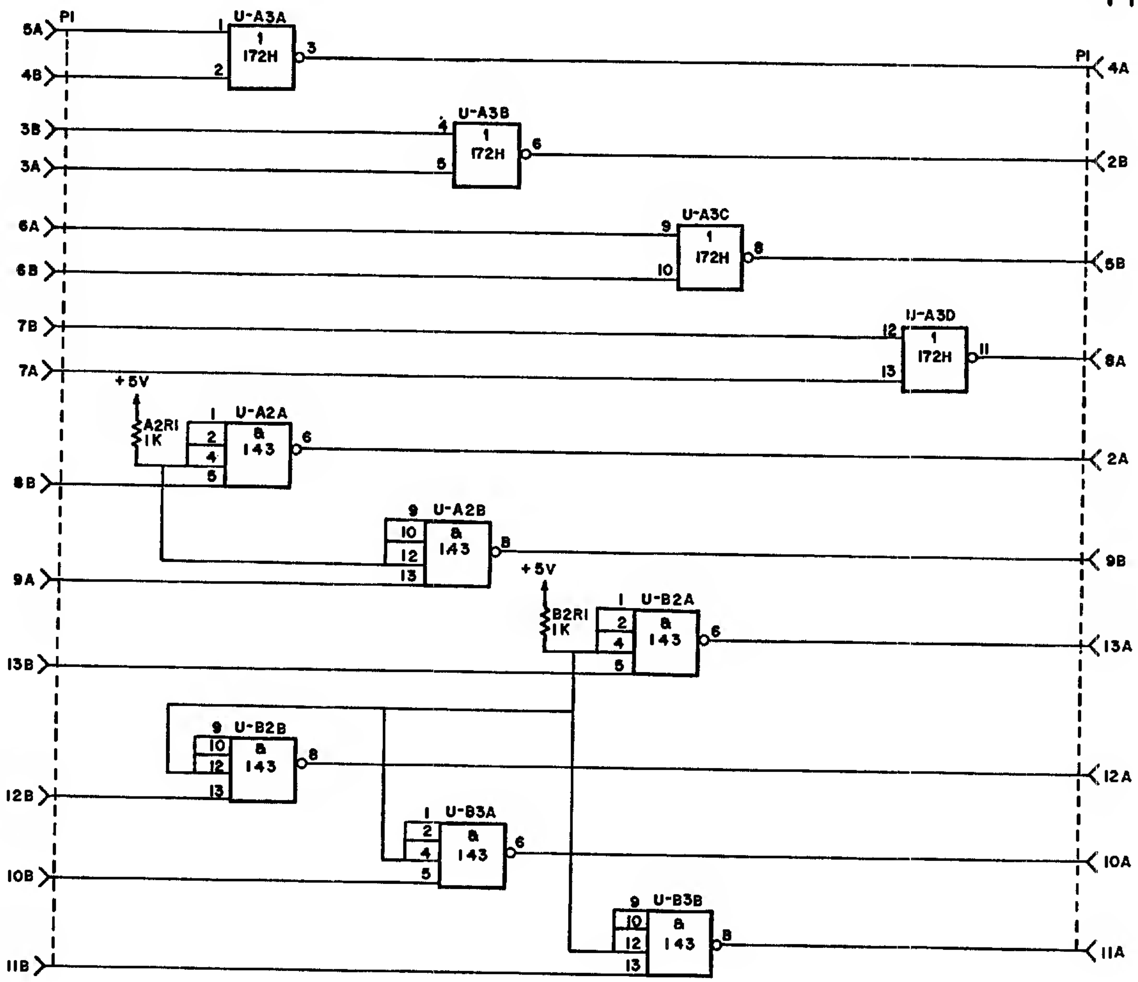
SHEET 1 OF 1

HPD

54194600

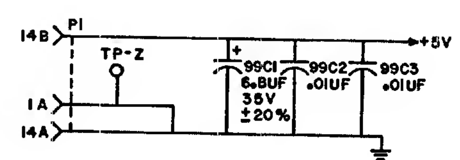
70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	PE 23000	RELEASED		11/17/71		RH



NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS	
COMPONENT ASSY 54194501	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4W
CAP	-30%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON	BR301	
DWN	R. BOCHE	11-1-71
CHK	H. Hanson	11-2-71
ENGR	[illegible]	11-3-71
MFG	[illegible]	11-12-71
APPR	[illegible]	11-4-71

TITLE

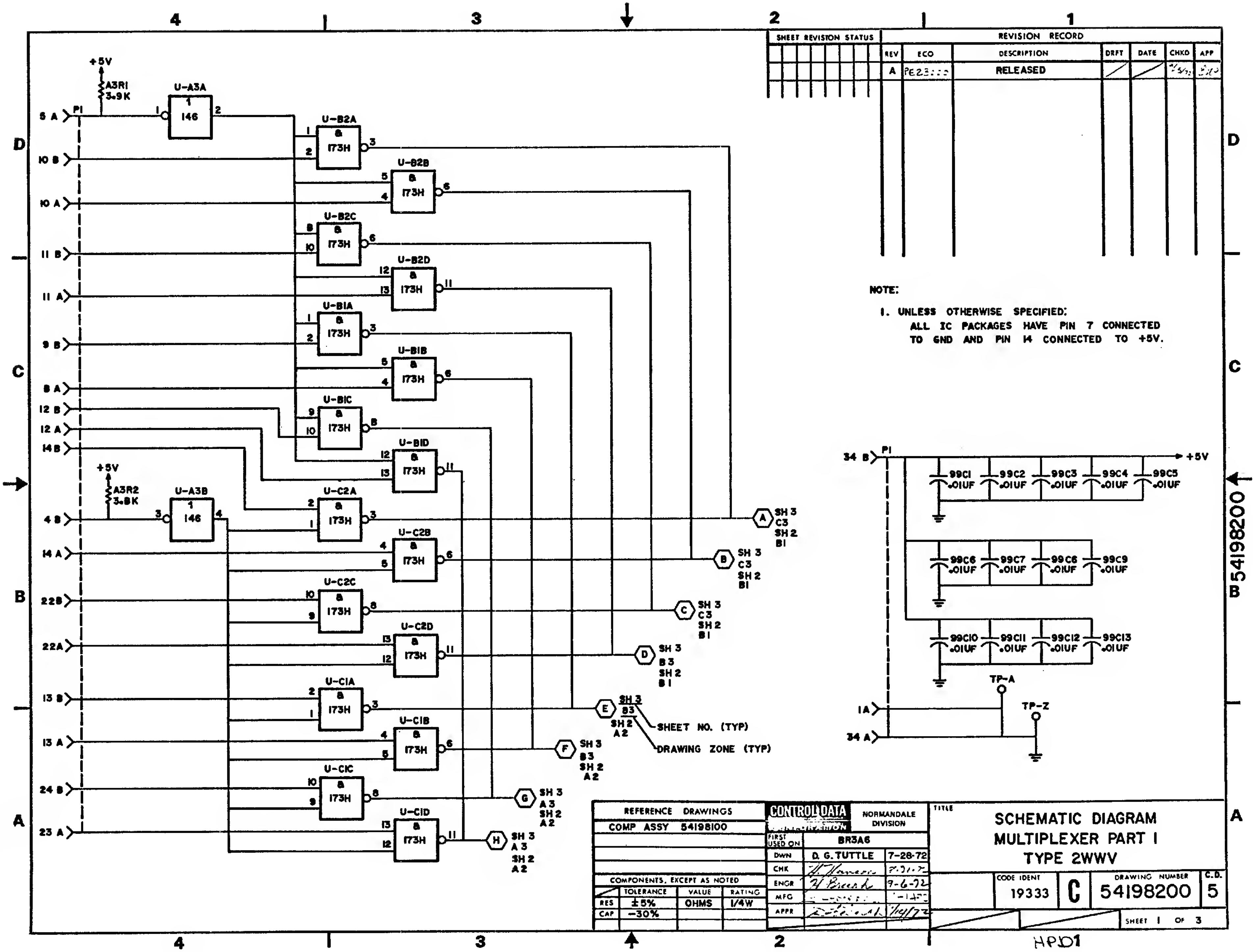
SCHEMATIC DIAGRAM BUFFER TYPE AWMV

CODE IDENT 19333 | SIZE C | DRAWING NUMBER 54194601 | CD 8

SHEET 1 OF 1

54194601

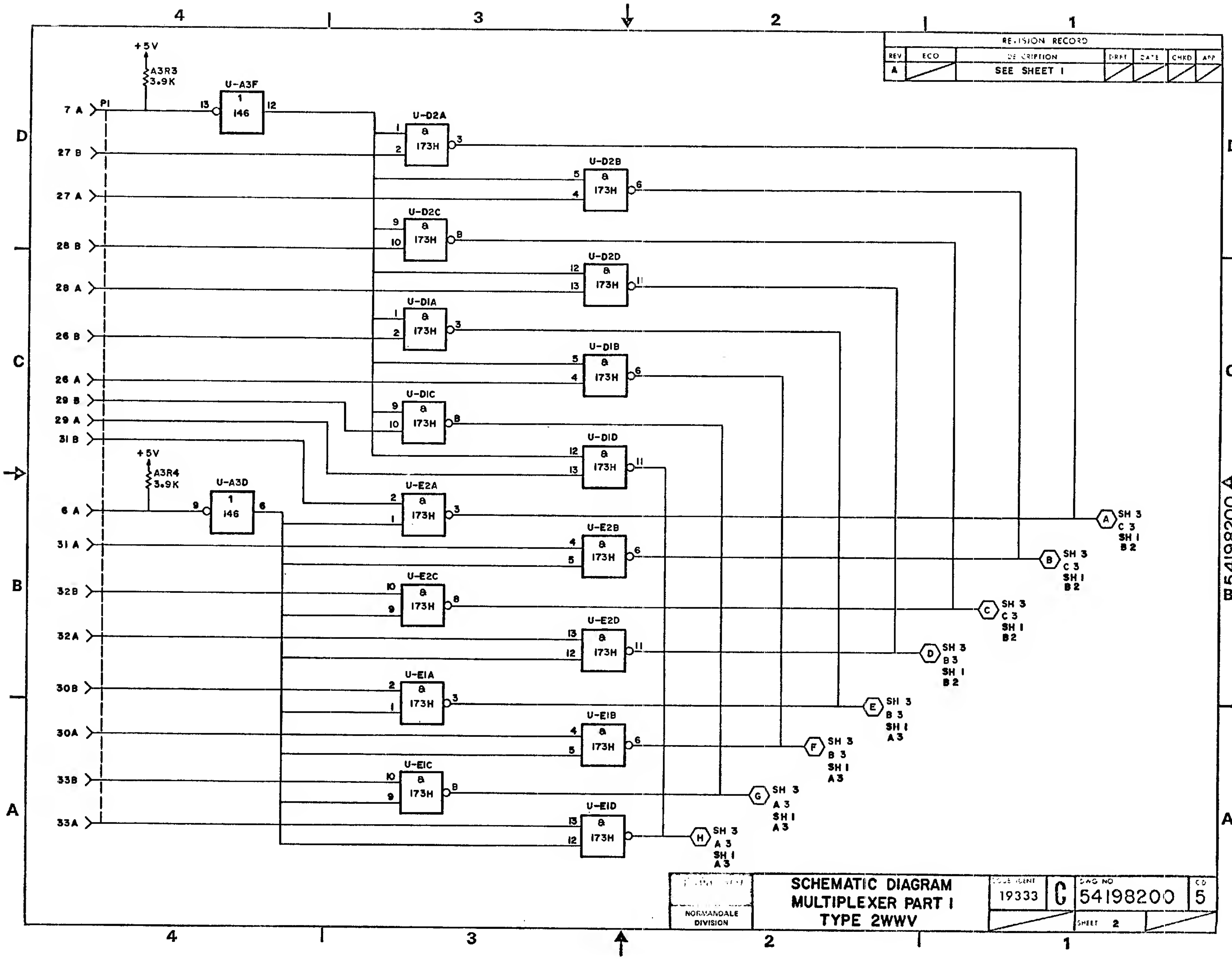
HPD

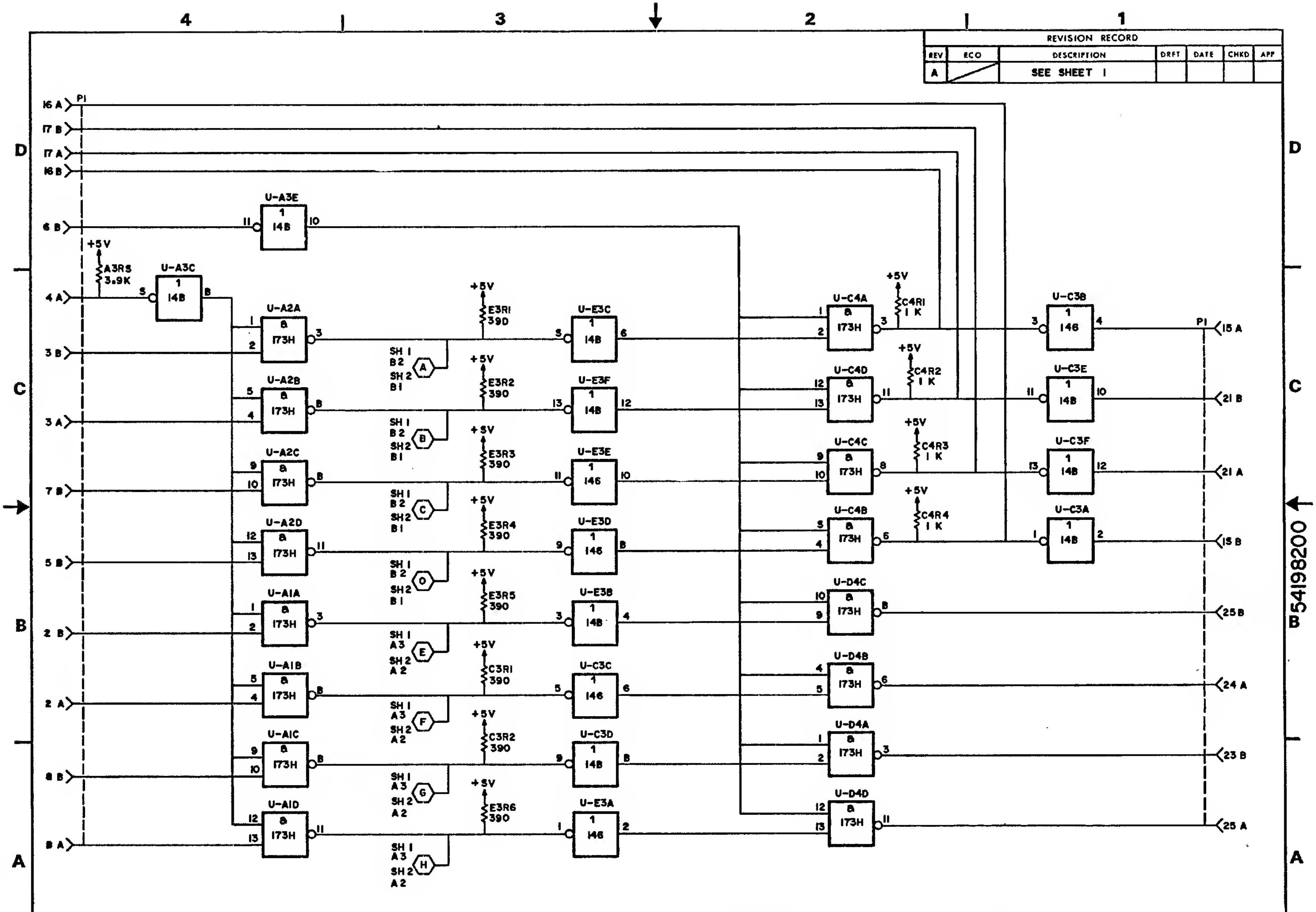


SHEET REVISION STATUS
REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | PE23 | RELEASED
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
+5V
A3R1 3.9K
A3R2 3.9K
U-A3A 146
U-A3B 146
U-B2A 173H
U-B2B 173H
U-B2C 173H
U-B2D 173H
U-B1A 173H
U-B1B 173H
U-B1C 173H
U-B1D 173H
U-C2A 173H
U-C2B 173H
U-C2C 173H
U-C2D 173H
U-C1A 173H
U-C1B 173H
U-C1C 173H
U-C1D 173H
P1
9 A
10 B
10 A
11 B
11 A
9 B
8 A
12 B
12 A
14 B
4 B
14 A
22B
22A
13 B
13 A
24 B
23 A
A SH 3 C3 SH 2 B1
B SH 3 C3 SH 2 B1
C SH 3 C3 SH 2 B1
D SH 3 B3 SH 2 B1
E SH 3 B3 SH 2 A2
SHEET NO. (TYP)
DRAWING ZONE (TYP)
F SH 3 B3 SH 2 A2
G SH 3 A3 SH 2 A2
H SH 3 A3 SH 2 A2
34 B
+5V
99C1 .01UF
99C2 .01UF
99C3 .01UF
99C4 .01UF
99C5 .01UF
99C6 .01UF
99C7 .01UF
99C8 .01UF
99C9 .01UF
99C10 .01UF
99C11 .01UF
99C12 .01UF
99C13 .01UF
TP-A
TP-Z
1A
34 A
REFERENCE DRAWINGS
COMP ASSY 54198100
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% OHMS 1/4W
CAP -30%
CONTROL DATA CORPORATION
NORMANDALE DIVISION
FIRST USED ON BR3A6
DWN D. G. TUTTLE 7-28-72
CHK
ENGR 9-6-72
MFG
APPR
TITLE
SCHEMATIC DIAGRAM
MULTIPLEXER PART I
TYPE 2WWV
CODE IDENT 19333
C
DRAWING NUMBER 54198200
C.D. 5
SHEET 1 OF 3
HPD1
54198200

70629100 E

70629100 E


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | SEE SHEET 1
+5V
A3R3 3.9K
P1
7 A
27 B
27 A
28 B
28 A
26 B
26 A
29 B
29 A
31 B
+5V
A3R4 3.9K
6 A
31 A
32B
32A
30B
30A
33B
33A
U-A3F 1 146
U-A3D 1 146
U-D2A & 173H
U-D2B & 173H
U-D2C & 173H
U-D2D & 173H
U-D1A & 173H
U-D1B & 173H
U-D1C & 173H
U-D1D & 173H
U-E2A & 173H
U-E2B & 173H
U-E2C & 173H
U-E2D & 173H
U-E1A & 173H
U-E1B & 173H
U-E1C & 173H
U-E1D & 173H
A SH 3 C 3 SH 1 B 2
B SH 3 C 3 SH 1 B 2
C SH 3 C 3 SH 1 B 2
D SH 3 B 3 SH 1 B 2
E SH 3 B 3 SH 1 A 3
F SH 3 B 3 SH 1 A 3
G SH 3 A 3 SH 1 A 3
H SH 3 A 3 SH 1 A 3
54198200 A
NORMANDALE DIVISION
SCHEMATIC DIAGRAM
MULTIPLEXER PART I
TYPE 2WWV
19333
C
DWG NO 54198200
5
SHEET 2



REVISION RECORD

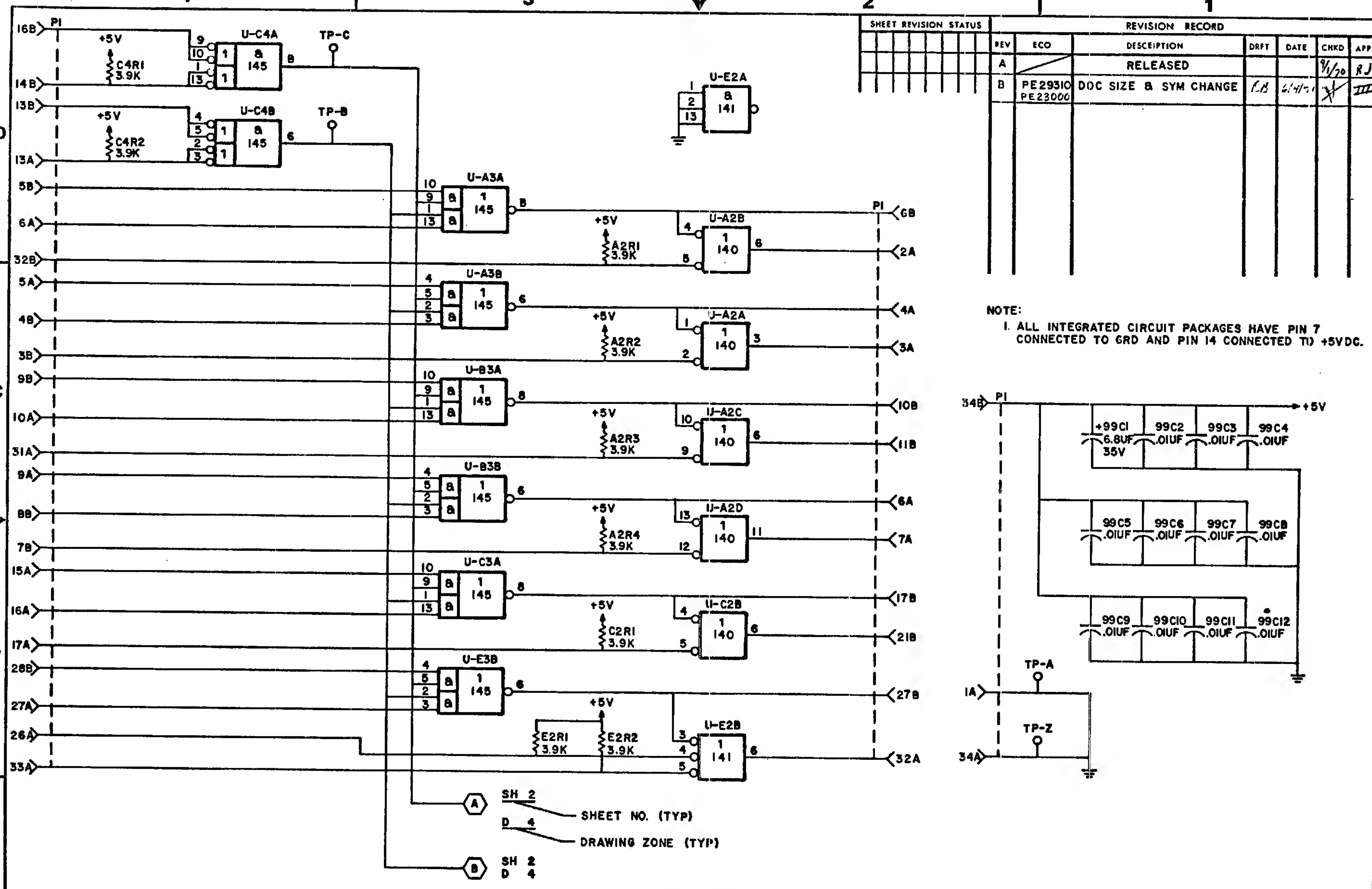
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
MULTIPLEXER PART I
TYPE 2WWV

CODE IDENT		DWG NO	CD
19333	C	54198200	5
		SHEET 3	

70629100 E



REFERENCE DRAWINGS
COMPONENT ASSEMBLY 54198900

COMPONENTS EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±20%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: VCD

DWN / CHK / ENGR / MFG / APPR

TITLE: SCHEMATIC DIAGRAM COUNTER CONTROL TYPE ØWYV

CODE IDENT	SIZE	DRAWING NUMBER	CD
19333	C	54199000	8

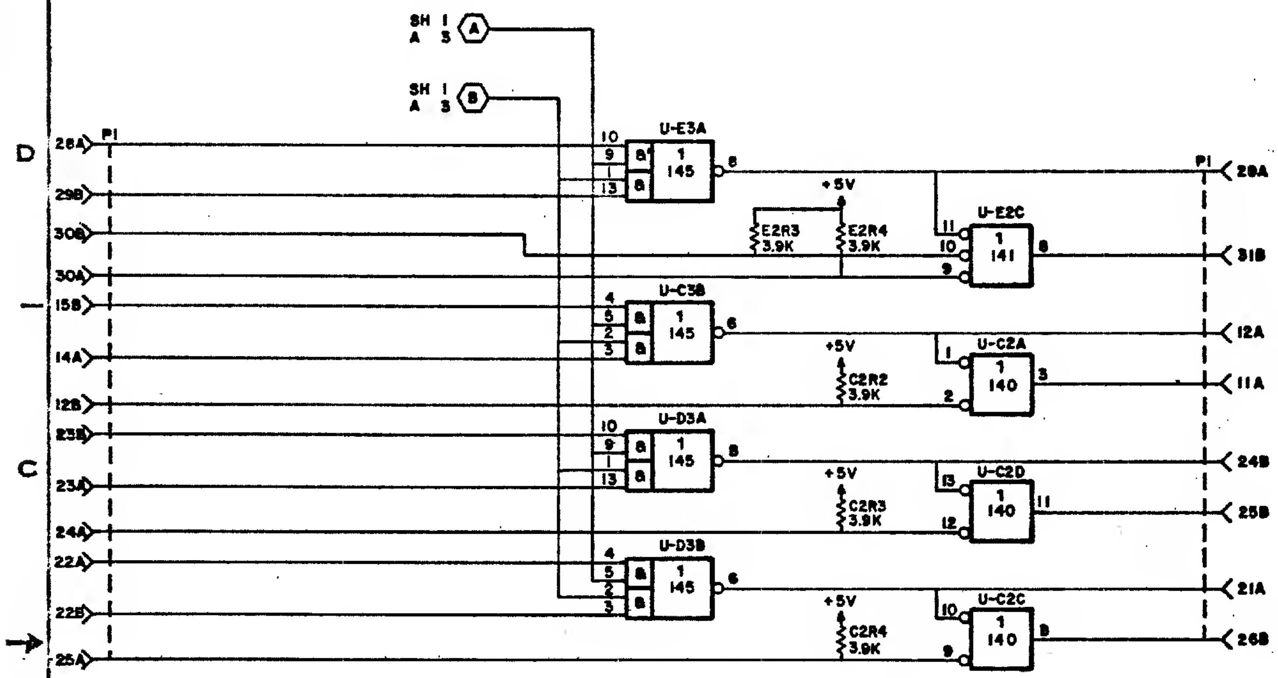
SHEET 1 OF 2

54199000 B

4-227

4-228

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APP
B		SEE SHT 1 FOR REVISION				



SCHEMATIC DIAGRAM
COUNTER CONTROL
TYPE ØWYV

54199000 CD 8

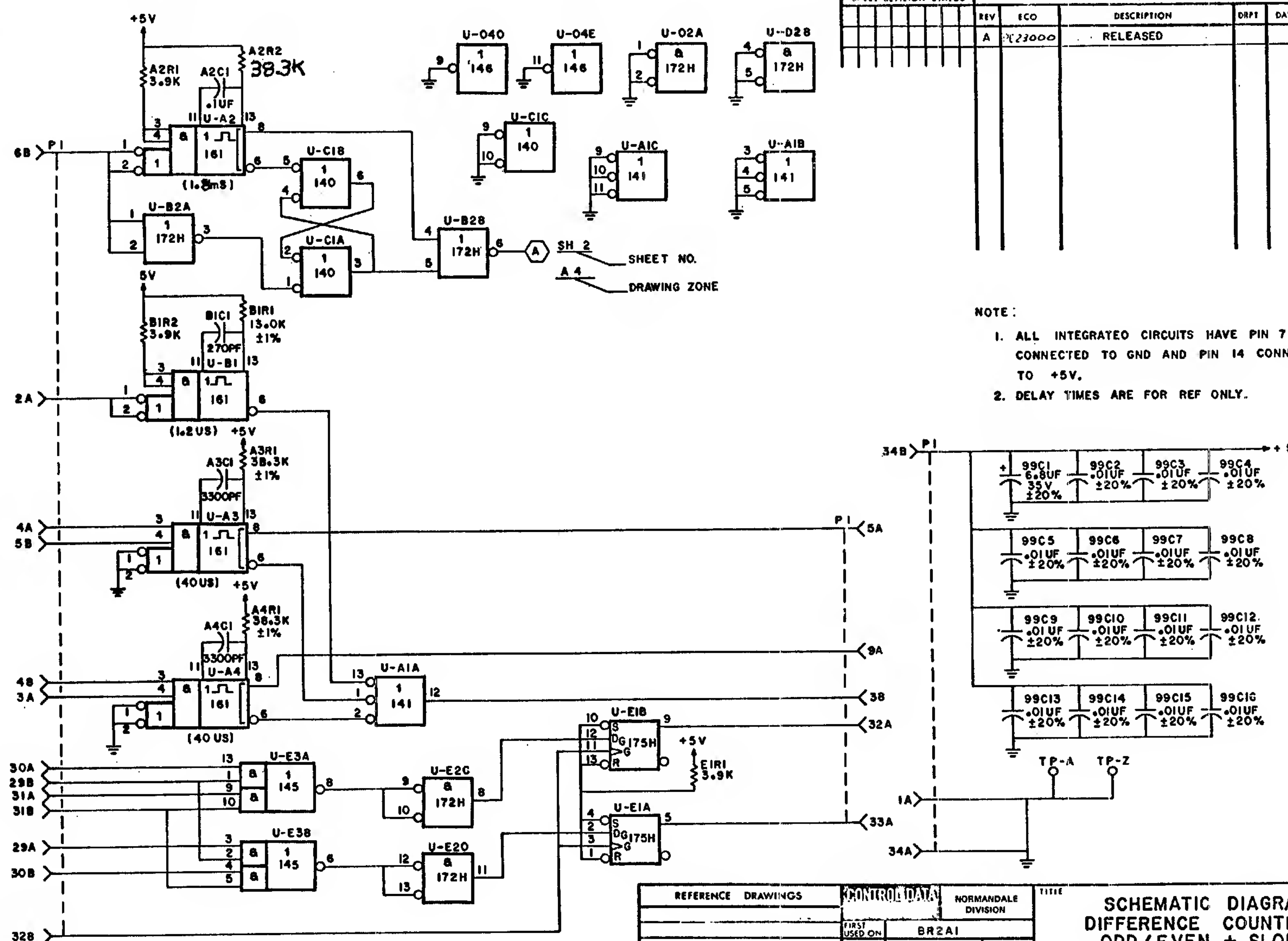
2

B54199000

70629100 E

70629100 E

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	P(23000	RELEASED				



NOTE:

1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIMES ARE FOR REF ONLY.

REFERENCE DRAWINGS

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		

CONTROL DATA — NORMANDALE DIVISION

FIRST USED ON: BR2A1

DWN: V STREETER

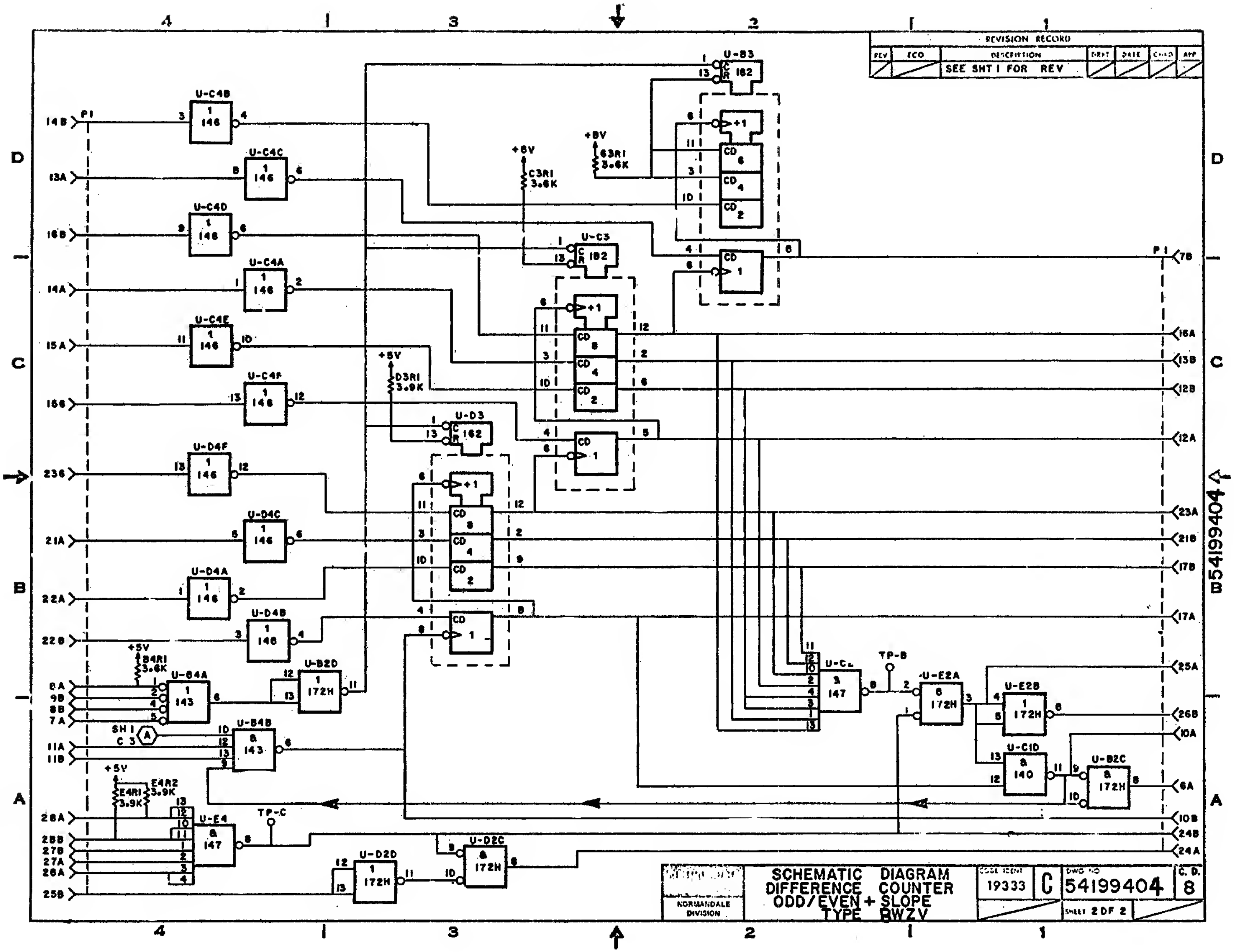
TITLE: SCHEMATIC DIAGRAM DIFFERENCE COUNTER ODD/EVEN + SLOPE TYPE BWZV

CODE IDENT 19333 | C | DRAWING NUMBER 54199404 | C.O. 8

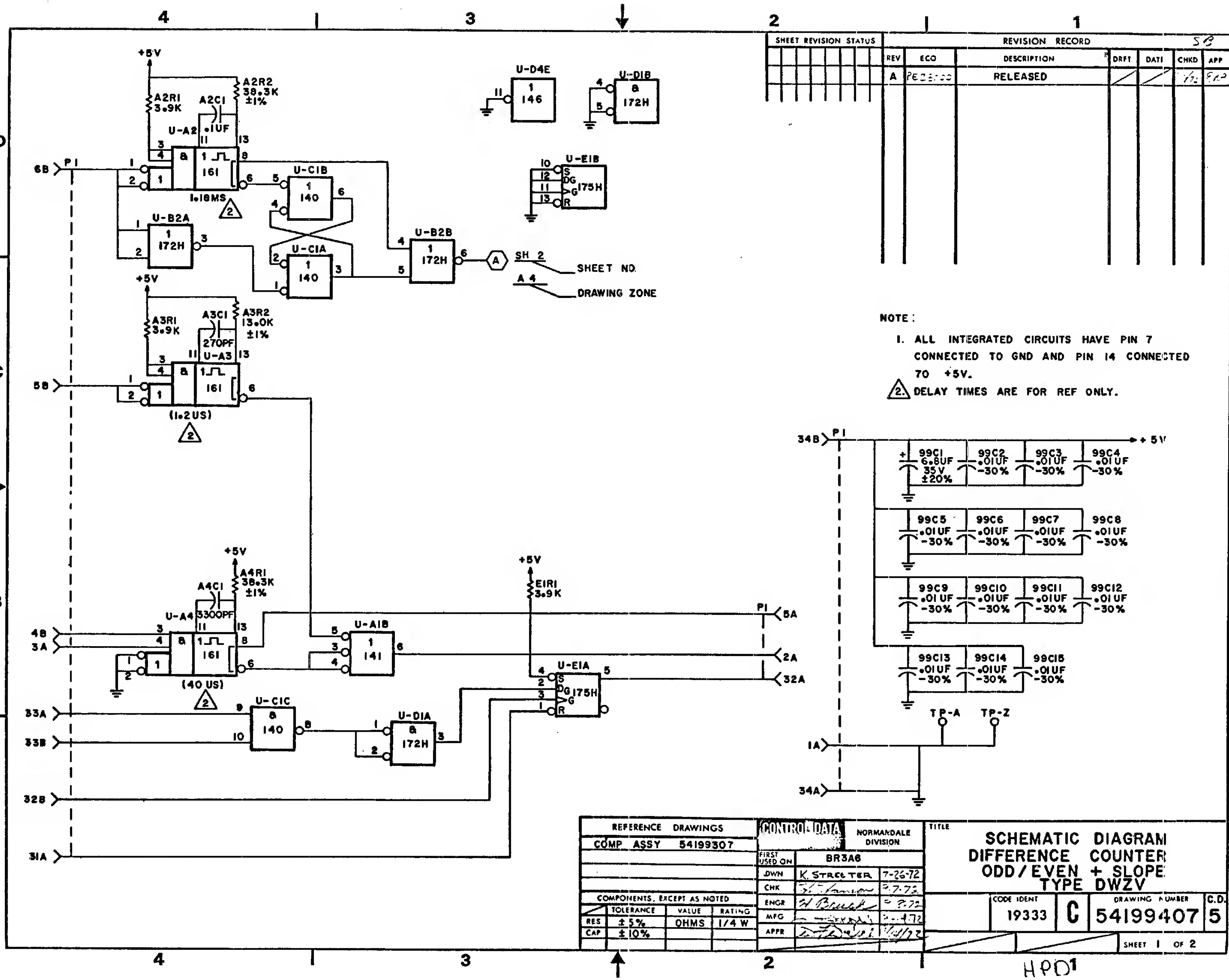
SHEET 1 of 2

54199404 A

4-230

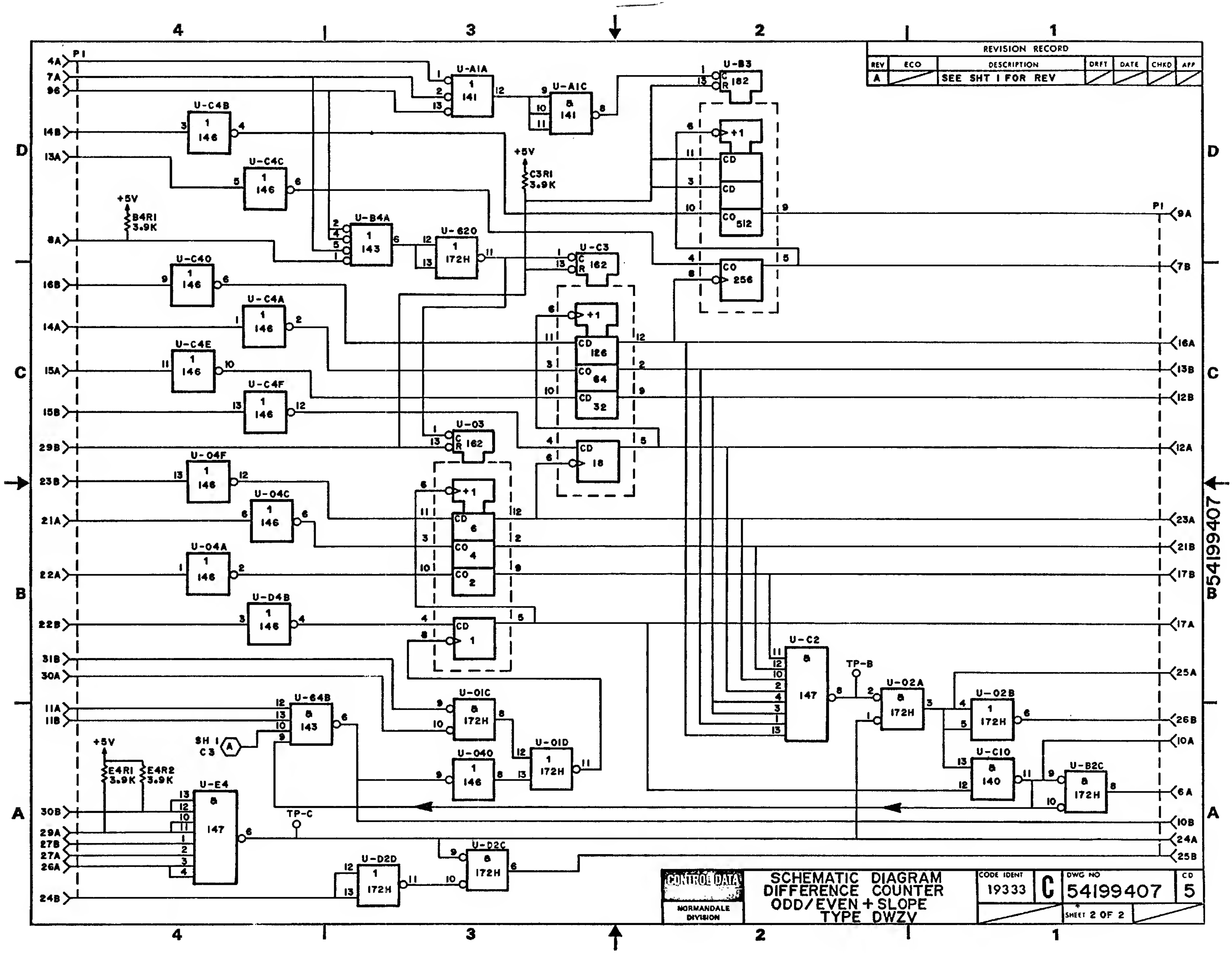


70629100 E



REVISION RECORD
SHEET REVISION STATUS
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
A | RELEASED
NOTE:
1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIMES ARE FOR REF ONLY.
SH 2 SHEET NO.
A 4 DRAWING ZONE
U-A2 161 1.18MS
U-A3 161 (1.2US)
U-A4 161 (40 US)
U-B2A 172H
U-B2B 172H
U-C1A 140
U-C1B 140
U-C1C 140
U-D1A 172H
U-D1B 172H
U-D4E 146
U-E1A 175H
U-E1B 175H
U-A1B 141
A2R1 3.9K
A2R2 38.3K ±1%
A2C1 .1UF
A3R1 3.9K
A3R2 13.0K ±1%
A3C1 270PF
A4R1 38.3K ±1%
A4C1 3300PF
E1R1 3.9K
99C1 6.8UF 35V ±20%
99C2–99C15 .01UF -30%
TP-A TP-Z
REFERENCE DRAWINGS
COMP ASSY 54199307
COMPONENTS, EXCEPT AS NOTED
TOLERANCE | VALUE | RATING
RES ±5% OHMS 1/4 W
CAP ±10%
CONTROL DATA NORMANDALE DIVISION
FIRST USED ON BR3A6
DWN K. STREETER 7-26-72
TITLE SCHEMATIC DIAGRAM DIFFERENCE COUNTER ODD/EVEN + SLOPE TYPE DWZV
CODE IDENT 19333 C
DRAWING NUMBER 54199407
C.D. 5
SHEET 1 OF 2
54199407
HPD1

4-232



70629100 E

COMMENT SHEET

PLEASE COMPLETE ITEMS 1 THRU 11

From

(1) NAME
(2) DEPARTMENT OR ATTENTION OF
(3) STREET ADDRESS
(4) CITY AND STATE

Manual Information (From Revision Record)

(5) MANUAL TITLE	
(6) PUBLICATION NO.	(7) REVISION
(8) FCO'S INCORPORATED INTO MANUAL	

Equipment Information (From Equipment Nameplate & FCO Log)

(9) EQUIPMENT NO. AND DESCRIPTION
(10) SERIES CODE
(11) FCO'S INCORPORATED INTO EQUIPMENT

Comments

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